MT7981B
Wi-Fi 6 Generation Router Platform: Registers Part 1

Open Version

Part 1: MCU and Bus Fabric
Clock and Power Control, General System
Part 2: Peripherals, Connectivity

Version: 1.0
Release Date: 2024-03-25

Version History

Version	Date	Description
1.0	2024-03-25	Initial release

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1 MCU and Bus Fabric

1.1 External Interrupt Controller

1.1.1 Register Definition

Module name: ap_cirq_eint Base address: (+10005000h)

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10005404	EINT_D0EN1	32	Domain 0 External Interrupt Enable Control Register
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Address	Name	Width	Register Function
10005600	EINT_DBNC_SET_3_0	32	External Interrupt Debounce Control Register
10005700	EINT_DBNC_CLR_3_0	32	External Interrupt Debounce Control Register
10005800	DEINT_CON	32	Direct Couple EINT Control Register
10005840	DEINT_SEL_3_0	32	Direct Couple EINT Select Control Register
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10005000 EINT_STA0 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND0	**Each bit read as 1 indicates the corresponding external interrupt is pending**

10005004 EINT_STA1 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND1	**Each bit read as 1 indicates the corresponding external interrupt is pending**

10005008 EINT_STA2 External Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_PEND2	**Each bit read as 1 indicates the corresponding external interrupt is pending**

10005040 EINT_ACK0 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK0	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005044 EINT_ACK1 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK1	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005048 EINT_ACK2 External Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_ACK2	**Write 1 to specific bit to acknowledge the corresponding external interrupt.**

10005080 EINT_MASK0 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK0	**External interrupt mask value**

10005084 EINT_MASK1 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK1	**External interrupt mask value**

10005088 EINT_MASK2 External Interrupt Mask Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK2	**External interrupt mask value**

100050C0 EINT_MASK_SET0 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET0	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

100050C4 EINT_MASK_SET1 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET1	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

100050C8 EINT_MASK_SET2 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET2	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005100 EINT_MASK_CLR0 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR0	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005104 EINT_MASK_CLR1 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR1	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005108 EINT_MASK_CLR2 External Interrupt Mask Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR2	**Write 1 to specific bit to set up the mask of corresponding external interrupt.**

10005140 EINT_SENS0 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS0	**External interrupt sensitivity value**

10005144 EINT_SENS1 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS1	**External interrupt sensitivity value**

10005148 EINT_SENS2 External Interrupt Sensitivity Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS2	**External interrupt sensitivity value**

10005180 EINT_SENS_SET0 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET0	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

10005184 EINT_SENS_SET1 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET1	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

10005188 EINT_SENS_SET2 External Interrupt Sensitivity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET2	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051C0 EINT_SENS_CLR0 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR0	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051C4 EINT_SENS_CLR1 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR1	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

100051C8 EINT_SENS_CLR2 External Interrupt Sensitivity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR2	**Write 1 to specific bit to set up the sensitivity of corresponding external interrupt.**

10005200 EINT_SOFT0 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT0	**Software interrupt value**

10005204 EINT_SOFT1 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT1	**Software interrupt value**

10005208 EINT_SOFT2 Software Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT2	**Software interrupt value**

10005240 EINT_SOFT_SET0 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET0	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005244 EINT_SOFT_SET1 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET1	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005248 EINT_SOFT_SET2 Software Interrupt Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET2	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005280 EINT_SOFT_CLR0 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR0	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005284 EINT_SOFT_CLR1 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR1	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005288 EINT_SOFT_CLR2 Software Interrupt Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SOFT_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR2	**Write 1 to specific bit to set up the corresponding software interrupt.**

10005300 EINT_POL0 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL0	**External interrupt polarity value**

10005304 EINT_POL1 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL1	**External interrupt polarity value**

10005308 EINT_POL2 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL2	**External interrupt polarity value**

10005340 EINT_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET0	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005344 EINT_POL_SET1 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET1	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005348 EINT_POL_SET2 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET2	**Write 1 to specific bit to set up the polarity of corresponding external interrupt.**

10005380 EINT_POL_CLR0 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR0	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005384 EINT_POL_CLR1 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR1	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005388 EINT_POL_CLR2 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR2	**Write 1 to specific bit to clear the polarity of corresponding external interrupt.**

10005400 EINT_D0EN0 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN0	**Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.**

10005404 EINT_D0EN1 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN1	**Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.**

10005408 EINT_D0EN2 Domain 0 External Interrupt Enable Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_D0EN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_D0EN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_D0EN2	**Write 1 to specific bit to enable the corresponding software external interrupt in domain 0.**

10005500 EINT_DBNC_3_0 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING3						DBNC_RST3	EN3	DBNC_SETTING2						DBNC_RST2	EN2
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING1						DBNC_RST1	EN1	DBNC_SETTING0						DBNC_RST0	EN0
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN2	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN0	**Enables de-bounce function** 0: Disable 1: Enable

10005600 EINT_DBNC_SET_3_0 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET3						DBNC_RST_SET3	EN_SET3	DBNC_SETTING_SET2						DBNC_RST_SET2	EN_SET2
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET1						DBNC_RST_SET1	EN_SET1	DBNC_SETTING_SET0						DBNC_RST_SET0	EN_SET0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET3	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET2	**Resets de-bounce counter** 0: Negative 1: Positive

Bit(s)	Mnemonic	Name	Description
16		EN_SET2	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET0	**Enables de-bounce function** 0: Disable 1: Enable

10005700 EINT_DBNC_CLR_3_0 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR3						DBNC_RST3	EN_CLR3		DBNC_SETTING_CLR_CLR2					DBNC_RST2	EN_CLR2
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR1						DBNC_RST1	EN_CLR1	DBNC_SETTING_CLR_CLR0						DBNC_RST0	EN_CLR0
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR3	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST3	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR3	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR2	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST2	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR2	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING_CLR_CLR1	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST1	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR1	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR0	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST0	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR0	**Enables de-bounce function** 0: Disable 1: Enable

10005800 DEINT_CON Direct Couple EINT Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEINT_CON3	DEINT_CON2	DEINT_CON1	DEINT_CON0
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3		DEINT_CON3	**Controls direct couple EINT3** 0: Disable 1: Enable
2		DEINT_CON2	**Controls direct couple EINT2** 0: Disable 1: Enable
1		DEINT_CON1	**Controls direct couple EINT1** 0: Disable 1: Enable
0		DEINT_CON0	**Controls direct couple EINT0** 0: Disable 1: Enable

10005840 DEINT_SEL_3_0 Direct Couple EINT Select Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Selects direct couple EINT3** #: EINT number
23:16		DEINT_SEL2	**Selects direct couple EINT2** #: EINT number
15:8		DEINT_SEL1	**Selects direct couple EINT1** #: EINT number
7:0		DEINT_SEL0	**Selects direct couple EINT0** #: EINT number

10005880 DEINT_SEL_SET_3_0 Direct Couple EINT Select Control Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Sets up direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Sets up direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Sets up direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Sets up direct couple EINT0 selection** #: EINT number

100058C0 DEINT_SEL_CLR_3_0 Direct Couple EINT Select Control Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEINT_SEL3								DEINT_SEL2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEINT_SEL1								DEINT_SEL0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24		DEINT_SEL3	**Clears direct couple EINT3 selection** #: EINT number
23:16		DEINT_SEL2	**Clears direct couple EINT2 selection** #: EINT number
15:8		DEINT_SEL1	**Clears direct couple EINT1 selection** #: EINT number
7:0		DEINT_SEL0	**Clears direct couple EINT0 selection** #: EINT number

10005900 EINT_EEVT EINT Wakeup Event Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EINT_EEVT
Type																RO
Reset																1

Bit(s)	Mnemonic	Name	Description
0		EINT_EEVT	**EINT wakeup event status**

10005A00 EINT_RAW_STA0 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND0	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)**

10005A04 EINT_RAW_STA1 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND1	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)**

10005A08 EINT_RAW_STA2 External Interrupt Raw Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_RAW_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_RAW_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_RAW_PEND2	**Each bit read as 1 indicates the corresponding external interrupt is pending (no matter it's mask or not)**

10005504 EINT_DBNC_7_4 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING7						DBNC_RST7	EN7	DBNC_SETTING6						DBNC_RST6	EN6
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING5						DBNC_RST5	EN5	DBNC_SETTING4						DBNC_RST4	EN4
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN6	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN4	**Enables de-bounce function** 0: Disable 1: Enable

10005604 EINT_DBNC_SET_7_4 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET7						DBNC_RST_SET7	EN_SET7	DBNC_SETTING_SET6						DBNC_RST_SET6	EN_SET6
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET5						DBNC_RST_SET5	EN_SET5	DBNC_SETTING_SET4						DBNC_RST_SET4	EN_SET4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET7	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET6	**Resets de-bounce counter** 0: Negative 1: Positive

Bit(s)	Mnemonic	Name	Description
16		EN_SET6	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET4	**Enables de-bounce function** 0: Disable 1: Enable

10005704 EINT_DBNC_CLR_7_4 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR7						DBNC_RST7	EN_CLR7		DBNC_SETTING_CLR_CLR6					DBNC_RST6	EN_CLR6
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR5						DBNC_RST5	EN_CLR5	DBNC_SETTING_CLR_CLR4						DBNC_RST4	EN_CLR4
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR7	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST7	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR7	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR6	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST6	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR6	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING_CLR_CLR5	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST5	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR5	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR4	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST4	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR4	**Enables de-bounce function** 0: Disable 1: Enable

10005508 EINT_DBNC_B_8 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING11						DBNC_RST11	EN11	DBNC_SETTING10						DBNC_RST10	EN10
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING9						DBNC_RST9	EN9	DBNC_SETTING8						DBNC_RST8	EN8
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN10	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN8	**Enables de-bounce function** 0: Disable 1: Enable

10005608 EINT_DBNC_SET_B_8 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET11						DBNC_RST_SET11	EN_SET11	DBNC_SETTING_SET10						DBNC_RST_SET10	EN_SET10
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET9						DBNC_RST_SET9	EN_SET9	DBNC_SETTING_SET8						DBNC_RST_SET8	EN_SET8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET11	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET10	**Resets de-bounce counter** 0: Negative

Bit(s)	Mnemonic	Name	Description
			1: Positive
16		EN_SET10	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET8	**Enables de-bounce function** 0: Disable 1: Enable

10005708 EINT_DBNC_CLR_B_8 External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR11						DBNC_RST11	EN_CLR11		DBNC_SETTING_CLR_CLR10					DBNC_RST10	EN_CLR10
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR9						DBNC_RST9	EN_CLR9	DBNC_SETTING_CLR_CLR8						DBNC_RST8	EN_CLR8
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR11	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST11	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR11	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR10	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST10	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR10	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING_CLR_CLR9	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST9	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR9	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR8	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST8	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR8	**Enables de-bounce function** 0: Disable 1: Enable

1000550C EINT_DBNC_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING15						DBNC_RST15	EN15	DBNC_SETTING14						DBNC_RST14	EN14
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING13						DBNC_RST13	EN13	DBNC_SETTING12						DBNC_RST12	EN12
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN14	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN12	**Enables de-bounce function** 0: Disable 1: Enable

1000560C EINT_DBNC_SET_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET15						DBNC_RST_SET15	EN_SET15	DBNC_SETTING_SET14						DBNC_RST_SET14	EN_SET14
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET13						DBNC_RST_SET13	EN_SET13	DBNC_SETTING_SET12						DBNC_RST_SET12	EN_SET12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_SET15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST_SET15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_SET15	**Enables de-bounce function** 0: Disable 1: Enable
23:20		DBNC_SETTING_SET14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST_SET14	**Resets de-bounce counter** 0: Negative

Bit(s)	Mnemonic	Name	Description
			1: Positive
16		EN_SET14	**Enables de-bounce function** 0: Disable 1: Enable
15:12		DBNC_SETTING_SET13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST_SET13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_SET13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_SET12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST_SET12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_SET12	**Enables de-bounce function** 0: Disable 1: Enable

1000570C EINT_DBNC_CLR_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR15						DBNC_RST15	EN_CLR15		DBNC_SETTING_CLR_CLR14					DBNC_RST14	EN_CLR14
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR13						DBNC_RST13	EN_CLR13	DBNC_SETTING_CLR_CLR12						DBNC_RST12	EN_CLR12
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28		DBNC_SETTING_CLR_CLR15	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
25		DBNC_RST15	**Resets de-bounce counter** 0: Negative 1: Positive
24		EN_CLR15	**Enables de-bounce function** 0: Disable 1: Enable
22:20		DBNC_SETTING_CLR_CLR14	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
17		DBNC_RST14	**Resets de-bounce counter** 0: Negative 1: Positive
16		EN_CLR14	**Enables de-bounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
15:12		DBNC_SETTING_CLR_CLR13	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
9		DBNC_RST13	**Resets de-bounce counter** 0: Negative 1: Positive
8		EN_CLR13	**Enables de-bounce function** 0: Disable 1: Enable
7:4		DBNC_SETTING_CLR_CLR12	**De-bounce setting** 0000: 0.125ms 0001: 0.25ms 0010: 0.5ms 0011: 1ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms Others: 0.5ms
1		DBNC_RST12	**Resets de-bounce counter** 0: Negative 1: Positive
0		EN_CLR12	**Enables de-bounce function** 0: Disable 1: Enable

100055CC EINT_DBNC_C_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING207						DBNC_RST207	EN207	DBNC_SETTING206						DBNC_RST206	EN206
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING205						DBNC_RST205	EN205	DBNC_SETTING204						DBNC_RST204	EN204
Type	RO						RO	RO	RO						RO	RO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28	DBNC_SETTING207		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST207		**Resets debounce counter** 0: Negative 1: Positive
24	EN207		**Enables debounce function** 0: Disable 1: Enable
23:20	DBNC_SETTING206		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms

Bit(s)	Mnemonic	Name	Description
			0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
17	DBNC_RST207		**Resets debounce counter** 0: Negative 1: Positive
16	EN206		**Enables debounce function** 0: Disable 1: Enable
15:12	DBNC_SETTING205		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
9	DBNC_RST205		**Resets debounce counter** 0: Negative 1: Positive
8	EN205		**Enables debounce function** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
7:4	DBNC_SETTING204		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
1	DBNC_RST204		**Resets debounce counter** 0: Negative 1: Positive
0	EN204		**Enables debounce function** 0: Disable 1: Enable

100056CC EINT_DBNC_SET_C_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_SET207						DBNC_RST_SET207	EN_SET207	DBNC_SETTING_SET206						DBNC_RST_SET206	EN_SET206
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_SET205						DBNC_RST_SET205	EN_SET205	DBNC_SETTING_SET204						DBNC_RST_SET204	EN_SET204
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28	DBNC_SETTING_SET207		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST_SET207		**Resets debounce counter** 0: Negative 1: Positive
24	EN_SET207		**Enables debounce function** 0: Disable 1: Enable
23:20	DBNC_SETTING_SET206		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms

Bit(s)	Mnemonic	Name	Description
			0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
17	DBNC_RST_SET206		**Resets debounce counter** 0: Negative 1: Positive
16	EN_SET206		**Enables debounce function** 0: Disable 1: Enable
15:12	DBNC_SETTING_SET205		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
9	DBNC_RST_SET205		**Resets debounce counter** 0: Negative 1: Positive
8	EN_SET205		**Enables debounce function** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
7:4	DBNC_SETTING_SET204		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
1	DBNC_RST_SET204		**Resets debounce counter** 0: Negative 1: Positive
0	EN_SET204		**Enables debounce function** 0: Disable 1: Enable

100057CC EINT_DBNC_CLR_C_F_C External Interrupt Debounce Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBNC_SETTING_CLR_CLR207						DBNC_RST207	EN_CLR207		DBNC_SETTING_CLR_CLR206					DBNC_RST206	EN_CLR206
Type	WO						WO	WO		WO					WO	WO
Reset	0	0	0	0			0	0		0	0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBNC_SETTING_CLR_CLR205						DBNC_RST205	EN_CLR205	DBNC_SETTING_CLR_CLR204						DBNC_RST204	EN_CLR204
Type	WO						WO	WO	WO						WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
31:28	DBNC_SETTING_CLR_CLR207		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
25	DBNC_RST207		**Resets debounce counter** 0: Negative 1: Positive
24	EN_CLR207		**Enables debounce function** 0: Disable 1: Enable
23:20	DBNC_SETTING_CLR_CLR206		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms

Bit(s)	Mnemonic	Name	Description
			0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
17	DBNC_RST206		**Resets debounce counter** 0: Negative 1: Positive
16	EN_CLR206		**Enables debounce function** 0: Disable 1: Enable
15:12	DBNC_SETTING_CLR_CLR205		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
9	DBNC_RST205		**Resets debounce counter** 0: Negative 1: Positive
8	EN_CLR205		**Enables debounce function** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
7:4	DBNC_SETTING_CLR_CLR204		**Debounce setting** 0000: 0.125 ms 0001: 0.25 ms 0010: 0.5 ms 0011: 1 ms 0100: 16 ms 0101: 32 ms 0110: 64 ms 0111: 128 ms 1000: 256 ms 1001: 512 ms Others: 0.5 ms
1	DBNC_RST204		**Resets debounce counter** 0: Negative 1: Positive
0	EN_CLR204		**Enables debounce function** 0: Disable 1: Enable

1.2 System Interrupt Controller

1.2.1 Register Definition

Module name: sys_cirq Base address: (+10204000h)

Address	Name	Width	Register Function
10204000	CIRQ_STA0	32	System CIRQ status register
10204004	CIRQ_STA1	32	System CIRQ status register
10204008	CIRQ_STA2	32	System CIRQ status register
1020400C	CIRQ_STA3	32	System CIRQ status register
10204010	CIRQ_STA4	32	System CIRQ status register
10204040	CIRQ_ACK0	32	System CIRQ acknowledge register
10204044	CIRQ_ACK1	32	System CIRQ acknowledge register
10204048	CIRQ_ACK2	32	System CIRQ acknowledge register
1020404C	CIRQ_ACK3	32	System CIRQ acknowledge register
10204050	CIRQ_ACK4	32	System CIRQ acknowledge register
10204080	CIRQ_MASK0	32	System CIRQ mask register
10204084	CIRQ_MASK1	32	System CIRQ mask register
10204088	CIRQ_MASK2	32	System CIRQ mask register
1020408C	CIRQ_MASK3	32	System CIRQ mask register
10204090	CIRQ_MASK4	32	System CIRQ mask register
102040C0	CIRQ_MASK_SET0	32	System CIRQ mask set register
102040C4	CIRQ_MASK_SET1	32	System CIRQ mask set register
102040C8	CIRQ_MASK_SET2	32	System CIRQ mask set register
102040CC	CIRQ_MASK_SET3	32	System CIRQ mask set register
102040D0	CIRQ_MASK_SET4	32	System CIRQ mask set register
10204100	CIRQ_MASK_CLR0	32	System CIRQ mask set register
10204104	CIRQ_MASK_CLR1	32	System CIRQ mask set register
10204108	CIRQ_MASK_CLR2	32	System CIRQ mask set register
1020410C	CIRQ_MASK_CLR3	32	System CIRQ mask set register
10204110	CIRQ_MASK_CLR4	32	System CIRQ mask set register
10204140	CIRQ_SENS0	32	System CIRQ sensitivity register
10204144	CIRQ_SENS1	32	System CIRQ sensitivity register
10204148	CIRQ_SENS2	32	System CIRQ sensitivity register
1020414C	CIRQ_SENS3	32	System CIRQ sensitivity register
10204150	CIRQ_SENS4	32	System CIRQ sensitivity register
10204180	CIRQ_SENS_SET0	32	System CIRQ sensitivity set register
10204184	CIRQ_SENS_SET1	32	System CIRQ sensitivity set register
10204188	CIRQ_SENS_SET2	32	System CIRQ sensitivity set register
1020418C	CIRQ_SENS_SET3	32	System CIRQ sensitivity set register
10204190	CIRQ_SENS_SET4	32	System CIRQ sensitivity set register
102041C0	CIRQ_SENS_CLR0	32	System CIRQ sensitivity clear register
102041C4	CIRQ_SENS_CLR1	32	System CIRQ sensitivity clear register
102041C8	CIRQ_SENS_CLR2	32	System CIRQ sensitivity clear register
102041CC	CIRQ_SENS_CLR3	32	System CIRQ sensitivity clear register
102041D0	CIRQ_SENS_CLR4	32	System CIRQ sensitivity clear register
10204200	CIRQ_POL0	32	External Interrupt Polarity Register
10204204	CIRQ_POL1	32	External Interrupt Polarity Register
10204208	CIRQ_POL2	32	External Interrupt Polarity Register
1020420C	CIRQ_POL3	32	External Interrupt Polarity Register
10204210	CIRQ_POL4	32	External Interrupt Polarity Register
10204240	CIRQ_POL_SET0	32	External Interrupt Polarity Set Register
10204244	CIRQ_POL_SET1	32	External Interrupt Polarity Set Register
10204248	CIRQ_POL_SET2	32	External Interrupt Polarity Set Register
1020424C	CIRQ_POL_SET3	32	External Interrupt Polarity Set Register

Address	Name	Width	Register Function
10204250	CIRQ_POL_SET4	32	External Interrupt Polarity Set Register
10204280	CIRQ_POL_CLR0	32	External Interrupt Polarity Clear Register
10204284	CIRQ_POL_CLR1	32	External Interrupt Polarity Clear Register
10204288	CIRQ_POL_CLR2	32	External Interrupt Polarity Clear Register
1020428C	CIRQ_POL_CLR3	32	External Interrupt Polarity Clear Register
10204290	CIRQ_POL_CLR4	32	External Interrupt Polarity Clear Register
10204300	CIRQ_CON	32	System CIRQ Control Register

10204000 CIRQ_STA0 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND0	**Each bit read as 1 indicates the corresponding system CIRQ is pending**

10204004 CIRQ_STA1 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND1	**Each bit read as 1 indicates the corresponding system CIRQ is pending**

10204008 CIRQ_STA2 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND2	**Each bit read as 1 indicates the corresponding system CIRQ is pending**

1020400C CIRQ_STA3 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_PEND3	**Each bit read as 1 indicates the corresponding system CIRQ is pending**

10204010 CIRQ_STA4 System CIRQ status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_PEND4														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_PEND4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_PEND4	**Each bit read as 1 indicates the corresponding system CIRQ is pending**

10204040 CIRQ_ACK0 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK0	**Write 1 to specific bit acknowledges the corresponding system CIRQ**

10204044 CIRQ_ACK1 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK1	**Write 1 to specific bit acknowledges the corresponding system CIRQ**

10204048 CIRQ_ACK2 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK2	**Write 1 to specific bit acknowledges the corresponding system CIRQ**

1020404C CIRQ_ACK3 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_ACK3	**Write 1 to specific bit acknowledges the corresponding system CIRQ**

10204050 CIRQ_ACK4 System CIRQ acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_ACK4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_ACK4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_ACK4	**Write 1 to specific bit acknowledges the corresponding system CIRQ**

10204080 CIRQ_MASK0 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK0	**System CIRQ mask value**

10204084 CIRQ_MASK1 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK1															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK1	**System CIRQ mask value**

10204088 CIRQ_MASK2 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK2	**System CIRQ mask value**

1020408C CIRQ_MASK3 System CIRQ mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK3	**System CIRQ mask value**

10204090 CIRQ_MASK4 System CIRQ mask register 7FFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK4														
Type		RO														
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK4	**System CIRQ mask value**

102040C0 CIRQ_MASK_SET0 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET0	**Write 1 to specific bit sets the mask of corresponding system CIRQ**

102040C4 **CIRQ_MASK_SET1** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET1	**Write 1 to specific bit sets the mask of corresponding system CIRQ**

102040C8 **CIRQ_MASK_SET2** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET2	**Write 1 to specific bit sets the mask of corresponding system CIRQ**

102040CC **CIRQ_MASK_SET3** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_SET3	**Write 1 to specific bit sets the mask of corresponding system CIRQ**

102040D0 **CIRQ_MASK_SET4** **System CIRQ mask set register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK_SET4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK_SET4	**Write 1 to specific bit sets the mask of corresponding system CIRQ**

10204100 CIRQ_MASK_CLR0 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR0	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204104 CIRQ_MASK_CLR1 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR1	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204108 CIRQ_MASK_CLR2 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR2	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

1020410C CIRQ_MASK_CLR3 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_MASK_CLR3	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204110 CIRQ_MASK_CLR4 System CIRQ mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_MASK_CLR4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_MASK_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_MASK_CLR4	**Write 1 to specific bit clear the mask of corresponding system CIRQ**

10204140 CIRQ_SENS0 System CIRQ sensitivity register FFFFFFE3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS0															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS0	**System CIRQ sensitivity value**

10204144 CIRQ_SENS1 System CIRQ sensitivity register FEFC7FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS1															
Type	RO															
Reset	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS1															
Type	RO															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS1	**System CIRQ sensitivity value**

10204148 CIRQ_SENS2 System CIRQ sensitivity register FFEFDFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS2															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS2															
Type	RO															
Reset	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS2	**System CIRQ sensitivity value**

1020414C **CIRQ_SENS3** **System CIRQ sensitivity register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS3															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS3	**System CIRQ sensitivity value**

10204150 **CIRQ_SENS4** **System CIRQ sensitivity register** **7F77FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS4														
Type		RO														
Reset		1	1	1	1	1	1	1	0	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS4															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS4	**System CIRQ sensitivity value**

10204180 CIRQ_SENS_SET0 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET0	**Write 1 to specific bit sets the sensitivity of corresponding system CIRQ**

10204184 CIRQ_SENS_SET1 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET1	**Write 1 to specific bit sets the sensitivity of corresponding system CIRQ**

10204188 CIRQ_SENS_SET2 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET2	**Write 1 to specific bit sets the sensitivity of corresponding system CIRQ**

1020418C CIRQ_SENS_SET3 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_SET3	**Write 1 to specific bit sets the sensitivity of corresponding system CIRQ**

10204190 CIRQ_SENS_SET4 System CIRQ sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS_SET4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS_SET4	**Write 1 to specific bit sets the sensitivity of corresponding system CIRQ**

102041C0 CIRQ_SENS_CLR0 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR0	**Write 1 to specific bit clear the sensitivity of corresponding system CIRQ**

102041C4 CIRQ_SENS_CLR1 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR1	**Write 1 to specific bit clear the sensitivity of corresponding system CIRQ**

102041C8 CIRQ_SENS_CLR2 System CIRQ sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR2	**Write 1 to specific bit clear the sensitivity of corresponding system CIRQ**

102041CC **CIRQ_SENS_CLR3** **System CIRQ sensitivity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_SENS_CLR3	**Write 1 to specific bit clear the sensitivity of corresponding system CIRQ**

102041D0 **CIRQ_SENS_CLR4** **System CIRQ sensitivity clear register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_SENS_CLR4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_SENS_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_SENS_CLR4	**Write 1 to specific bit clear the sensitivity of corresponding system CIRQ**

10204200 CIRQ_POL0 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL0	**System CIRQ polarity value**

10204204 CIRQ_POL1 External Interrupt Polarity Register 00038000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL1															
Type	RO															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL1	**System CIRQ polarity value**

10204208 CIRQ_POL2 External Interrupt Polarity Register 00102001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL2															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL2	**system CIRQ polarity value**

1020420C CIRQ_POL3 External Interrupt Polarity Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL3	**System CIRQ polarity value**

10204210 CIRQ_POL4 External Interrupt Polarity Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL4														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL4	**System CIRQ polarity value**

10204240 CIRQ_POL_SET0 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET0	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204244 CIRQ_POL_SET1 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET1	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204248 CIRQ_POL_SET2 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET2	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

1020424C CIRQ_POL_SET3 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_SET3	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204250 CIRQ_POL_SET4 External Interrupt Polarity Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL_SET4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_SET4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL_SET4	**Write 1 to specific bit sets the polarity of corresponding system CIRQ**

10204280 CIRQ_POL_CLR0 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR0	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204284 CIRQ_POL_CLR1 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR1	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204288 CIRQ_POL_CLR2 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR2	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

1020428C CIRQ_POL_CLR3 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		CIRQ_POL_CLR3	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204290 CIRQ_POL_CLR4 External Interrupt Polarity Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CIRQ_POL_CLR4														
Type		WO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIRQ_POL_CLR4															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30:0		CIRQ_POL_CLR4	**Write 1 to specific bit clear the polarity of corresponding system CIRQ**

10204300 CIRQ_CON System CIRQ Control Register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIRQ_EVENT_B															
Type	RO															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CIRQ_FLUSH	CIRQ_EDGE_ONLY	CIRQ_EN
Type														WO	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
31		CIRQ_EVENT_B	**Indicate sys_cirq_irq_b is triggered**
2		CIRQ_FLUSH	**Flush pending interrupts**
1		CIRQ_EDGE_ONLY	**Set edge-only mode, only edge-triggered interrupt will be recorded**
0		CIRQ_EN	**Enable bit of system CIRQ controller**

1.3 AP_DMA (Application Processor Direct Memory Access)

1.3.1 Register Definition

Module name: AP_DMA Base address: (+0x10217000)

Address	Name	Width	Register Function
10217020	AP_DMA_GLOBAL_INT_FLAG	32	AP DMA Global Interrupt Flag Register
10217004	AP_DMA_GLOBAL_RST	32	AP DMA Reset Register
10217024	AP_DMA_GLOBAL_RUNNING_STATUS	32	AP DMA Global Running Status Register
1021700C	AP_DMA_GLOBAL_SLOW_DOWN	32	AP DMA AXI Slow Down Register
10217010	AP_DMA_GLOBAL_SEC_EN	32	AP DMA Security Enable Register
10217080	AP_DMA_I2C0_CHN_INT_FLAG	32	Peripheral DMA Interrupt Flag Register
10217084	AP_DMA_I2C0_CHN_INT_EN	32	Peripheral DMA Interrupt Enable Register
10217088	AP_DMA_I2C0_CHN_EN	32	Peripheral DMA Enable Register
1021708C	AP_DMA_I2C0_CHN_RST	32	Peripheral DMA Reset Register
10217090	AP_DMA_I2C0_CHN_STOP	32	Peripheral DMA Enable Register
10217094	AP_DMA_I2C0_CHN_FLUSH	32	Peripheral DMA Flush Register
10217098	AP_DMA_I2C0_CHN_CON	32	Peripheral DMA Control Register
1021709C	AP_DMA_I2C0_CHN_TX_MEM_ADDR	32	Peripheral DMA Memory Address Register
102170A0	AP_DMA_I2C0_CHN_RX_MEM_ADDR	32	Peripheral DMA Memory Address Register
102170A4	AP_DMA_I2C0_CHN_TX_LEN	32	Peripheral DMA Transfer Length Register
102170A8	AP_DMA_I2C0_CHN_RX_LEN	32	Peripheral DMA Transfer Length Register
102170B8	AP_DMA_I2C0_CHN_INT_BUF_SIZE	32	Peripheral DMA Internal Buffer Size Register
102170D4	AP_DMA_I2C0_CHN_TX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
102170D8	AP_DMA_I2C0_CHN_RX_MEM_ADDR2	32	Peripheral DMA Memory Address Register
10217100	AP_DMA_UART_0_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
10217104	AP_DMA_UART_0_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
10217108	AP_DMA_UART_0_TX_EN	32	UART TX Virtual FIFO Enable Register
1021710C	AP_DMA_UART_0_TX_RST	32	UART TX Virtual FIFO Reset Register
10217110	AP_DMA_UART_0_TX_STOP	32	UART TX Virtual FIFO Enable Register
10217114	AP_DMA_UART_0_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1021711C	AP_DMA_UART_0_TX_VFF_ADDR	32	UART TX Virtual FIFO Base Address Register
10217124	AP_DMA_UART_0_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register
10217128	AP_DMA_UART_0_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1021712C	AP_DMA_UART_0_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
10217130	AP_DMA_UART_0_TX_VFF_RPT	32	UART TX Virtual FIFO Read Pointer Register
10217138	AP_DMA_UART_0_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1021713C	AP_DMA_UART_0_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
10217140	AP_DMA_UART_0_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
10217154	AP_DMA_UART_0_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
10217158	AP_DMA_UART_0_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1021715C	AP_DMA_UART_0_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
10217160	AP_DMA_UART_0_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
10217164	AP_DMA_UART_0_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
10217168	AP_DMA_UART_0_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
10217200	AP_DMA_UART_1_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
10217204	AP_DMA_UART_1_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
10217208	AP_DMA_UART_1_TX_EN	32	UART TX Virtual FIFO Enable Register
1021720C	AP_DMA_UART_1_TX_RST	32	UART TX Virtual FIFO Reset Register
10217210	AP_DMA_UART_1_TX_STOP	32	UART TX Virtual FIFO Enable Register
10217214	AP_DMA_UART_1_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1021721C	AP_DMA_UART_1_TX_VFF_ADDR	32	UART TX Virtual FIFO Base Address Register
10217224	AP_DMA_UART_1_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register

Address	Name	Width	Register Function
10217228	AP_DMA_UART_1_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1021722C	AP_DMA_UART_1_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
10217230	AP_DMA_UART_1_TX_VFF_RPT	32	UART TX Virtual FIFO Read Pointer Register
10217238	AP_DMA_UART_1_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1021723C	AP_DMA_UART_1_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
10217240	AP_DMA_UART_1_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
10217254	AP_DMA_UART_1_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
10217258	AP_DMA_UART_1_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1021725C	AP_DMA_UART_1_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
10217260	AP_DMA_UART_1_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
10217264	AP_DMA_UART_1_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
10217268	AP_DMA_UART_1_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
10217300	AP_DMA_UART_2_TX_INT_FLAG	32	UART TX Virtual FIFO Interrupt Flag Register
10217304	AP_DMA_UART_2_TX_INT_EN	32	UART TX Virtual FIFO Interrupt Enable Register
10217308	AP_DMA_UART_2_TX_EN	32	UART TX Virtual FIFO Enable Register
1021730C	AP_DMA_UART_2_TX_RST	32	UART TX Virtual FIFO Reset Register
10217310	AP_DMA_UART_2_TX_STOP	32	UART TX Virtual FIFO Enable Register
10217314	AP_DMA_UART_2_TX_FLUSH	32	UART TX Virtual FIFO Flush Register
1021731C	AP_DMA_UART_2_TX_VFF_ADDR	32	UART TX Virtual FIFO Base Address Register
10217324	AP_DMA_UART_2_TX_VFF_LEN	32	UART TX Virtual FIFO Length Register
10217328	AP_DMA_UART_2_TX_VFF_THRE	32	UART TX Virtual FIFO Threshold Register
1021732C	AP_DMA_UART_2_TX_VFF_WPT	32	UART TX Virtual FIFO Write Pointer Register
10217330	AP_DMA_UART_2_TX_VFF_RPT	32	UART TX Virtual FIFO Read Pointer Register
10217338	AP_DMA_UART_2_TX_INT_BUF_SIZE	32	UART Tx Internal Buffer Size Register
1021733C	AP_DMA_UART_2_TX_VFF_VALID_SIZE	32	UART Tx Virtual FIFO Valid Size Register
10217340	AP_DMA_UART_2_TX_VFF_LEFT_SIZE	32	UART Tx Virtual FIFO Left Size Register
10217354	AP_DMA_UART_2_TX_VFF_ADDR2	32	UART TX Virtual FIFO Base Address Register
10217358	AP_DMA_UART_2_TX_VFF_WPT_VALID	32	UART TX Virtual FIFO Write Pointer Register by HW Control
1021735C	AP_DMA_UART_2_TX_VFF_WPT_VALID2	32	UART TX Virtual FIFO Write Pointer Register by HW Control
10217360	AP_DMA_UART_2_TX_FLUSH_ACT	32	UART TX Virtual FIFO Flush Status Register
10217364	AP_DMA_UART_2_TX_HW_FLUSH	32	UART TX Virtual FIFO HW Flush Register
10217368	AP_DMA_UART_2_TX_VFF_WPT_REAL	32	UART TX Virtual FIFO Write Pointer Register Value
10217180	AP_DMA_UART_0_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
10217184	AP_DMA_UART_0_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
10217188	AP_DMA_UART_0_RX_EN	32	UART RX Virtual FIFO Enable Register
1021718C	AP_DMA_UART_0_RX_RST	32	UART RX Virtual FIFO Reset Register
10217190	AP_DMA_UART_0_RX_STOP	32	UART RX Virtual FIFO Enable Register
10217194	AP_DMA_UART_0_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1021719C	AP_DMA_UART_0_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
102171A4	AP_DMA_UART_0_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
102171A8	AP_DMA_UART_0_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register
102171AC	AP_DMA_UART_0_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
102171B0	AP_DMA_UART_0_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
102171B4	AP_DMA_UART_0_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
102171B8	AP_DMA_UART_0_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
102171BC	AP_DMA_UART_0_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
102171C0	AP_DMA_UART_0_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
102171D4	AP_DMA_UART_0_RX_VFF_ADDR2	32	UART RX Virtual FIFO Base Address Register
10217280	AP_DMA_UART_1_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
10217284	AP_DMA_UART_1_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
10217288	AP_DMA_UART_1_RX_EN	32	UART RX Virtual FIFO Enable Register
1021728C	AP_DMA_UART_1_RX_RST	32	UART RX Virtual FIFO Reset Register

Address	Name	Width	Register Function
10217290	AP_DMA_UART_1_RX_STOP	32	UART RX Virtual FIFO Enable Register
10217294	AP_DMA_UART_1_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1021729C	AP_DMA_UART_1_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
102172A4	AP_DMA_UART_1_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
102172A8	AP_DMA_UART_1_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register
102172AC	AP_DMA_UART_1_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
102172B0	AP_DMA_UART_1_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
102172B4	AP_DMA_UART_1_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
102172B8	AP_DMA_UART_1_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
102172BC	AP_DMA_UART_1_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
102172C0	AP_DMA_UART_1_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
102172D4	AP_DMA_UART_1_RX_VFF_ADDR2	32	UART RX Virtual FIFO Base Address Register
10217380	AP_DMA_UART_2_RX_INT_FLAG	32	UART RX Virtual FIFO Interrupt Flag Register
10217384	AP_DMA_UART_2_RX_INT_EN	32	UART RX Virtual FIFO Interrupt Enable Register
10217388	AP_DMA_UART_2_RX_EN	32	UART RX Virtual FIFO Enable Register
1021738C	AP_DMA_UART_2_RX_RST	32	UART RX Virtual FIFO Reset Register
10217390	AP_DMA_UART_2_RX_STOP	32	UART RX Virtual FIFO Enable Register
10217394	AP_DMA_UART_2_RX_FLUSH	32	UART RX Virtual FIFO Flush Register
1021739C	AP_DMA_UART_2_RX_VFF_ADDR	32	UART RX Virtual FIFO Base Address Register
102173A4	AP_DMA_UART_2_RX_VFF_LEN	32	UART RX Virtual FIFO Length Register
102173A8	AP_DMA_UART_2_RX_VFF_THRE	32	UART RX Virtual FIFO Threshold Register
102173AC	AP_DMA_UART_2_RX_VFF_WPT	32	UART RX Virtual FIFO Write Pointer Register
102173B0	AP_DMA_UART_2_RX_VFF_RPT	32	UART RX Virtual FIFO Read Pointer Register
102173B4	AP_DMA_UART_2_RX_FLOW_CTRL_THRE	32	UART RX Virtual FIFO Flow Control Threshold
102173B8	AP_DMA_UART_2_RX_INT_BUF_SIZE	32	UART Rx Internal Buffer Size Register
102173BC	AP_DMA_UART_2_RX_VFF_VALID_SIZE	32	UART Rx Virtual FIFO Valid Size Register
102173C0	AP_DMA_UART_2_RX_VFF_LEFT_SIZE	32	UART Rx Virtual FIFO Left Size Register
102173D4	AP_DMA_UART_2_RX_VFF_ADDR2	32	UART RX Virtual FIFO Base Address Register

10217020 AP_DMA_GLOBAL_INT_FLAG AP DMA Global Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C0
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	UART2_RX	**UART2 RX interrupt** 0: No interrupt event 1: Interrupt event occurred
5	UART2_TX	**UART2 TX interrupt** 0: No interrupt event 1: Interrupt event occurred
4	UART1_RX	**UART1 RX interrupt** 0: No interrupt event 1: Interrupt event occurred
3	UART1_TX	**UART1 TX interrupt** 0: No interrupt event 1: Interrupt event occurred
2	UART0_RX	**UART0 RX interrupt** 0: No interrupt event 1: Interrupt event occurred
1	UART0_TX	**UART0 TX interrupt** 0: No interrupt event 1: Interrupt event occurred
0	I2C0	**I2C0 interrupt** 0: No interrupt event 1: Interrupt event occurred

10217004 AP_DMA_GLOBAL_RST AP DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**General DMA hard reset (reset regardless of the current transaction)** SW sets hard_rst to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**General DMA warm reset (after the current transaction)** SW sets warm_rst to 1 and waits for all running statuses to become 0. SW then sets warm_rst back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217024 AP_DMA_GLOBAL_RUNNING_STATUS AP DMA Global Running Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										UART2_RX	UART2_TX	UART1_RX	UART1_TX	UART0_RX	UART0_TX	I2C0
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	UART2_RX	0: Idle
		1: Running
5	UART2_TX	0: Idle
		1: Running
4	UART1_RX	0: Idle
		1: Running
3	UART1_TX	0: Idle
		1: Running
2	UART0_RX	0: Idle
		1: Running
1	UART0_TX	0: Idle
		1: Running
0	I2C0	0: Idle
		1: Running

1021700C AP_DMA_GLOBAL_SLOW_DOWN AP DMA AXI Slow Down Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	W_SLOW_CNT															W_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R_SLOW_CNT															R_SLOW_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0						0

Bit(s)	Name	Description
31:22	W_SLOW_CNT	**AXI write to external AXI slow-down counter (0~1023)** The number means cycle. 0: Wait for 0 cycle and then issue request 1: Wait for 1 cycle and then issue request
16	W_SLOW_EN	**Enables AXI write to external AXI slow-down** 0: Do not slow down 1: Slow down
15:6	R_SLOW_CNT	**AXI read from external AXI slow-down counter (0~1023)** The number means cycle. 0: Wait for 0 cycle and then issue request 1: Wait for 1 cycle and then issue request
0	R_SLOW_EN	**Enables ARM side AXI read from external AXI slow-down** 0: Do not slow down 1: Slow down

10217010 AP_DMA_GLOBAL_SEC_EN AP DMA Security Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOCK	DLOCK														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	LOCK	**Locks the secure bit** 0: Unlock channel secure bit write 1: Lock channel secure bit
30	DLOCK	**Locks the domain registers** 0: Unlock channel domain register write 1: Lock channel domain register write

10217080 AP_DMA_I2C0_CHN_INT_FLAG Peripheral DMA Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RX_FLAG	TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RX_FLAG	**Raised when RX DMA is finished. Write 0 to clear it.**
0	TX_FLAG	**This flag is raised when TX DMA is finished. Write 0 to clear it.** 1. After normal operation is done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 2. If STOP = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 3. If FLUSH = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will be set to 1. 4. If WARM_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1. 5. If HARD_RST = 1 and operation done, EN will be set from 1 to 0, and interrupt flag will not be set to 1.

10217084 AP_DMA_I2C0_CHN_INT_EN Peripheral DMA Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN_RX_FLAG	INTEN_TX_FLAG
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN_RX_FLAG	**Enables interrupt for RX_FLAG** 0: Disable 1: Enable
0	INTEN_TX_FLAG	**Enables interrupt for TX_FLAG** 0: Disable 1: Enable

10217088 AP_DMA_I2C0_CHN_EN Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables peripheral DMA** Set to 1 to start DMA. When DMA is busy, EN will always be 1. When DMA is finished, EN will be set to 0. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When FLUSH is set, EN will be 0 after the nearest transaction is finished and all internal data are delivered to destination; then, DMA stops. When STOP is set, EN will be 0 after the nearest transaction is finished. 0: Disable 1: Enable

1021708C AP_DMA_I2C0_CHN_RST Peripheral DMA Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (reset regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217090 AP_DMA_I2C0_CHN_STOP Peripheral DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PAUSE	STOP
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Pauses peripheral DMA** Set to 1 to pause DMA and back to 0 to resume DMA. 0: Disable 1: Enable
0	STOP	**Stops peripheral DMA** Set to 1 to stop DMA and wait for EN to become 0. HW then auto sets STOP back to 0 to finish the stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217094 AP_DMA_I2C0_CHN_FLUSH Peripheral DMA Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes peripheral DMA** Set to 1 to stop DMA and allow DMA to flush its internal buffer residual data to EMI. After flush is finished, DMA will set EN back to 0 and stop DMA. There may still be data not transferred (len may not be 0). SW will set FLUSH to 1, wait for EN to become 0, and HW will auto set FLUSH back to 0 to finish the flush mechanism. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217098 AP_DMA_I2C0_CHN_CON Peripheral DMA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							dir_change	addr_ctrl			align	skip_config	req_blk	async_mode	FIX_EN	DIR
Type							RW	RW			RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	dir_change	**If I2C needs direction change, please set 1.**
8:6	addr_ctrl	**Make this reg as default.**
5	align	**Make this reg as default.** 0: Half word alignment 1: Word alignment
4	skip_config	**Please configure 1 as I2C setting.** 0: Configure 1: No configuration
3	req_blk	**Make this reg as default.** 0: Request block 1: Non-request block
2	async_mode	**Please configure 1 as I2C setting.** 0: Old hand-shake 1: New hand-shake
1	FIX_EN	**Peripheral DMA fixed pattern** When FIX_EN is turned on, DIR will be ignored, and DMA will always treat this transfer as TX. 0: Do not use fixed pattern 1: Use fixed pattern
0	DIR	**Half duplex peripheral DMA direction** 0: TX 1: RX

1021709C **AP_DMA_I2C0_CHN_TX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. When FIX_EN = 1, TX_MEM_ADDR will be treated as FIX_PATTERN. DO NOT set TX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination; e.g. 0xff9 ~ 0xfff are not allowed to be TX_MEM_ADDR when users use SYSRAM as a source memory.

102170A0 **AP_DMA_I2C0_CHN_RX_MEM_ADDR** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MEM_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MEM_ADDR	**Peripheral DMA memory address** It can be any byte alignment. This address will be increased after each bus transaction. DO NOT set RX_MEM_ADDR to be within the last 8 bytes before a 4KB boundary when users use SYSRAM as a destination; e.g. 0xff9 ~ 0xfff are not allowed to be RX_MEM_ADDR when users use SYSRAM as a destination memory.

102170A4 AP_DMA_I2C0_CHN_TX_LEN Peripheral DMA Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how much data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

102170A8 AP_DMA_I2C0_CHN_RX_LEN Peripheral DMA Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_LEN	**Peripheral DMA transfer length** It can be any byte alignment. This number will decrease after each bus transaction. This number also indicates how much data have not been delivered. 0: 0 byte transfer 1: 1 byte transfer

102170B8 AP_DMA_I2C0_CHN_INT_BUF_SIZE Peripheral DMA Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									INT_BUF_SIZE							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	INT_BUF_SIZE	**Byte size in internal buffer**

102170D4 **AP_DMA_I2C0_CHN_TX_MEM_ADDR2** **Peripheral DMA Memory Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_MEM_ADDR2	**Peripheral DMA TX memory address bit [32]**

102170D8 AP_DMA_I2C0_CHN_RX_MEM_ADDR2 Peripheral DMA Memory Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_MEM_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_MEM_ADDR2	**Peripheral DMA TX memory address bit [32]**

10217100 AP_DMA_UART_0_TX_INT_FLAG UART TX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG = 1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN = 1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

10217104 AP_DMA_UART_0_TX_INT_EN UART TX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Do not set flag to 1, even when tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto sets inten back to 0 when tx_vff_left_size >= tx_vff_thrs

10217108 AP_DMA_UART_0_TX_EN UART TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1021710C AP_DMA_UART_0_TX_RST UART TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217110 AP_DMA_UART_0_TX_STOP UART TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217114 AP_DMA_UART_0_TX_FLUSH UART TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even if MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021711C AP_DMA_UART_0_TX_VFF_ADDR UART TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

10217124 AP_DMA_UART_0_TX_VFF_LEN UART TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

10217128 AP_DMA_UART_0_TX_VFF_THRE UART TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when left size in VFF is bigger than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1021712C AP_DMA_UART_0_TX_VFF_WPT UART TX Virtual FIFO Write Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

10217130 AP_DMA_UART_0_TX_VFF_RPT UART TX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

10217138 AP_DMA_UART_0_TX_INT_BUF_SIZE UART Tx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1021713C AP_DMA_UART_0_TX_VFF_VALID_SIZE UART Tx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

10217140 AP_DMA_UART_0_TX_VFF_LEFT_SIZE UART Tx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

10217154 AP_DMA_UART_0_TX_VFF_ADDR2 UART TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_VFF_ADDR2	**UART memory address bit[32]**

10217158 AP_DMA_UART_0_TX_VFF_WPT_VALID UART TX Virtual FIFO Write Pointer Register by HW Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH = 0, sync to TX_VFF_WPT_WRAP. If flushing, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH = 0, sync to TX_VFF_WPT. If flushing, it will not update the value until the flush is finished.

1021715C **AP_DMA_UART_0_TX_VFF_WPT_VALID2** **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH = 0, sync to TX_VFF_WPT. If flushing, it will not update the value until the flush is finished.

10217160 AP_DMA_UART_0_TX_FLUSH_ACT UART TX Virtual FIFO Flush Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART TX channel is flushing.**
0	FLUSH_ACT	**UART TX channel flush status**

10217164 AP_DMA_UART_0_TX_HW_FLUSH UART TX Virtual FIFO HW Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush = 0

10217168 **AP_DMA_UART_0_TX_VFF_WPT_REAL** **UART TX Virtual FIFO Write Pointer Register Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

10217200 AP_DMA_UART_1_TX_INT_FLAG UART TX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG = 1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN = 1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

10217204 AP_DMA_UART_1_TX_INT_EN UART TX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Do not set flag to 1, even when tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

10217208 AP_DMA_UART_1_TX_EN UART TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1021720C AP_DMA_UART_1_TX_RST UART TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217210 AP_DMA_UART_1_TX_STOP UART TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217214 AP_DMA_UART_1_TX_FLUSH UART TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even when MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021721C AP_DMA_UART_1_TX_VFF_ADDR UART TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

10217224 AP_DMA_UART_1_TX_VFF_LEN UART TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

10217228 AP_DMA_UART_1_TX_VFF_THRE UART TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when left size in VFF is bigger than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1021722C **AP_DMA_UART_1_TX_VFF_WPT** **UART TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

10217230 AP_DMA_UART_1_TX_VFF_RPT UART TX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

10217238 AP_DMA_UART_1_TX_INT_BUF_SIZE UART Tx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1021723C **AP_DMA_UART_1_TX_VFF_VALID_SIZE** **UART Tx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

10217240 **AP_DMA_UART_1_TX_VFF_LEFT_SIZE** **UART Tx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

10217254 AP_DMA_UART_1_TX_VFF_ADDR2 UART TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_VFF_ADDR2	**UART memory address bit[32]**

10217258 **AP_DMA_UART_1_TX_VFF_WPT_VALID** **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH = 0, sync to TX_VFF_WPT_WRAP. If flushing, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH = 0, sync to TX_VFF_WPT. If flushing, it will not update the value until the flush is finished.

1021725C **AP_DMA_UART_1_TX_VFF_WPT_VALID2** **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH = 0, sync to TX_VFF_WPT. If flushing, it will not update the value until the flush is finished.

10217260 AP_DMA_UART_1_TX_FLUSH_ACT UART TX Virtual FIFO Flush Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART TX channel is flushing.**
0	FLUSH_ACT	**UART TX channel flush status**

10217264 AP_DMA_UART_1_TX_HW_FLUSH UART TX Virtual FIFO HW Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush =0

10217268 **AP_DMA_UART_1_TX_VFF_WPT_REAL** **UART TX Virtual FIFO Write Pointer Register Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

10217300 AP_DMA_UART_2_TX_INT_FLAG UART TX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLAG0
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLAG0	**Write 0 to clear it.** Interrupt will be issued to HW when FLAG = 1. Mechanism: 1. SW puts data into VFF and detects TX_VFF_LEFT_SIZE is approaching 0. 2. SW sets INTEN = 1 and leaves the task to wait for interrupt. 3. When HW delivers enough data to UART and makes TX_VFF_LEFT_SIZE >= TX_VFF_THRS, HW sets the flag to 1 and issues interrupt. 4. When SW receives this interrupt, it must set FLAG back to 0 and go on pushing data into VFF.

10217304 AP_DMA_UART_2_TX_INT_EN UART TX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																INTEN
Type																RW
Reset																0

Bit(s)	Name	Description
0	INTEN	**Controls interrupt enabling** This bit is used to control if the flag will be set to 1 when TX_VFF_LEFT_SIZE >= TX_VFF_THRS. 0: Do not set flag to 1, even when tx_vff_left_size >= tx_vff_thrs 1: Set flag to 1 and HW auto set inten back to 0 when tx_vff_left_size >= tx_vff_thrs

10217308 AP_DMA_UART_2_TX_EN UART TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART TX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. When EN = 0 and MCU writes data to the VFF_W port (an AHB slave port), VFF_W will ignore this command, and the data will not be written to virtual FIFO. 0: Disable 1: Enable

1021730C AP_DMA_UART_2_TX_RST UART TX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217310 AP_DMA_UART_2_TX_STOP UART TX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART TX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Disable 1: Enable

10217314 AP_DMA_UART_2_TX_FLUSH UART TX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART TX virtual FIFO** Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual due to MCU keeps putting data or in-coherent problems (data received by VFF_W behind receiving flush even when MCU issues data first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021731C AP_DMA_UART_2_TX_VFF_ADDR UART TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	TX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

10217324 AP_DMA_UART_2_TX_VFF_LEN UART TX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	TX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

10217328 AP_DMA_UART_2_TX_VFF_THRE UART TX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_THRE	**VFF threshold in byte alignment** In TX mode, DMA issues interrupt when left size in VFF is bigger than the threshold. In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold.

1021732C **AP_DMA_UART_2_TX_VFF_WPT** **UART TX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP	**TX VFF write pointer wrap bit** It is initialized to 0. When wrapped to the ring head again, invert this bit. For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.
15:0	TX_VFF_WPT	**Byte alignment FIFO write pointer** For UART TX, this pointer is read only. (VFF is maintained by hardware.) For BTIF TX VFF, the write pointer is maintained by software.

10217330 AP_DMA_UART_2_TX_VFF_RPT UART TX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_RPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_RPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_RPT_WRAP	**TX VFF read pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	TX_VFF_RPT	**TX VFF read pointer maintained by hardware** In byte alignment.

10217338 AP_DMA_UART_2_TX_INT_BUF_SIZE UART Tx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	TX_INT_BUF_SIZE	**Virtual FIFO DMA TX internal buffer size** 0: 0 byte 1: 1 byte

1021733C AP_DMA_UART_2_TX_VFF_VALID_SIZE UART Tx Virtual FIFO Valid Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_VALID_SIZE	**TX virtual FIFO valid size** 0: 0 byte 1: 1 byte

10217340 AP_DMA_UART_2_TX_VFF_LEFT_SIZE UART Tx Virtual FIFO Left Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_LEFT_SIZE	**TX virtual FIFO left size** 0: 0 byte 1: 1 byte

10217354 AP_DMA_UART_2_TX_VFF_ADDR2 UART TX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TX_VFF_ADDR2	**UART memory address bit[32]**

10217358 **AP_DMA_UART_2_TX_VFF_WPT_VALID** **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_VALID
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_VALID	**TX VFF write pointer wrap bit** If FLUSH = 0, sync to TX_VFF_WPT_WRAP. If flushing, it will not update the value until the flush is finished.
15:0	TX_VFF_WPT_VALID	**TX VFF write pointer** If FLUSH = 0, sync to TX_VFF_WPT. If flushing, it will not update the value until the flush is finished.

1021735C **AP_DMA_UART_2_TX_VFF_WPT_VALID2** **UART TX Virtual FIFO Write Pointer Register by HW Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_VALID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TX_VFF_WPT_VALID2	**TX VFF write pointer** If FLUSH = 0, sync to TX_VFF_WPT. If flushing, it will not update the value until the flush is finished.

10217360 AP_DMA_UART_2_TX_FLUSH_ACT UART TX Virtual FIFO Flush Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLUSH_NEXT	FLUSH_ACT
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	FLUSH_NEXT	**There is a flush command when the UART TX channel is flushing.**
0	FLUSH_ACT	**UART TX channel flush status**

10217364 AP_DMA_UART_2_TX_HW_FLUSH UART TX Virtual FIFO HW Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																HW_FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	HW_FLUSH	**Flush control bit** Controls the UART TX write pointer if the SW setting value at flushing is updated. 0: Update wpt with SW setting 1: Update wpt when flush = 0

10217368 **AP_DMA_UART_2_TX_VFF_WPT_REAL** **UART TX Virtual FIFO Write Pointer Register Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TX_VFF_WPT_WRAP_REAL
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_VFF_WPT_REAL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TX_VFF_WPT_WRAP_REAL	**TX VFF write pointer wrap bit** If HW_FLUSH = 1, sync to TX_VFF_WPT_WRAP_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT_WRAP.
15:0	TX_VFF_WPT_REAL	**TX VFF write pointer** If HW_FLUSH = 1, sync to TX_VFF_WPT_VALID. If HW_FLUSH = 0, sync to TX_VFF_WPT.

10217180 AP_DMA_UART_0_RX_INT_FLAG UART RX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

10217184 AP_DMA_UART_0_RX_INT_EN UART RX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However, even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However, even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

10217188 AP_DMA_UART_0_RX_EN UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021718C AP_DMA_UART_0_RX_RST UART RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217190 AP_DMA_UART_0_RX_STOP UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217194 AP_DMA_UART_0_RX_FLUSH UART RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual because MCU keeps putting data or in-coherent problems (DMA receives data by VFF_W after receiving flush, even if MCU issues data to VFF first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021719C AP_DMA_UART_0_RX_VFF_ADDR UART RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

102171A4 AP_DMA_UART_0_RX_VFF_LEN UART RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

102171A8 **AP_DMA_UART_0_RX_VFF_THRE** **UART RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold. In TX mode, DMA issues interrupt when left size in VFF is bigger than the threshold.

102171AC **AP_DMA_UART_0_RX_VFF_WPT** **UART RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

102171B0 AP_DMA_UART_0_RX_VFF_RPT UART RX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

102171B4 AP_DMA_UART_0_RX_FLOW_CTRL_THRE UART RX Virtual FIFO Flow Control Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

102171B8 **AP_DMA_UART_0_RX_INT_BUF_SIZE** **UART Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

102171BC **AP_DMA_UART_0_RX_VFF_VALID_SIZE** **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

102171C0 **AP_DMA_UART_0_RX_VFF_LEFT_SIZE** **UART Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

102171D4 AP_DMA_UART_0_RX_VFF_ADDR2 UART RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_VFF_ADDR2	**UART memory address bit[32]**

10217280 AP_DMA_UART_1_RX_INT_FLAG UART RX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

10217284 AP_DMA_UART_1_RX_INT_EN UART RX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However, even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However, even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

10217288 AP_DMA_UART_1_RX_EN UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021728C AP_DMA_UART_1_RX_RST UART RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217290 AP_DMA_UART_1_RX_STOP UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217294 AP_DMA_UART_1_RX_FLUSH UART RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual because MCU keeps putting data or in-coherent problems (DMA receives data by VFF_W after receiving flush, even if MCU issues data to VFF first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021729C AP_DMA_UART_1_RX_VFF_ADDR UART RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

102172A4 AP_DMA_UART_1_RX_VFF_LEN UART RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

102172A8 **AP_DMA_UART_1_RX_VFF_THRE** **UART RX Virtual FIFO Threshold Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold. In TX mode, DMA issues interrupt when left size in VFF is bigger than the threshold.

102172AC **AP_DMA_UART_1_RX_VFF_WPT** **UART RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

102172B0 AP_DMA_UART_1_RX_VFF_RPT UART RX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

102172B4 AP_DMA_UART_1_RX_FLOW_CTRL_THRE UART RX Virtual FIFO Flow Control Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

102172B8 **AP_DMA_UART_1_RX_INT_BUF_SIZE** **UART Rx Internal Buffer Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

102172BC **AP_DMA_UART_1_RX_VFF_VALID_SIZE** **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

102172C0 **AP_DMA_UART_1_RX_VFF_LEFT_SIZE** **UART Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

102172D4 AP_DMA_UART_1_RX_VFF_ADDR2 UART RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_VFF_ADDR2	**UART memory address bit[32]**

10217380 AP_DMA_UART_2_RX_INT_FLAG UART RX Virtual FIFO Interrupt Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															FLAG1	FLAG0
Type															W1C	W1C
Reset															0	0

Bit(s)	Name	Description
1	FLAG1	**Write 1 to clear it.** This flag is raised when UART issues flush to DMA and all data in UART FIFO are transferred to VFF.
0	FLAG0	**Write 1 to clear it.** This flag is raised when rx_vff_valid_size >= rx_vff_thre. (VFF is almost full and MCU needs to consume those data.)

10217384 AP_DMA_UART_2_RX_INT_EN UART RX Virtual FIFO Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															INTEN1	INTEN0
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	INTEN1	**Controls interrupt enabling** Only when this bit is set to 1 will flag1 be set to 1, and the interrupt will be sent out to CPU. However, even without this bit set to 1, flag1 will still be set to 1 regardless of this bit. 0: Disable 1: Enable
0	INTEN0	**Controls interrupt enabling** Only when this bit is set to 1 will flag0 be set to 1, and the interrupt will be sent out to CPU. However, even without this bit set to 1, flag0 will still be set to 1 regardless of this bit. 0: Disable 1: Enable

10217388 AP_DMA_UART_2_RX_EN UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	EN	**Enables UART1 RX virtual FIFO** Set EN to 1 to start DMA. When DMA is busy, EN will always be 1. When warm reset is set, EN will be 0 after the nearest transaction is finished, and all statuses in DMA will be reset. When hard reset is set, EN will immediately become 0, and all statuses in DMA will be reset. 0: Disable 1: Enable

1021738C AP_DMA_UART_2_RX_RST UART RX Virtual FIFO Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															HARD_RST	WARM_RST
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	HARD_RST	**Peripheral DMA hard reset (regardless of the current transaction)** SW sets HARD_RST to 1 then back to 0 to finish the reset mechanism. 0: Disable 1: Enable
0	WARM_RST	**Peripheral DMA warm reset (after the current transaction)** SW sets WARM_RST to 1 and waits for EN to become 0. HW auto sets WARM_RST back to 0 to finish the reset mechanism. 0: Disable 1: Enable

10217390 AP_DMA_UART_2_RX_STOP UART RX Virtual FIFO Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP	**Stops UART RX virtual FIFO** Set STOP to 1 to stop DMA, wait for EN to become 0 and set STOP back to 0 to finish stop mechanism. When DMA is set to stop, it will finish the current transaction. After that, EN will become 0 without resetting any status in DMA. 0: Disable 1: Enable

10217394 AP_DMA_UART_2_RX_FLUSH UART RX Virtual FIFO Flush Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLUSH
Type																RW
Reset																0

Bit(s)	Name	Description
0	FLUSH	**Flushes UART RX virtual FIFO** Set FLUSH to 1 to allow DMA to flush its internal buffer residual data to EMI. However, even after flush there may still be data in residual because MCU keeps putting data or in-coherent problems (DMA receives data by VFF_W after receiving flush, even if MCU issues data to VFF first). Therefore, SW must recheck the residual data. If not 0, flush again. Note: STOP and FLUSH cannot be set to 1 in the same operation. 0: Flush finished 1: Enable

1021739C AP_DMA_UART_2_RX_VFF_ADDR UART RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	RX_VFF_ADDR	**UART memory address** Must be 8-byte aligned. Use external memory as a virtual FIFO. Internal memory is not allowed to be used as a virtual FIFO.

102173A4 AP_DMA_UART_2_RX_VFF_LEN UART RX Virtual FIFO Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:3	RX_VFF_LEN	**VFF length** Must be 8-byte aligned and longer than 32 bytes. 0: 0 byte 1: 1 byte

102173A8 AP_DMA_UART_2_RX_VFF_THRE UART RX Virtual FIFO Threshold Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_THRE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_THRE	**VFF threshold in byte alignment** In RX mode, DMA issues interrupt when data in VFF is bigger than the threshold. In TX mode, DMA issues interrupt when left size in VFF is bigger than the threshold.

102173AC **AP_DMA_UART_2_RX_VFF_WPT** **UART RX Virtual FIFO Write Pointer Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_WPT_WRAP
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_WPT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_WPT_WRAP	**RX VFF write pointer wrap bit maintained by hardware** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_WPT	**RX VFF write pointer maintained by hardware** In byte alignment.

102173B0 AP_DMA_UART_2_RX_VFF_RPT UART RX Virtual FIFO Read Pointer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RX_VFF_RPT_WRAP
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_RPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	RX_VFF_RPT_WRAP	**RX VFF read pointer wrap bit maintained by software** It is initialized to 0. When wrapped to the ring head again, invert this bit.
15:0	RX_VFF_RPT	**RX VFF read pointer maintained by software** In byte alignment.

102173B4 AP_DMA_UART_2_RX_FLOW_CTRL_THRE UART RX Virtual FIFO Flow Control Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RX_FLOW_CTRL_THRE							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RX_FLOW_CTRL_THRE	**VFF flow control threshold in byte alignment** In RX mode, DMA issues flow control when left size in VFF is smaller than the threshold.

102173B8 AP_DMA_UART_2_RX_INT_BUF_SIZE UART Rx Internal Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RX_INT_BUF_SIZE				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RX_INT_BUF_SIZE	**Virtual FIFO DMA RX internal buffer size** 0: 0 byte 1: 1 byte

102173BC **AP_DMA_UART_2_RX_VFF_VALID_SIZE** **UART Rx Virtual FIFO Valid Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_VALID_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_VALID_SIZE	**RX virtual FIFO valid size** 0: 0 byte 1: 1 byte

102173C0 **AP_DMA_UART_2_RX_VFF_LEFT_SIZE** **UART Rx Virtual FIFO Left Size Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_VFF_LEFT_SIZE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RX_VFF_LEFT_SIZE	**RX virtual FIFO left size** 0: 0 byte 1: 1 byte

102173D4 AP_DMA_UART_2_RX_VFF_ADDR2 UART RX Virtual FIFO Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RX_VFF_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RX_VFF_ADDR2	**UART memory address bit[32]**

2 Clock and Power Control

2.1 Top Clock Generator

2.1.1 Register Definition

Module name: TOPCKGEN Base address: (+0x1001B000)

Address	Name	Width	Register Function
1001B000	CLK_CFG_0	32	Function Clock Selection Register 0
1001B004	CLK_CFG_0_SET	32	SET Control of CLK_CFG_0
1001B008	CLK_CFG_0_CLR	32	CLR Control of CLK_CFG_0
1001B010	CLK_CFG_1	32	Function Clock Selection Register 1
1001B014	CLK_CFG_1_SET	32	SET Control of CLK_CFG_1
1001B018	CLK_CFG_1_CLR	32	CLR Control of CLK_CFG_1
1001B020	CLK_CFG_2	32	Function Clock Selection Register 2
1001B024	CLK_CFG_2_SET	32	SET Control of CLK_CFG_2
1001B028	CLK_CFG_2_CLR	32	CLR Control of CLK_CFG_2
1001B030	CLK_CFG_3	32	Function Clock Selection Register 3
1001B034	CLK_CFG_3_SET	32	SET Control of CLK_CFG_3
1001B038	CLK_CFG_3_CLR	32	CLR Control of CLK_CFG_3
1001B040	CLK_CFG_4	32	Function Clock Selection Register 4
1001B044	CLK_CFG_4_SET	32	SET Control of CLK_CFG_4
1001B048	CLK_CFG_4_CLR	32	CLR Control of CLK_CFG_4
1001B050	CLK_CFG_5	32	Function Clock Selection Register 5
1001B054	CLK_CFG_5_SET	32	SET Control of CLK_CFG_5
1001B058	CLK_CFG_5_CLR	32	CLR Control of CLK_CFG_5
1001B060	CLK_CFG_6	32	Function Clock Selection Register 6
1001B064	CLK_CFG_6_SET	32	SET Control of CLK_CFG_6
1001B068	CLK_CFG_6_CLR	32	CLR Control of CLK_CFG_6
1001B070	CLK_CFG_7	32	Function Clock Selection Register 7
1001B074	CLK_CFG_7_SET	32	SET Control of CLK_CFG_7
1001B078	CLK_CFG_7_CLR	32	CLR Control of CLK_CFG_7
1001B080	CLK_CFG_8	32	Function Clock Selection Register 8
1001B084	CLK_CFG_8_SET	32	SET Control of CLK_CFG_8
1001B088	CLK_CFG_8_CLR	32	CLR Control of CLK_CFG_8
1001B140	CLK_CFG_20	32	Function Clock Selection Register 20
1001B144	CLK_CFG_20_SET	32	SET Control of CLK_CFG_20
1001B148	CLK_CFG_20_CLR	32	CLR Control of CLK_CFG_20
1001B1C0	CLK_CFG_UPDATE	32	Clock Configuration Update Register
1001B1C4	CLK_CFG_UPDATE1	32	Clock Configuration Update Register
1001B200	CLK_MISC_CFG_0	32	Miscellaneous Control
1001B320	CLK26CALI_0	32	Frequency Meter Control Register 0
1001B324	CLK26CALI_1	32	Frequency Meter Control Register 1
1001B330	CKSTA_REG	32	Function Clock Selection Status Register
1001B334	CKSTA_REG1	32	Function Clock Selection Status Register
1001B420	CLK_AUDDIV_0	32	Audio Clock Selection Register

1001B000 CLK_CFG_0 Function Clock Selection Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_spim_mst			clk_spim_mst_inv		clk_spim_mst_sel			pdn_spi			clk_spi_inv		clk_spi_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_spinfi_bclk			clk_spinfi_bclk_inv		clk_spinfi_bclk_sel			pdn_nfi1x			clk_nfi1x_inv		clk_nfi1x_sel		
Type	RW			RW		RW			RW			RW		RW		
Reset	0			0		0	0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_spim_mst	**Turns off spim_mst_ck** 1: Enable clock off
28	clk_spim_mst_inv	**spim_mst_ck clock phase invert** 1: Enable phase invert
26:24	clk_spim_mst_sel	**spim_mst_ck clock mux select** 0: cb_cksq_40m 1: cb_mpll_d2 2: cb_mmpll_d4 3: net1pll_d8_d2 4: cb_net2pll_d6 5: net1pll_d5_d4 6: cb_mpll_d4 7: net1pll_d8_d4
23	pdn_spi	**Turns off spi_ck** 1: Enable clock off
20	clk_spi_inv	**spi_ck clock phase invert** 1: Enable phase invert
18:16	clk_spi_sel	**spi_ck clock mux select** 0: cb_cksq_40m 1: cb_mpll_d2 2: cb_mmpll_d4 3: net1pll_d8_d2 4: cb_net2pll_d6

Bit(s)	Name	Description
		5: net1pll_d5_d4
		6: cb_mpll_d4
		7: net1pll_d8_d4
15	pdn_spinfi_bclk	**Turns off spinfi_bclk_ck**
		1: Enable clock off
12	clk_spinfi_bclk_inv	**spinfi_bclk_ck clock phase invert**
		1: Enable phase invert
10:8	clk_spinfi_bclk_sel	**spinfi_bclk_ck clock mux select**
		0: cksq_40m_d2
		1: cb_cksq_40m
		2: net1pll_d5_d4
		3: cb_mpll_d4
		4: cb_mmpll_d8
		5: net1pll_d8_d4
		6: mmpll_d6_d2
		7: cb_mpll_d8
7	pdn_nfi1x	**Turns off nfi1x_ck**
		1: Enable clock off
4	clk_nfi1x_inv	**nfi1x_ck clock phase invert**
		1: Enable phase invert
2:0	clk_nfi1x_sel	**nfi1x_ck clock mux select**
		0: cb_cksq_40m
		1: cb_mmpll_d4
		2: net1pll_d8_d2
		3: cb_net2pll_d6
		4: cb_mpll_d4
		5: cb_mmpll_d8
		6: net1pll_d8_d4
		7: cb_mpll_d8

1001B004 **CLK_CFG_0_SET** **SET Control of CLK_CFG_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_set	**Sets the corresponding bit of CLG_CFG_SEL_0** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B008 CLK_CFG_0_CLR CLR Control of CLK_CFG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_0_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_0_clr	**Clears the corresponding bit of CLG_CFG_SEL_0** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B010 CLK_CFG_1 Function Clock Selection Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_pextp_tl_clk			clk_pextp_tl_clk_inv			clk_pextp_tl_clk_sel		pdn_i2c_bclk			clk_i2c_bclk_inv			clk_i2c_bclk_sel	
Type	RW			RW			RW		RW			RW			RW	
Reset	0			0			0	0	0			0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_pwm_bclk			clk_pwm_bclk_inv		clk_pwm_bclk_sel			pdn_uart_bclk			clk_uart_bclk_inv			clk_uart_bclk_sel	
Type	RW			RW		RW			RW			RW			RW	
Reset	0			0		0	0	0	0			0			0	0

Bit(s)	Name	Description
31	pdn_pextp_tl_clk	**Turns off pextp_tl_clk_ck** 1: Enable clock off
28	clk_pextp_tl_clk_inv	**pextp_tl_clk_ck clock phase invert** 1: Enable phase invert
25:24	clk_pextp_tl_clk_sel	**pextp_tl_clk_ck clock mux select** 0: cb_cksq_40m 1: net1pll_d5_d4 2: net2pll_d4_d2 3: cb_rtc_32k
23	pdn_i2c_bclk	**Turns off i2c_bclk_ck** 1: Enable clock off
20	clk_i2c_bclk_inv	**i2c_bclk_ck clock phase invert** 1: Enable phase invert
17:16	clk_i2c_bclk_sel	**i2c_bclk_ck clock mux select** 0: cb_cksq_40m 1: net1pll_d5_d4 2: cb_mpll_d4 3: net1pll_d8_d4
15	pdn_pwm_bclk	**Turns off pwm_bclk_ck** 1: Enable clock off
12	clk_pwm_bclk_inv	**pwm_bclk_ck clock phase invert** 1: Enable phase invert
10:8	clk_pwm_bclk_sel	**pwm_bclk_ck clock mux select**

Bit(s)	Name	Description
		0: cb_cksq_40m
		1: net1pll_d8_d2
		2: net1pll_d5_d4
		3: cb_mpll_d4
		4: mpll_d8_d2
		5: cb_rtc_32k
7	pdn_uart_bclk	**Turns off uart_bclk_ck**
		1: Enable clock off
4	clk_uart_bclk_inv	**uart_bclk_ck clock phase invert**
		1: Enable phase invert
1:0	clk_uart_bclk_sel	**uart_bclk_ck clock mux select**
		0: cb_cksq_40m
		1: cb_mpll_d8
		2: mpll_d8_d2

1001B014 **CLK_CFG_1_SET** **SET Control of CLK_CFG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_set	**Sets the corresponding bit of CLG_CFG_SEL_1** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B018 CLK_CFG_1_CLR CLR Control of CLK_CFG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_1_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_1_clr	**Clears the corresponding bit of CLG_CFG_SEL_1** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B020 CLK_CFG_2 Function Clock Selection Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_dramc_ref			clk_dramc_ref_inv				clk_dramc_ref_sel	pdn_csw_infra_f26m			clk_csw_infra_f26m_inv				clk_csw_infra_f26m_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_emmc_400m			clk_emmc_400m_inv			clk_emmc_400m_sel		pdn_emmc_208m			clk_emmc_208m_inv		clk_emmc_208m_sel		
Type	RW			RW			RW		RW			RW		RW		
Reset	0			0			0	0	0			0		0	0	0

Bit(s)	Name	Description
31	pdn_dramc_ref	**Turns off dramc_ref_ck** 1: Enable clock off
28	clk_dramc_ref_inv	**dramc_ref_ck clock phase invert** 1: Enable phase invert
24	clk_dramc_ref_sel	**dramc_ref_ck clock mux select** 0: cksq_40m_d2 1: mpll_d8_d2
23	pdn_csw_infra_f26m	**Turns off csw_infra_f26m_ck** 1: Enable clock off
20	clk_csw_infra_f26m_inv	**csw_infra_f26m_ck clock phase invert** 1: Enable phase invert
16	clk_csw_infra_f26m_sel	**csw_infra_f26m_ck clock mux select** 0: cksq_40m_d2 1: mpll_d8_d2
15	pdn_emmc_400m	**Turns off emmc_400m_ck** 1: Enable clock off
12	clk_emmc_400m_inv	**emmc_400m_ck clock phase invert** 1: Enable phase invert
9:8	clk_emmc_400m_sel	**emmc_400m_ck clock mux select** 0: cb_cksq_40m 1: cb_net2pll_d2 2: cb_mmpll_d2

Bit(s)	Name	Description
		3: cb_net2pll_d4
7	pdn_emmc_208m	**Turns off emmc_208m_ck**
		1: Enable clock off
4	clk_emmc_208m_inv	**emmc_208m_ck clock phase invert**
		1: Enable phase invert
2:0	clk_emmc_208m_sel	**emmc_208m_ck clock mux select**
		0: cb_cksq_40m
		1: cb_mpll_d2
		2: cb_net2pll_d4
		3: cb_apll2_196m
		4: cb_mmpll_d4
		5: net1pll_d8_d2
		6: cb_mmpll_d6

1001B024 CLK_CFG_2_SET SET Control of CLK_CFG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_set	**Sets the corresponding bit of CLG_CFG_SEL_2** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B028 CLK_CFG_2_CLR CLR Control of CLK_CFG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_2_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_2_clr	**Clears the corresponding bit of CLG_CFG_SEL_2** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B030 CLK_CFG_3 Function Clock Selection Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_arm_debugtop_main			clk_arm_debugtop_main_inv				clk_arm_debugtop_main_sel	pdn_sysapb			clk_sysapb_inv				clk_sysapb_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_sysaxi			clk_sysaxi_inv				clk_sysaxi_sel	pdn_pwr_dramc_md32			clk_pwr_dramc_md32_inv			clk_pwr_dramc_md32_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_arm_debugtop_main	**Turns off arm_debugtop_main_ck** 1: Enable clock off
28	clk_arm_debugtop_main_inv	**arm_debugtop_main_ck clock phase invert** 1: Enable phase invert
24	clk_arm_debugtop_main_sel	**arm_debugtop_main_ck clock mux select** 0: cb_cksq_40m 1: cb_net2pll_d6
23	pdn_sysapb	**Turns off sysapb_ck** 1: Enable clock off
20	clk_sysapb_inv	**sysapb_ck clock phase invert** 1: Enable phase invert
16	clk_sysapb_sel	**sysapb_ck clock mux select** 0: cb_cksq_40m 1: mpll_d3_d2
15	pdn_sysaxi	**Turns off sysaxi_ck** 1: Enable clock off
12	clk_sysaxi_inv	**sysaxi_ck clock phase invert** 1: Enable phase invert
8	clk_sysaxi_sel	**sysaxi_ck clock mux select** 0: cb_cksq_40m 1: net1pll_d8_d2

Bit(s)	Name	Description
7	pdn_pwr_dramc_md32	**Turns off pwr_dramc_md32_ck** 1: Enable clock off
4	clk_pwr_dramc_md32_inv	**pwr_dramc_md32_ck clock phase invert** 1: Enable phase invert
1:0	clk_pwr_dramc_md32_sel	**pwr_dramc_md32_ck clock mux select** 0: cb_cksq_40m 1: cb_mpll_d2 2: cb_wedmcupll_208m

1001B034 CLK_CFG_3_SET SET Control of CLK_CFG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_set	**Sets the corresponding bit of CLG_CFG_SEL_3** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B038 CLK_CFG_3_CLR CLR Control of CLK_CFG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_3_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_3_clr	**Clears the corresponding bit of CLG_CFG_SEL_3** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B040 CLK_CFG_4 Function Clock Selection Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_netsys_wed_mcu			clk_netsys_wed_mcu_inv		clk_netsys_wed_mcu_sel			pdn_netsys_500m			clk_netsys_500m_inv				clk_netsys_500m_sel
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_netsys			clk_netsys_inv				clk_netsys_sel	pdn_ap2conn_host			clk_ap2conn_host_inv				clk_ap2conn_host_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_netsys_wed_mcu	**Turns off netsys_wed_mcu_ck** 1: Enable clock off
28	clk_netsys_wed_mcu_inv	**netsys_wed_mcu_ck clock phase invert** 1: Enable phase invert
26:24	clk_netsys_wed_mcu_sel	**netsys_wed_mcu_ck clock mux select** 0: cb_cksq_40m 1: cb_mmpll_720m 2: cb_net1pll_d4 3: cb_net1pll_d5 4: cb_mpll_416m
23	pdn_netsys_500m	**Turns off netsys_500m_ck** 1: Enable clock off
20	clk_netsys_500m_inv	**netsys_500m_ck clock phase invert** 1: Enable phase invert
16	clk_netsys_500m_sel	**netsys_500m_ck clock mux select** 0: cb_cksq_40m 1: cb_net1pll_d5
15	pdn_netsys	**Turns off netsys_ck** 1: Enable clock off
12	clk_netsys_inv	**netsys_ck clock phase invert** 1: Enable phase invert
8	clk_netsys_sel	**netsys_ck clock mux select**

Bit(s)	Name	Description
		0: cb_cksq_40m
		1: cb_mmpll_d2
7	pdn_ap2conn_host	**Turns off ap2conn_host_ck**
		1: Enable clock off
4	clk_ap2conn_host_inv	**ap2conn_host_ck clock phase invert**
		1: Enable phase invert
0	clk_ap2conn_host_sel	**ap2conn_host_ck clock mux select**
		0: cb_cksq_40m
		1: net1pll_d8_d4

1001B044 CLK_CFG_4_SET SET Control of CLK_CFG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_set	**Sets the corresponding bit of CLG_CFG_SEL_4** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B048 CLK_CFG_4_CLR CLR Control of CLK_CFG_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_4_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_4_clr	**Clears the corresponding bit of CLG_CFG_SEL_4** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B050 CLK_CFG_5 Function Clock Selection Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_eip97b			clk_eip97b_inv		clk_eip97b_sel			pdn_sgmii_reg			clk_sgmii_reg_inv				clk_sgmii_reg_sel
Type	RW			RW		RW			RW			RW				RW
Reset	0			0		0	0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_sgmii_ref_325m			clk_sgmii_ref_325m_inv				clk_sgmii_ref_325m_sel	pdn_netsys_2x			clk_netsys_2x_inv			clk_netsys_2x_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_eip97b	**Turns off eip97b_ck** 1: Enable clock off
28	clk_eip97b_inv	**eip97b_ck clock phase invert** 1: Enable phase invert
26:24	clk_eip97b_sel	**eip97b_ck clock mux select** 0: cb_cksq_40m 1: cb_net1pll_d5 2: cb_mpll_416m 3: cb_mmpll_d2 4: net1pll_d5_d2
23	pdn_sgmii_reg	**Turns off sgmii_reg_ck** 1: Enable clock off
20	clk_sgmii_reg_inv	**sgmii_reg_ck clock phase invert** 1: Enable phase invert
16	clk_sgmii_reg_sel	**sgmii_reg_ck clock mux select** 0: cb_cksq_40m 1: cb_net2pll_d4
15	pdn_sgmii_ref_325m	**Turns off sgmii_ref_325m_ck** 1: Enable clock off
12	clk_sgmii_ref_325m_inv	**sgmii_ref_325m_ck clock phase invert** 1: Enable phase invert
8	clk_sgmii_ref_325m_sel	**sgmii_ref_325m_ck clock mux select**

Bit(s)	Name	Description
		0: cb_cksq_40m
		1: cb_sgmiipll_325m
7	pdn_netsys_2x	**Turns off netsys_2x_ck**
		1: Enable clock off
4	clk_netsys_2x_inv	**netsys_2x_ck clock phase invert**
		1: Enable phase invert
1:0	clk_netsys_2x_sel	**netsys_2x_ck clock mux select**
		0: cb_cksq_40m
		1: cb_net2pll_800m
		2: cb_mmpll_720m

1001B054 CLK_CFG_5_SET SET Control of CLK_CFG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_set	**Sets the corresponding bit of CLG_CFG_SEL_5** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B058 CLK_CFG_5_CLR CLR Control of CLK_CFG_5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_5_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_5_clr	**Clears the corresponding bit of CLG_CFG_SEL_5** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B060 CLK_CFG_6 Function Clock Selection Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_aud_intbus			clk_aud_intbus_inv			clk_aud_intbus_sel		pdn_a1sys			clk_a1sys_inv				clk_a1sys_sel
Type	RW			RW			RW		RW			RW				RW
Reset	0			0			0	0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_aud			clk_aud_inv				clk_aud_sel	pdn_usb3_dphy_ref			clk_usb3_dphy_ref_inv				clk_usb3_dphy_ref_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0

Bit(s)	Name	Description
31	pdn_aud_intbus	**Turns off aud_intbus_ck** 1: Enable clock off
28	clk_aud_intbus_inv	**aud_intbus_ck clock phase invert** 1: Enable phase invert
25:24	clk_aud_intbus_sel	**aud_intbus_ck clock mux select** 0: cb_cksq_40m 1: cb_apll2_196m 2: mpll_d8_d2
23	pdn_a1sys	**Turns off a1sys_ck** 1: Enable clock off
20	clk_a1sys_inv	**a1sys_ck clock phase invert** 1: Enable phase invert
16	clk_a1sys_sel	**a1sys_ck clock mux select** 0: cb_cksq_40m 1: apll2_d4
15	pdn_aud	**Turns off aud_ck** 1: Enable clock off
12	clk_aud_inv	**aud_ck clock phase invert** 1: Enable phase invert
8	clk_aud_sel	**aud_ck clock mux select** 0: cb_cksq_40m 1: cb_apll2_196m
7	pdn_usb3_dphy_ref	**Turns off usb3_dphy_ref_ck**

Bit(s)	Name	Description
		1: Enable clock off
4	clk_usb3_dphy_ref_inv	**usb3_dphy_ref_ck clock phase invert** 1: Enable phase invert
0	clk_usb3_dphy_ref_sel	**usb3_dphy_ref_ck clock mux select** 0: cksq_40m_d2 1: mpll_d8_d2

1001B064 CLK_CFG_6_SET SET Control of CLK_CFG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_set	**Sets the corresponding bit of CLG_CFG_SEL_6** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B068 CLK_CFG_6_CLR CLR Control of CLK_CFG_6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_6_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_6_clr	**Clears the corresponding bit of CLG_CFG_SEL_6** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B070 **CLK_CFG_7** **Function Clock Selection Register 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	pdn_u2u3_xhci			clk_u2u3_xhci_inv				clk_u2u3_xhci_sel	pdn_u2u3_sys			clk_u2u3_sys_inv				clk_u2u3_sys_sel
Type	RW			RW				RW	RW			RW				RW
Reset	0			0				0	0			0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pdn_u2u3_ref			clk_u2u3_ref_inv				clk_u2u3_ref_sel	pdn_apll_tuner			clk_apll_tuner_inv			clk_apll_tuner_sel	
Type	RW			RW				RW	RW			RW			RW	
Reset	0			0				0	0			0			0	0

Bit(s)	Name	Description
31	pdn_u2u3_xhci	**Turns off u2u3_xhci_ck** 1: Enable clock off
28	clk_u2u3_xhci_inv	**u2u3_xhci_ck clock phase invert** 1: Enable phase invert
24	clk_u2u3_xhci_sel	**u2u3_xhci_ck clock mux select** 0: cb_cksq_40m 1: net1pll_d5_d4
23	pdn_u2u3_sys	**Turns off u2u3_sys_ck** 1: Enable clock off
20	clk_u2u3_sys_inv	**u2u3_sys_ck clock phase invert** 1: Enable phase invert
16	clk_u2u3_sys_sel	**u2u3_sys_ck clock mux select** 0: cb_cksq_40m 1: net1pll_d5_d4
15	pdn_u2u3_ref	**Turns off u2u3_ref_ck** 1: Enable clock off
12	clk_u2u3_ref_inv	**u2u3_ref_ck clock phase invert** 1: Enable phase invert
8	clk_u2u3_ref_sel	**u2u3_ref_ck clock mux select** 0: cb_cksq_40m 1: mpll_d8_d2
7	pdn_apll_tuner	**Turns off apll_tuner_ck** 1: Enable clock off

Bit(s)	Name	Description
4	clk_apll_tuner_inv	**apll_tuner_ck clock phase invert** 1: Enable phase invert
1:0	clk_apll_tuner_sel	**apll_tuner_ck clock mux select** 0: cb_cksq_40m 1: apll2_d4 2: mpll_d8_d2

1001B074 **CLK_CFG_7_SET** **SET Control of CLK_CFG_7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_set	**Sets the corresponding bit of CLG_CFG_SEL_7** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B078 CLK_CFG_7_CLR CLR Control of CLK_CFG_7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_7_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_7_clr	**Clears the corresponding bit of CLG_CFG_SEL_7** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B080 CLK_CFG_8 Function Clock Selection Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									pdn_ssusb_frmcnt			clk_ssusb_frmcnt_inv				clk_ssusb_frmcnt_sel
Type									RW			RW				RW
Reset									0			0				0

Bit(s)	Name	Description
7	pdn_ssusb_frmcnt	**Turns off ssusb_frmcnt_ck** 1: Enable clock off
4	clk_ssusb_frmcnt_inv	**ssusb_frmcnt_ck clock phase invert** 1: Enable phase invert
0	clk_ssusb_frmcnt_sel	**ssusb_frmcnt_ck clock mux select** 0: cb_cksq_40m 1: cb_mmpll_d3_d5

1001B084 CLK_CFG_8_SET SET Control of CLK_CFG_8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_8_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_8_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_8_set	**Sets the corresponding bit of CLG_CFG_SEL_8** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B088 CLK_CFG_8_CLR CLR Control of CLK_CFG_8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_8_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_8_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_8_clr	**Clears the corresponding bit of CLG_CFG_SEL_8** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B140 CLK_CFG_20 Function Clock Selection Register 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																en_spm2cksys_mem_ck_mux_update
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
16	en_spm2cksys_mem_ck_mux_update	**en_spm2cksys_mem_ck_mux_update** 1: Enable

1001B144 CLK_CFG_20_SET SET Control of CLK_CFG_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_20_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_20_set															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_20_set	**Sets the corresponding bit of CLG_CFG_SEL_11** 0: Unchanged 1: Set 1'b1 to the corresponding bit

1001B148 CLK_CFG_20_CLR CLR Control of CLK_CFG_20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	clk_cfg_20_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	clk_cfg_20_clr															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	clk_cfg_20_clr	**Clears the corresponding bit of CLG_CFG_SEL_11** 0: Unchanged 1: Set 1'b0 to the corresponding bit

1001B1C0 CLK_CFG_UPDATE Clock Configuration Update Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		u2u3_sys_ck_update	u2u3_ref_ck_update	apll_tuner_ck_update	aud_intbus_ck_update	a1sys_ck_update	aud_ck_update	usb3_dphy_ref_ck_update	eip97b_ck_update	sgmii_reg_ck_update	sgmii_ref_325m_ck_update	netsys_2x_ck_update	netsys_wedmcu_ck_update	netsys_500m_ck_update	netsys_bus_ck_update	ap2conn_host_ck_update
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	arm_debugtop_main_ck_update	sysapb_ck_update	sysaxi_ck_update	pwr_dramc_md32_ck_update	dramc_ref_ck_update	csw_infra_f26m_ck_update	emmc_400m_ck_update	emmc_208m_ck_update	pextp_tl_clk_ck_update	i2c_bclk_ck_update	pwm_bclk_ck_update	uart_bclk_ck_update	spim_mst_ck_update	spi_ck_update	spinfi_ck_update	nfi1x_ck_update
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	u2u3_sys_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update u2u3_sys_clkmux
29	u2u3_ref_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update u2u3_ref_clkmux
28	apll_tuner_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update apll_tuner_clkmux
27	aud_intbus_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update aud_intbus_clkmux
26	a1sys_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update a1sys_clkmux
25	aud_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update aud_clkmux
24	usb3_dphy_ref_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update usb3_dphy_ref_clkmux
23	eip97b_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update eip97b_clkmux
22	sgmii_reg_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update sgmii_reg_clkmux
21	sgmii_ref_325m_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update sgmii_ref_325m_clkmux
20	netsys_2x_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update netsys_2x_clkmux

Bit(s)	Name	Description
19	netsys_wedmcu_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update netsys_wedmcu_clkmux
18	netsys_500m_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update netsys_500m_clkmux
17	netsys_bus_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update netsys_bus_clkmux
16	ap2conn_host_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update ap2conn_host_clkmux
15	arm_debugtop_main_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update arm_debugtop_main_clkmux
14	sysapb_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update sysapb_clkmux
13	sysaxi_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update sysaxi_clkmux
12	pwr_dramc_md32_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update pwr_dramc_md32_clkmux
11	dramc_ref_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update dramc_ref_clkmux
10	csw_infra_f26m_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update csw_infra_f26m_clkmux
9	emmc_400m_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update emmc_400m_clkmux
8	emmc_208m_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update emmc_208m_clkmux
7	pextp_tl_clk_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update pextp_tl_clk_clkmux
6	i2c_bclk_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update i2c_bclk_clkmux
5	pwm_bclk_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update pwm_bclk_clkmux
4	uart_bclk_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update uart_bclk_clkmux

Bit(s)	Name	Description
3	spim_mst_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update spim_mst_clkmux
2	spi_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update spi_clkmux
1	spinfi_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update spinfi_clkmux
0	nfi1x_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update nfi1x_clkmux

1001B1C4 CLK_CFG_UPDATE1 Clock Configuration Update Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ssusb_frmcnt_ck_update	u2u3_xhci_ck_update
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	ssusb_frmcnt_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update usu3_frmcnt_clkmux
0	u2u3_xhci_ck_update	**Write 1 to update the change for clk_sel and clk_inv** 1: Update u2u3_xhci_clkmux

1001B200 **CLK_MISC_CFG_0** **Miscellaneous Control** **FF00FF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ckgen_k1															
Type	RW															
Reset	1	1	1	1	1	1	1	1								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:24	ckgen_k1	**Frequency meter divider configuration**

1001B320 CLK26CALI_0 Frequency Meter Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**fmeter_en**				**ckgen_clk_exc**				**ckgen_tri_cal**
Type								RW				RW				RW
Reset								0				0				0

Bit(s)	Name	Description
8	fmeter_en	0: Disable fmeter 1: Enable fmeter
4	ckgen_clk_exc	**Selects measure clock** 0: f_fckgen_ck 1: CLK26M
0	ckgen_tri_cal	**Triggers frequency meter on f_fckgen_ck** Auto-cleared when calibration is done. 0: Disable 1: Enable

1001B324 **CLK26CALI_1** **Frequency Meter Control Register 1** **3FF00000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			ckgen_load_cnt										cal_target_offset			
Type			RW										RW			
Reset			1	1	1	1	1	1	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cal_target_value															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:20	ckgen_load_cnt	**clock_sync period ('h27 =>1us, 'h18f=>10us)**
19:16	cal_target_offset	**Target value offset of frequency meter result**
15:0	cal_target_value	**Target value of frequency meter result**

1001B330 CKSTA_REG Function Clock Selection Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		u2u3_sys_ck_change	u2u3_ref_ck_change	apll_tuner_ck_change	aud_intbus_ck_change	a1sys_ck_change	aud_ck_change	usb3_dphy_ref_ck_change	eip97b_ck_change	sgmii_reg_ck_change	sgmii_ref_325m_ck_change	netsys_2x_ck_change	netsys_wedmcu_ck_change	netsys_500m_ck_change	netsys_bus_ck_change	ap2conn_host_ck_change
Type		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	arm_debugtop_main_ck_change	sysapb_ck_change	sysaxi_ck_change	pwr_dramc_md32_ck_change	dramc_ref_ck_change	csw_infra_f26m_ck_change	emmc_400m_ck_change	emmc_208m_ck_change	pextp_tl_clk_ck_change	i2c_bclk_ck_change	pwm_bclk_ck_change	uart_bclk_ck_change	spim_mst_ck_change	spi_ck_change	spinfi_ck_change	nfi1x_ck_change
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	u2u3_sys_ck_change	**Clock switch status** 1: Clock switch is in progress
29	u2u3_ref_ck_change	**Clock switch status** 1: Clock switch is in progress
28	apll_tuner_ck_change	**Clock switch status** 1: Clock switch is in progress
27	aud_intbus_ck_change	**Clock switch status** 1: Clock switch is in progress
26	a1sys_ck_change	**Clock switch status** 1: Clock switch is in progress
25	aud_ck_change	**Clock switch status** 1: Clock switch is in progress
24	usb3_dphy_ref_ck_change	**Clock switch status** 1: Clock switch is in progress
23	eip97b_ck_change	**Clock switch status** 1: Clock switch is in progress
22	sgmii_reg_ck_change	**Clock switch status** 1: Clock switch is in progress
21	sgmii_ref_325m_ck_change	**Clock switch status** 1: Clock switch is in progress
20	netsys_2x_ck_change	**Clock switch status** 1: Clock switch is in progress

Bit(s)	Name	Description
19	netsys_wedmcu_ck_change	**Clock switch status** 1: Clock switch is in progress
18	netsys_500m_ck_change	**Clock switch status** 1: Clock switch is in progress
17	netsys_bus_ck_change	**Clock switch status** 1: Clock switch is in progress
16	ap2conn_host_ck_change	**Clock switch status** 1: Clock switch is in progress
15	arm_debugtop_main_ck_change	**Clock switch status** 1: Clock switch is in progress
14	sysapb_ck_change	**Clock switch status** 1: Clock switch is in progress
13	sysaxi_ck_change	**Clock switch status** 1: Clock switch is in progress
12	pwr_dramc_md32_ck_change	**Clock switch status** 1: Clock switch is in progress
11	dramc_ref_ck_change	**Clock switch status** 1: Clock switch is in progress
10	csw_infra_f26m_ck_change	**Clock switch status** 1: Clock switch is in progress
9	emmc_400m_ck_change	**Clock switch status** 1: Clock switch is in progress
8	emmc_208m_ck_change	**Clock switch status** 1: Clock switch is in progress
7	pextp_tl_clk_ck_change	**Clock switch status** 1: Clock switch is in progress
6	i2c_bclk_ck_change	**Clock switch status** 1: Clock switch is in progress
5	pwm_bclk_ck_change	**Clock switch status** 1: Clock switch is in progress
4	uart_bclk_ck_change	**Clock switch status** 1: Clock switch is in progress

Bit(s)	Name	Description
3	spim_mst_ck_change	**Clock switch status** 1: Clock switch is in progress
2	spi_ck_change	**Clock switch status** 1: Clock switch is in progress
1	spinfi_ck_change	**Clock switch status** 1: Clock switch is in progress
0	nfi1x_ck_change	**Clock switch status** 1: Clock switch is in progress

1001B334 CKSTA_REG1 Function Clock Selection Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ssusb_frmcnt_ck_change	u2u3_xhci_ck_change
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
1	ssusb_frmcnt_ck_change	**Clock switch status** 1: Clock switch is in progress
0	u2u3_xhci_ck_change	**Clock switch status** 1: Clock switch is in progress

1001B420 CLK_AUDDIV_0 Audio Clock Selection Register 00000701

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	apll12_ck_div_pcm											apll12_div_pcm_inv				apll12_div_pcm_pdn
Type	RW											RW				RW
Reset	0	0	0	0	0	1	1	1				0				1

Bit(s)	Name	Description
15:8	apll12_ck_div_pcm	**Divider setting of f_faud_pcm_m_ck, n = [7:0]** f_faud_pcm_m_ck = clock source*[1/(n + 1)]
4	apll12_div_pcm_inv	**Inverts f_faud_pcm_m_ck clock phase** 1: Enable phase inversion
0	apll12_div_pcm_pdn	**Powers down apll12_div_pcm divider** 1: Enable power down

2.2 TOP Reset Generator Unit

2.2.1 Register Definition

Module name: TOPRGU Base address: (+0x1001C000)

Address	Name	Width	Register Function
1001C000	WDT_MODE	32	Watchdog Mode Register
1001C004	WDT_LENGTH	32	Watchdog Counter Setting Register
1001C008	WDT_RESTART	32	Watchdog Counter Restart Register
1001C00C	WDT_STA	32	Watchdog Status Register
1001C010	WDT_INTERVAL	32	Watchdog Reset Pulse Width Register
1001C014	WDT_SWRST	32	Software Watchdog Reset Register
1001C018	WDT_SWSYSRST	32	System Software Reset Register
1001C030	WDT_REQ_MODE	32	Reset Request Mode Register
1001C034	WDT_REQ_IRQ_EN	32	Reset Request IRQ Enable Register
1001C050	WDT_INTERCORE_SYNC	32	Intercore Sync Register
1001C054	WDT_INTERCORE_SYNC_SET	32	Set Control of Intercore Sync Register
1001C058	WDT_INTERCORE_SYNC_CLR	32	Clear Control of Intercore Sync Register
1001C060	STRAP_PAR	32	Parallel HW Trap
1001C080	WDT_DEBUG_CTL3	32	Debug System Control Register
1001C0A4	WDT_PWR_LATCH	32	sw_bootup_ready
1001C500	DEBUG_0_REG	32	Shadow Register of WDT_MODE
1001C504	DEBUG_1_REG	32	Shadow Register of WDT_STA
1001C50C	DEBUG_3_REG	32	Shadow Register of WDT_REQ_MODE
1001C510	DEBUG_4_REG	32	Shadow Register of WDT_REG_IRQ_EN
1001C514	DEBUG_5_REG	32	Shadow Register of WDT_DEBUG_CTL3
1001C518	DEBUG_6_REG	32	Watchdog Counter
1001C580	WDT_EAP_TIMER	32	TOPRGU WDT_DEBUG(LATCH)_CTL_2 Timeout Value

1001C000 WDT_MODE Watchdog Mode Register 0000004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								wdt_cnt_reset_sel		dual_mode	irq_lvl_en		wdt_irq	exten	extpol	wdt_en
Type								RW		RW	RW		RW	RW	RW	RW
Reset								0		1	0		1	1	0	1

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x22 to unlock the write protection of this register**
8	wdt_cnt_reset_sel	**Selects reset source of watchdog timer** 0: Reset only by external reset 1: Reset by TOPRGU
6	dual_mode	**Enables dual_mode** Turns on watchdog timer and enables the corresponding irq_en and wdt_en if dual_mode is used 0: Disable 1: Enable
5	irq_lvl_en	**Selects IRQ type** 0: Edge (32K) 1: Level
3	wdt_irq	**Enables watchdog timer IRQ** 0: Trigger reset 1: Trigger IRQ
2	exten	**Enables watchdog output reset signal** 0: Disable 1: Enable
1	extpol	**Watchdog output reset signal polarity** 0: Active low 1: Active high
0	wdt_en	**Enables watchdog timer** 0: Disable 1: Enable

Bit(s)	Name	Description

1001C004 WDT_LENGTH Watchdog Counter Setting Register 0000FFE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_length											unlock_key				
Type	RW											WO				
Reset	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
15:5	wdt_length	**Watchdog time-out counter setting** The counter is restarted with {wdt_length [10:0], 1_1111_1111b}, and therefore the watchdog timer time-out period is a multiple of 512*T32k = 15.6ms
4:0	unlock_key	**Write 0x8 to unlock the write protection of this register**

1001C008 WDT_RESTART Watchdog Counter Restart Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wdt_restart															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	wdt_restart	**Write 0x1971 to reset the watchdog time-out counter**

1001C00C WDT_STA Watchdog Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	hw_wdt_rst	sw_wdt_rst	irq_assert	security_rst									debug_rst	thermal_ctl_rst		
Type	RO	RO	RO	RO									RO	RO		
Reset	0	0	0	0									0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_rst	spm_thermal_rst
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	hw_wdt_rst	**Indicates hardware watchdog generated reset is asserted**
30	sw_wdt_rst	**Indicates software watchdog generated reset is asserted**
29	irq_assert	**Indicates IRQ is asserted instead of reset**
28	security_rst	**Indicates security reset is asserted**
19	debug_rst	**Indicates debug generated reset is asserted**
18	thermal_ctl_rst	**Indicates thermal reset generated by thermal controller is asserted**
1	spm_rst	**Indicates scpsys time-out generated reset is asserted**
0	spm_thermal_rst	**Indicates thermal reset generated by scpsys reset is asserted**

1001C010 WDT_INTERVAL Watchdog Reset Pulse Width Register 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**wdt_reset_interval**											
Type					RW											
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11:0	wdt_reset_interval	**Resets pulse width generated by watchdog** 2T 32K duration is required for TD modem. Unit: 1T = 1 x 32 kHz

1001C014 WDT_SWRST Software Watchdog Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unlock_key															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	unlock_key	**Write 0x1209 to generate a software watchdog reset**

1001C018 WDT_SWSYSRST System Software Reset Register 00F00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key								consys_rst	RESV_bits			efuse_grst_b			
Type	WO								RW	RW			RW			
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							gephy_grst_b	ethdma_grst_b	ssusb_grst_b	pcie_grst_b	u2phy_grst_b	RESV0_bit	infra_grst_b	sgmii1_grst_b	sgmii0_grst_b	apmixedsys_grst_b
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x88 to unlock the write protection of this register**
23	consys_rst	**Write 1 to reset CONNSYS**
22:20	RESV_bits	**Reserved**
19	efuse_grst_b	**Write 1 to reset eFuse**
9	gephy_grst_b	**Write 1 to reset gephy**
8	ethdma_grst_b	**Write 1 to reset ethdma**
7	ssusb_grst_b	**Write 1 to reset SSUSB**
6	pcie_grst_b	**Write 1 to reset PCIe**
5	u2phy_grst_b	**Write 1 to reset u2phy**
4	RESV0_bit	**Reserved**
3	infra_grst_b	**Write 1 to reset infra**
2	sgmii1_grst_b	**Write 1 to reset sgmii1**
1	sgmii0_grst_b	**Write 1 to reset sgmii0**
0	apmixedsys_grst_b	**Write 1 to reset apmixedsys**

1001C030 WDT_REQ_MODE Reset Request Mode Register 000C0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												debug_en			
Type	WO												RW			
Reset	0	0	0	0	0	0	0	0					1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															spm_en	
Type															RW	
Reset															1	

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x33 to unlock the write protection of this register**
19	debug_en	**Enables debugsys reset** 0: Disable 1: Enable
1	spm_en	**Enables scpsys reset** 0: Disable 1: Enable

1001C034 WDT_REQ_IRQ_EN Reset Request IRQ Enable Register 000C0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key												debug_irq			
Type	WO												RW			
Reset	0	0	0	0	0	0	0	0					1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															scpsys_irq	
Type															RW	
Reset															1	

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x44 to unlock the write protection of this register**
19	debug_irq	**Triggers IRQ instead of reset when debugsys reset is enabled** 0: Trigger reset 1: Trigger IRQ
1	scpsys_irq	**Triggers IRQ instead of reset when scpsys reset is enabled** 0: Trigger reset 1: Trigger IRQ

1001C050 WDT_INTERCORE_SYNC Intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync	**Register for using intercore sync**

1001C054 WDT_INTERCORE_SYNC_SET Set Control of Intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_set															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_set															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_set	**Sets 1'b1 to the corresponding bit of rg_intercore_sync**

1001C058 WDT_INTERCORE_SYNC_CLR Clear Control of Intercore Sync Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_intercore_sync_clr															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	rg_intercore_sync_clr	**Sets 1'b0 to the corresponding bit of rg_intercore_sync**

1001C060 STRAP_PAR Parallel HW Trap 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV															testmode
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:1	RESV	**Reserved**
0	testmode	**PAD_TESTMODE Value** 0: Default 1: PAD_TESTMODE is set

1001C080 WDT_DEBUG_CTL3 Debug System Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key										debugsys_wdt_ack_32k					debugsys_success
Type	WO										RO					RW
Reset	0	0	0	0	0	0	0	0			0					0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	debugsys_req	debugsys_thermal_req														
Type	RW	RW														
Reset	0	0														

Bit(s)	Name	Description
31:24	unlock_key	**Write 0x51 to unlock the write protection of this register**
21	debugsys_wdt_ack_32k	**ACK from DDR reserve mode module**
16	debugsys_success	**Write address 0x0 && Write data 0x23000100 to clear this bit**
15	debugsys_req	**Request to DDR reserve mode module in normal**
14	debugsys_thermal_req	**Request to DDR reserve mode module**

1001C0A4 WDT_PWR_LATCH sw_bootup_ready 66000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	unlock_key															
Type	WO															
Reset	0	1	1	0	0	1	1	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																sw_bootup_ready
Type																RW
Reset																0

Bit(s)	Name	Description
31:24	unlock_key	**Writes 0x66 to unlock the write protection of this register**
0	sw_bootup_ready	**Informs PMIC if system is ready during bootup on ROM stage** 0: System is not ready on ROM stage. 1: System is ready on ROM stage.

1001C500 DEBUG_0_REG Shadow Register of WDT_MODE 0000004D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								shadow_wdt_cnt_reset_sel		shadow_dual_mode	shadow_irq_lvl_en	shadow_wdt_restart_dummy_en	shadow_wdt_irq	shadow_exten	shadow_extpol	shadow_wdt_en
Type								RO		RO	RO	RO	RO	RO	RO	RO
Reset								0		1	0	0	1	1	0	1

Bit(s)	Name	Description
8	shadow_wdt_cnt_reset_sel	**Shadow wdt_cnt_reset_sel**
6	shadow_dual_mode	**Shadow dual_mode**
5	shadow_irq_lvl_en	**Shadow irq_lvl_en**
4	shadow_wdt_restart_dummy_en	**Shadow wdt_restart_dummy_en**
3	shadow_wdt_irq	**Shadow wdt_irq**
2	shadow_exten	**Shadow exten**
1	shadow_extpol	**Shadow extpol**
0	shadow_wdt_en	**Shadow wdt_en**

1001C504 **DEBUG_1_REG** **Shadow Register of WDT_STA** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	shadow_hw_wdt_rst	shadow_sw_wdt_rst	shadow_irq_assert	shadow_security_rst									shadow_debug_rst	shadow_thermal_ctl_rst		
Type	RO	RO	RO	RO									RO	RO		
Reset	0	0	0	0									0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_spm_wdt_rst	shadow_thermal_rst
Type															RO	RO
Reset															0	0

Bit(s)	Name	Description
31	shadow_hw_wdt_rst	**Shadow hw_wdt_rst**
30	shadow_sw_wdt_rst	**Shadow sw_wdt_rst**
29	shadow_irq_assert	**Shadow irq_assert**
28	shadow_security_rst	**Shadow security_rst**
19	shadow_debug_rst	**Shadow debug_rst**
18	shadow_thermal_ctl_rst	**Shadow thermal_ctl_rst**
1	shadow_spm_wdt_rst	**Shadow spm_wdt_rst**
0	shadow_thermal_rst	**Shadow thermal_rst**

1001C50C **DEBUG_3_REG** **Shadow Register of WDT_REQ_MODE** **003C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													shadow_debug_en	shadow_thermal_ctl_en		
Type													RO	RO		
Reset													1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_en	shadow_thermal_en
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
19	shadow_debug_en	**Shadow debug_en**
18	shadow_thermal_ctl_en	**Shadow thermal_ctl_en**
1	shadow_scpsys_en	**Shadow scpsys_en**
0	shadow_thermal_en	**Shadow thermal_en**

1001C510 **DEBUG_4_REG** **Shadow Register of WDT_REG_IRQ_EN** **000C0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													shadow_debug_irq	shadow_thermal_ctl_irq		
Type													RO	RO		
Reset													1	1		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															shadow_scpsys_irq	shadow_thermal_irq
Type															RO	RO
Reset															1	1

Bit(s)	Name	Description
19	shadow_debug_irq	**Shadow debug_irq**
18	shadow_thermal_ctl_irq	**Shadow thermal_ctl_irq**
1	shadow_scpsys_irq	**Shadow scpsys_irq**
0	shadow_thermal_irq	**Shadow thermal_irq**

1001C514 **DEBUG_5_REG** **Shadow Register of WDT_DEBUG_CTL3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											shadow_debugsys_wdt_ack_32k					shadow_debugsys_success
Type											RO					RO
Reset											0					0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	shadow_debugsys_req	shadow_debugsys_thermal_req														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
21	shadow_debugsys_wdt_ack_32k	**Shadow debugsys_wdt_ack_32k**
16	shadow_debugsys_success	**Shadow debugsys_success**
15	shadow_debugsys_req	**Shadow debugsys_req**
14	shadow_debugsys_thermal_req	**Shadow debugsys_thermal_req**

1001C518 DEBUG_6_REG Watchdog Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**sw_boot_rdy_status**
Type																RO
Reset																0

Bit(s)	Name	Description
0	sw_boot_rdy_status	**Software boot ready status**

1001C580 WDT_EAP_TIMER TOPRGU WDT_DEBUG(LATCH)_CTL_2 Timeout Value 0000010F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																rg_eap_timer
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_eap_timer															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1

Bit(s)	Name	Description
16:0	rg_eap_timer	**EAP timer**

2.3 AP Mixedsys

2.3.1 Register Definition

Module name: APMIXEDSYS Base address: (+0x1001E000)

Address	Name	Width	Register Function
1001E000	AP_PLL_CON0	32	AP PLL Control Register 0
1001E004	AP_PLL_CON1	32	AP PLL Control Register 1
1001E008	AP_PLL_CON2	32	AP PLL Control Register 2
1001E00C	AP_PLL_CON3	32	AP PLL Control Register 3
1001E010	AP_PLL_CON4	32	AP PLL Control Register 4
1001E014	AP_PLL_CON5	32	AP PLL Control Register 5
1001E018	AP_PLL_CON6	32	AP PLL Control Register 6
1001E040	PLL_TEST_CON0	32	PLL Test Control Register 0
1001E044	PLL_TEST_CON1	32	PLL Test Control Register 1
1001E048	PLL_TEST_CON2	32	PLL Test Control Register 2
1001E200	ARMPLL_CON0	32	ARMPLL Control Register 0
1001E204	ARMPLL_CON1	32	ARMPLL Control Register 1
1001E20C	ARMPLL_PWR_CON0	32	ARMPLL Power Control Register 0
1001E210	NET2PLL_CON0	32	NET2PLL Control Register 0
1001E214	NET2PLL_CON1	32	NET2PLL Control Register 1
1001E21C	NET2PLL_PWR_CON0	32	NET2PLL Power Control Register 0
1001E220	MMPLL_CON0	32	MMPLL Control Register 0
1001E224	MMPLL_CON1	32	MMPLL Control Register 1
1001E22C	MMPLL_PWR_CON0	32	MMPLL Power Control Register 0
1001E230	SGMIIPLL_CON0	32	SGMIIPLL Control Register 0
1001E234	SGMIIPLL_CON1	32	SGMIIPLL Control Register 1
1001E23C	SGMIIPLL_PWR_CON0	32	SGMIIPLL Power Control Register 0
1001E240	WEDMCUPLL_CON0	32	WEDMCUPLL Control Register 0
1001E244	WEDMCUPLL_CON1	32	WEDMCUPLL Control Register 1
1001E24C	WEDMCUPLL_PWR_CON0	32	WEDMCUPLL Power Control Register 0
1001E250	NET1PLL_CON0	32	NET1PLL Control Register 0
1001E254	NET1PLL_CON1	32	NET1PLL Control Register 1
1001E25C	NET1PLL_PWR_CON0	32	NET1PLL Power Control Register 0
1001E260	MPLL_CON0	32	MPLL Control Register 0
1001E264	MPLL_CON1	32	MPLL Control Register 1
1001E26C	MPLL_CON3	32	MPLL Control Register 3
1001E270	MPLL_PWR_CON0	32	MPLL Power Control Register 0
1001E278	APLL2_CON0	32	APLL2 Control Register 0
1001E27C	APLL2_CON1	32	APLL2 Control Register 1
1001E284	APLL2_CON3	32	APLL2 Control Register 3
1001E288	APLL2_PWR_CON0	32	APLL2 Power Control Register 0
1001E28C	MMPLL_D3_CON0	32	MMPLL D3 Control Register 0
1001E3AC	DRAMC_CON	32	DRAMC PLL setting
1001E3A0	POR_CON0	32	POR Control Register 0
1001E3A4	POR_CON1	32	POR Control Register 1
1001E3A8	POR_CON2	32	POR Control Register 2
1001E400	AP_AUXADC_CON0	32	AUXADC Control Register 0
1001E600	TS_CON0	32	Thermal Sensor Control Register 0
1001E604	TS_CON1	32	Thermal Sensor Control Register 1

1001E000 AP_PLL_CON0 AP PLL Control Register 0 33F00023

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		CLKSQ1_RESERVE_EN			CLKSQ1_HYS_SEL			CLKSQ1_HYS_EN	CLKSQ1_QPHY1_40M_CK_EN	CLKSQ1_QPHY0_40M_CK_EN	CLKSQ1_GPHY_40M_CK_EN	CLKSQ1_40M_CK_EN				CLKSQ1_BIAS_LPF_EN
Type		RW			RW			RW	RW	RW	RW	RW				RW
Reset		0			0	0	1	1	1	1	1	1				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CLKSQ1_VOD_EN				CLKSQ1_MON_EN			CLKSQ1_LPF_EN_SEL	CLKSQ1_LPF_EN			CLKSQ1_EN_SEL	CLKSQ1_EN
Type				RW				RW			RW	RW			RW	RW
Reset				0				0			1	0			1	1

Bit(s)	Name	Description
30	CLKSQ1_RESERVE_EN	**Reserved** 0: Disable 1: Enable
27:25	CLKSQ1_HYS_SEL	**Selects clock square hysteresis level**
24	CLKSQ1_HYS_EN	**Enable clock square hysteresis level**
23	CLKSQ1_QPHY1_40M_CK_EN	**QPHY1 40M CK enable** 0: Disable 1: Enable
22	CLKSQ1_QPHY0_40M_CK_EN	**QPHY0 40M CK enable** 0: Disable 1: Enable
21	CLKSQ1_GPHY_40M_CK_EN	**GPHY 40M CK enable** 0: Disable 1: Enable
20	CLKSQ1_40M_CK_EN	**40M CK enable** 0: Disable 1: Enable
16	CLKSQ1_BIAS_LPF_EN	**Low-pass filter V2I's output** 0: Disable 1: Enable
12	CLKSQ1_VOD_EN	**Reserved** 0: Disable

Bit(s)	Name	Description
		1: Enable
8	CLKSQ1_MON_EN	**Enables clock square monitor**
		0: Disable
		1: Enable
5	CLKSQ1_LPF_EN_SEL	**Selects CLKSQ1 LPF_EN control**
		0: Sleep control
		1: Register control
4	CLKSQ1_LPF_EN	**Enables clock square1 low-pass filter**
1	CLKSQ1_EN_SEL	**Selects CLKSQ1 enable control**
		0: Sleep control
		1: Register control
0	CLKSQ1_EN	**Enables clock square1**

1001E004 **AP_PLL_CON1** **AP PLL Control Register 1** **030F030F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											NET1PLL_TUNER_EN	NET1PLL_OUT_OFF	NET1PLL_OUT_OFF_SEL	NET1PLL_EN_SEL	NET1PLL_ISO_SEL	NET1PLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ARMPLL_TUNER_EN	ARMPLL_OUT_OFF	ARMPLL_OUT_OFF_SEL	ARMPLL_EN_SEL	ARMPLL_ISO_SEL	ARMPLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
21	NET1PLL_TUNER_EN	**Enable NET1PLL tuning function**
20	NET1PLL_OUT_OFF	**Controls NET1PLL CG register**
19	NET1PLL_OUT_OFF_SEL	**Selects NET1PLL CG control** 0: Sleep control 1: Register control
18	NET1PLL_EN_SEL	**Selects NET1PLL enable control** 0: Sleep control 1: Register control
17	NET1PLL_ISO_SEL	**Selects NET1PLL ISO_EN control** 0: Sleep control 1: Register control
16	NET1PLL_PWR_SEL	**Selects NET1PLL PWR_ON control** 0: Sleep control 1: Register control
5	ARMPLL_TUNER_EN	**Enable APLL1 tuning function**
4	ARMPLL_OUT_OFF	**Controls ARMPLL CG register**
3	ARMPLL_OUT_OFF_SEL	**Selects ARMPLL CG control** 0: Sleep control 1: Register control
2	ARMPLL_EN_SEL	**Selects ARMPLL enable control** 0: Sleep control 1: Register control

Bit(s)	Name	Description
1	ARMPLL_ISO_SEL	**Selects ARMPLL ISO_EN control** 0: Sleep control 1: Register control
0	ARMPLL_PWR_SEL	**Selects ARMPLL PWR_ON control** 0: Sleep control 1: Register control

1001E008 **AP_PLL_CON2** **AP PLL Control Register 2** **030F030F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											APLL2_TUNER_EN	APLL2_OUT_OFF	APLL2_OUT_OFF_SEL	APLL2_EN_SEL	APLL2_ISO_SEL	APLL2_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											NET2PLL_TUNER_EN	NET2PLL_OUT_OFF	NET2PLL_OUT_OFF_SEL	NET2PLL_EN_SEL	NET2PLL_ISO_SEL	NET2PLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
21	APLL2_TUNER_EN	**Enable APLL2 tuning function**
20	APLL2_OUT_OFF	**Controls APLL2 CG register**
19	APLL2_OUT_OFF_SEL	**Selects APLL2 CG control** 0: Sleep control 1: Register control
18	APLL2_EN_SEL	**Selects APLL2 enable control** 0: Sleep control 1: Register control
17	APLL2_ISO_SEL	**Selects APLL2 ISO_EN control** 0: Sleep control 1: Register control
16	APLL2_PWR_SEL	**Selects APLL2 PWR_ON control** 0: Sleep control 1: Register control
5	NET2PLL_TUNER_EN	**Enable NET2PLL tuning function**
4	NET2PLL_OUT_OFF	**Controls NET2PLL CG register**
3	NET2PLL_OUT_OFF_SEL	**Selects NET2PLL CG control** 0: Sleep control 1: Register control
2	NET2PLL_EN_SEL	**Selects NET2PLL enable control** 0: Sleep control 1: Register control
1	NET2PLL_ISO_SEL	**Selects NET2PLL ISO_EN control**

Bit(s)	Name	Description
		0: Sleep control 1: Register control
0	NET2PLL_PWR_SEL	**Selects NET2PLL PWR_ON control** 0: Sleep control 1: Register control

1001E00C **AP_PLL_CON3** **AP PLL Control Register 3** **030F030F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											MMPLL_TUNER_EN	MMPLL_OUT_OFF	MMPLL_OUT_OFF_SEL	MMPLL_EN_SEL	MMPLL_ISO_SEL	MMPLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											WEDMCUPLL_TUNER_EN	WEDMCUPLL_OUT_OFF	WEDMCUPLL_OUT_OFF_SEL	WEDMCUPLL_EN_SEL	WEDMCUPLL_ISO_SEL	WEDMCUPLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
21	MMPLL_TUNER_EN	**Enable MMPLL tuning function**
20	MMPLL_OUT_OFF	**Controls MMPLL CG register**
19	MMPLL_OUT_OFF_SEL	**Selects MMPLL CG control** 0: Sleep control 1: Register control
18	MMPLL_EN_SEL	**Selects MMPLL enable control** 0: Sleep control 1: Register control
17	MMPLL_ISO_SEL	**Selects MMPLL ISO_EN control** 0: Sleep control 1: Register control
16	MMPLL_PWR_SEL	**Selects MMPLL PWR_ON control** 0: Sleep control 1: Register control
5	WEDMCUPLL_TUNER_EN	**Enable WEDMCUPLL tuning function**
4	WEDMCUPLL_OUT_OFF	**Controls WEDMCUPLL CG register**
3	WEDMCUPLL_OUT_OFF_SEL	**Selects WEDMCUPLL CG control** 0: Sleep control 1: Register control
2	WEDMCUPLL_EN_SEL	**Selects WEDMCUPLL enable control** 0: Sleep control 1: Register control

Bit(s)	Name	Description
1	WEDMCUPLL_ISO_SEL	**Selects WEDMCUPLL ISO_EN control** 0: Sleep control 1: Register control
0	WEDMCUPLL_PWR_SEL	**Selects WEDMCUPLL PWR_ON control** 0: Sleep control 1: Register control

1001E010 **AP_PLL_CON4** **AP PLL Control Register 4** **030F030F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											SGMIIPLL_TUNER_EN	SGMIIPLL_OUT_OFF	SGMIIPLL_OUT_OFF_SEL	SGMIIPLL_EN_SEL	SGMIIPLL_ISO_SEL	SGMIIPLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											MPLL_TUNER_EN	MPLL_OUT_OFF	MPLL_OUT_OFF_SEL	MPLL_EN_SEL	MPLL_ISO_SEL	MPLL_PWR_SEL
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	1	1	1	1

Bit(s)	Name	Description
21	SGMIIPLL_TUNER_EN	**Enable SGMIIPLL tuning function**
20	SGMIIPLL_OUT_OFF	**Controls SGMIIPLL CG register**
19	SGMIIPLL_OUT_OFF_SEL	**Selects SGMIIPLL CG control** 0: Sleep control 1: Register control
18	SGMIIPLL_EN_SEL	**Selects SGMIIPLL enable control** 0: Sleep control 1: Register control
17	SGMIIPLL_ISO_SEL	**Selects SGMIIPLL ISO_EN control** 0: Sleep control 1: Register control
16	SGMIIPLL_PWR_SEL	**Selects SGMIIPLL PWR_ON control** 0: Sleep control 1: Register control
5	MPLL_TUNER_EN	**Enable MPLL tuning function**
4	MPLL_OUT_OFF	**Controls MPLL CG register**
3	MPLL_OUT_OFF_SEL	**Selects MPLL CG control** 0: Sleep control 1: Register control
2	MPLL_EN_SEL	**Selects MPLL enable control** 0: Sleep control 1: Register control
1	MPLL_ISO_SEL	**Selects MPLL ISO_EN control**

Bit(s)	Name	Description
		0: Sleep control 1: Register control
0	MPLL_PWR_SEL	**Selects MPLL PWR_ON control** 0: Sleep control 1: Register control

1001E014 **AP_PLL_CON5** **AP PLL Control Register 5** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**MDPLL2_FS26M_CK**	**MDPLL1_ARM26M_CK_EN**	**MDPLL1_MEM26M_CK_EN**	**MDPLL1_MIPI26M_CK_EN**	**MDPLL1_FS26M_CK_EN**
Type												RW	RW	RW	RW	RW
Reset												1	1	1	1	1

Bit(s)	Name	Description
4	MDPLL2_FS26M_CK	**Enables MDPLL2 FS 26 MHz clock source**
3	MDPLL1_ARM26M_CK_EN	**Enables ARM 26 MHz clock source**
2	MDPLL1_MEM26M_CK_EN	**Enables MEM 26 MHz clock source**
1	MDPLL1_MIPI26M_CK_EN	**Enables MIPI 26 MHz clock source**
0	MDPLL1_FS26M_CK_EN	**Enables FS 26 MHz clock source**

1001E018 **AP_PLL_CON6** **AP PLL Control Register 6** **00FF00FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									MMPLLDIV_RSTB_SEL	MPLLDIV_RSTB_SEL	SGMIIPLLDIV_RSTB_SEL	ARMPLLDIV_RSTB_SEL	APLL2DIV_RSTB_SEL	NET1PLLDIV_RSTB_SEL	NET2PLLDIV_RSTB_SEL	WEDMCUPLLDIV_RSTB_SEL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	MMPLLDIV_RSTB_SEL	**Selects MMPLL DIV_RSTB control** 0: Sleep control 1: Register control
22	MPLLDIV_RSTB_SEL	**Selects MPLL DIV_RSTB control** 0: Sleep control 1: Register control
21	SGMIIPLLDIV_RSTB_SEL	**Selects SGMIIPLL DIV_RSTB control** 0: Sleep control 1: Register control
20	ARMPLLDIV_RSTB_SEL	**Selects ARMPLL DIV_RSTB control** 0: Sleep control 1: Register control
19	APLL2DIV_RSTB_SEL	**Selects APLL2 DIV_RSTB control** 0: Sleep control 1: Register control
18	NET1PLLDIV_RSTB_SEL	**Selects NET1PLL DIV_RSTB control** 0: Sleep control 1: Register control
17	NET2PLLDIV_RSTB_SEL	**Selects NET2PLL DIV_RSTB control** 0: Sleep control 1: Register control
16	WEDMCUPLLDIV_RSTB_SEL	**Selects WEDMCUPLL DIV_RSTB control** 0: Sleep control

Bit(s)	Name	Description
		1: Register control

1001E040 PLL_TEST_CON0 PLL Test Control Register 0 FF000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PLLGP_RESERVE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		PLLGP_LTEREF_MON_CK_EN	PLLGP_C2KREF_MON_CK_EN		PLLGP_MONREF_EN	PLLGP_LVROD_EN	PLLGP_TST_SEL				PLLGP_VOD_EN	PLLGP_OPEN	PLLGP_TSTOD_EN	PLLGP_A2DCK_EN	PLLGP_TSTCK_EN	PLLGP_TST_EN
Type		RW	RW		RW	RW	RW				RW	RW	RW	RW	RW	RW
Reset		0	0		0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PLLGP_RESERVE	**Reserved**
14	PLLGP_LTEREF_MON_CK_EN	**Enables REF_CK monitor**
13	PLLGP_C2KREF_MON_CK_EN	**Enables REF_CK monitor**
11	PLLGP_MONREF_EN	**Enables FBK clock testing mode**
10	PLLGP_LVROD_EN	**Overdrive open drain LDO**
9:8	PLLGP_TST_SEL	**Selects test mux**
5	PLLGP_VOD_EN	**Overdrive open drain LDO**
4	PLLGP_OPEN	**Enable open drain**
3	PLLGP_TSTOD_EN	**Enables open drain**
2	PLLGP_A2DCK_EN	**Enables frequency meter path**
1	PLLGP_TSTCK_EN	**Enables PLL output clock testing mode**
0	PLLGP_TST_EN	**Enables testing mode**

1001E044 **PLL_TEST_CON1** **PLL Test Control Register 1** **FF000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARMPLL_TOP_RESERVE															
Type	RW															
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ARMPLL_TOP_REF_MON_CK_EN		ARMPLL_TOP_MONREF_EN	ARMPLL_TOP_LVROD_EN	ARMPLL_TOP_TST_SEL		ARMPLL_TOP_TSTMUX				ARMPLL_TOP_TSTOD_EN	ARMPLL_TOP_A2DCK_EN	ARMPLL_TOP_TSTCK_EN	ARMPLL_TOP_TST_EN
Type			RW		RW	RW	RW		RW				RW	RW	RW	RW
Reset			0		0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ARMPLL_TOP_RESERVE	**Reserved**
13	ARMPLL_TOP_REF_MON_CK_EN	**Enables REF_CK monitor**
11	ARMPLL_TOP_MONREF_EN	**Enables REF_CK monitor**
10	ARMPLL_TOP_LVROD_EN	**Overdrive open drain LDO**
9:8	ARMPLL_TOP_TST_SEL	**Selects test mux**
7:4	ARMPLL_TOP_TSTMUX	**Selects test mux**
3	ARMPLL_TOP_TSTOD_EN	**Enables open drain**
2	ARMPLL_TOP_A2DCK_EN	**Enables frequency meter path**
1	ARMPLL_TOP_TSTCK_EN	**Enables PLL output clock testing mode**
0	ARMPLL_TOP_TST_EN	**Enables testing mode**

1001E048 PLL_TEST_CON2 PLL Test Control Register 2 00000076

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							QI_ALDO_OC_STATUS_SEL			PLLGP_REFCK_DIV2_SEL	PCIE_XTAL25M_OUT_EN	MEM25M_OUT_EN		SSUSB_SR_DRIVER_EN	SSUSB_SR_GATE_ENB	PLLGP25M_REF_MON_EN
Type							RW			RW	RW	RW		RW	RW	RW
Reset							0	0		1	1	1		1	1	0

Bit(s)	Name	Description
9:8	QI_ALDO_OC_STATUS_SEL	**No use**
6	PLLGP_REFCK_DIV2_SEL	**Reference clock divide option** 1'b0: Divided by 2 1'b1: Not divided
5	PCIE_XTAL25M_OUT_EN	**No use**
4	MEM25M_OUT_EN	**No use**
2	SSUSB_SR_DRIVER_EN	**Gating SSUSB SR**
1	SSUSB_SR_GATE_ENB	**No use**
0	PLLGP25M_REF_MON_EN	**Enable REFCLK to monitor path**

1001E200 ARMPLL_CON0 ARMPLL Control Register 0 00670114

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ARMPLL_BP	ARMPLL_BR	ARMPLL_LVROD_EN	ARMPLL_RST_DLY		ARMPLL_GLITCH_FREE_EN	ARMPLL_BLP
Type										RW	RW	RW	RW		RW	RW
Reset										1	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ARMPLL_SDM_FRA_EN		ARMPLL_POSDIV				ARMPLL_SDM_PCW_CHG		ARMPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	0	1		1		0

Bit(s)	Name	Description
22	ARMPLL_BP	**Enables fast locking**
21	ARMPLL_BR	**LPF bandwidth control; 1'b0: wide; 1'b1: narrow**
20	ARMPLL_LVROD_EN	**Overdrive LDO**
19:18	ARMPLL_RST_DLY	**Test sequence delay control**
17	ARMPLL_GLITCH_FREE_EN	**Enables glitch free**
16	ARMPLL_BLP	**LPF bandwidth control; should be the same as ARMPLL_BP**
8	ARMPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode**
		0: Integer mode
		1: Fractional mode
6:4	ARMPLL_POSDIV	**Post divide ratio**
		000: /1
		001: /2
		010: /4
		011: /8
		100: /16
2	ARMPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	ARMPLL_EN	**Enables PLL**

1001E204 **ARMPLL_CON1** **ARMPLL Control Register 1** **64000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARMPLL_SDM_PCW															
Type	RW															
Reset	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARMPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ARMPLL_SDM_PCW	**Feedback divide ratio**

1001E20C ARMPLL_PWR_CON0 ARMPLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARMPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ARMPLL_SDM_ISO_EN	ARMPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	ARMPLL_SDM_PWR_ACK	**ARMPLL power ack**
1	ARMPLL_SDM_ISO_EN	**Enables ARMPLL ISO**
0	ARMPLL_SDM_PWR_ON	**ARMPLL power-on**

1001E210 **NET2PLL_CON0** **NET2PLL Control Register 0** **E8010114**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NET2PLL_DIV2_EN	NET2PLL_DIV3_EN	NET2PLL_DIV4_EN	NET2PLL_DIV5_EN	NET2PLL_DIV6_EN	NET2PLL_DIV7_EN	NET2PLL_DIV8_EN	NET2PLL_DIV9_EN	NET2PLL_DIV_RSTB						NET2PLL_GLITCH_FREE_EN	NET2PLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW						RW	RW
Reset	1	1	1	0	1	0	0	0	0						0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								NET2PLL_SDM_FRA_EN		NET2PLL_POSDIV				NET2PLL_SDM_PCW_CHG		NET2PLL_EN
Type								RW		RW				RW		RW
Reset								1		0	0	1		1		0

Bit(s)	Name	Description
31	NET2PLL_DIV2_EN	**Enables NET2PLL DIV2**
30	NET2PLL_DIV3_EN	**Enables NET2PLL DIV3**
29	NET2PLL_DIV4_EN	**Enables NET2PLL DIV4**
28	NET2PLL_DIV5_EN	**Enables NET2PLL DIV5**
27	NET2PLL_DIV6_EN	**Enables NET2PLL DIV6**
26	NET2PLL_DIV7_EN	**Enables NET2PLL DIV7**
25	NET2PLL_DIV8_EN	**Enables NET2PLL DIV8**
24	NET2PLL_DIV9_EN	**Enables NET2PLL DIV9**
23	NET2PLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
17	NET2PLL_GLITCH_FREE_EN	**Enables glitch free**
16	NET2PLL_BLP	**LPF bandwidth control**
8	NET2PLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4	NET2PLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16

Bit(s)	Name	Description
2	NET2PLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	NET2PLL_EN	**Enables PLL**

1001E214 **NET2PLL_CON1** **NET2PLL Control Register 1** **50000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NET2PLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NET2PLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NET2PLL_SDM_PCW	**Feedback divide ratio**

1001E21C NET2PLL_PWR_CON0 NET2PLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NET2PLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															NET2PLL_SDM_ISO_EN	NET2PLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	NET2PLL_SDM_PWR_ACK	**NET2PLL power ack**
1	NET2PLL_SDM_ISO_EN	**Enables NET2PLL ISO**
0	NET2PLL_SDM_PWR_ON	**NET2PLL power-on**

1001E220 **MMPLL_CON0** **MMPLL Control Register 0** **FA010124**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_DIV2_EN	MMPLL_DIV3_EN	MMPLL_DIV4_EN	MMPLL_DIV5_EN	MMPLL_DIV6_EN	MMPLL_DIV7_EN	MMPLL_DIV8_EN	MMPLL_DIV9_EN	MMPLL_DIV_RSTB						MMPLL_GLITCH_FREE_EN	MMPLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW						RW	RW
Reset	1	1	1	1	1	0	1	0	0						0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MMPLL_SDM_FRA_EN		MMPLL_POSDIV				MMPLL_SDM_PCW_CHG		MMPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	1	0		1		0

Bit(s)	Name	Description
31	MMPLL_DIV2_EN	**Enables MMPLL DIV2**
30	MMPLL_DIV3_EN	**Enables MMPLL DIV3**
29	MMPLL_DIV4_EN	**Enables MMPLL DIV4**
28	MMPLL_DIV5_EN	**Enables MMPLL DIV5**
27	MMPLL_DIV6_EN	**Enables MMPLL DIV6**
26	MMPLL_DIV7_EN	**Enables MMPLL DIV7**
25	MMPLL_DIV8_EN	**Enables MMPLL DIV8**
24	MMPLL_DIV9_EN	**Enables MMPLL DIV9**
23	MMPLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
17	MMPLL_GLITCH_FREE_EN	**Enables glitch free**
16	MMPLL_BLP	**LPF bandwidth control**
8	MMPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4	MMPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16

Bit(s)	Name	Description
2	MMPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	MMPLL_EN	**Enables PLL**

1001E224 **MMPLL_CON1** **MMPLL Control Register 1** **90000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_SDM_PCW															
Type	RW															
Reset	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MMPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MMPLL_SDM_PCW	**Feedback divide ratio**

1001E22C MMPLL_PWR_CON0 MMPLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MMPLL_SDM_ISO_EN	MMPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	MMPLL_SDM_PWR_ACK	**MMPLL power ack**
1	MMPLL_SDM_ISO_EN	**Enables MMPLL ISO**
0	MMPLL_SDM_PWR_ON	**MMPLL power-on**

1001E230 SGMIIPLL_CON0 SGMIIPLL Control Register 0 00010134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															SGMIIPLL_GLITCH_FREE_EN	SGMIIPLL_BLP
Type															RW	RW
Reset															0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SGMIIPLL_SDM_FRA_EN		SGMIIPLL_POSDIV				SGMIIPLL_SDM_PCW_CHG		SGMIIPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	1	1		1		0

Bit(s)	Name	Description
17	SGMIIPLL_GLITCH_FREE_EN	**Enables glitch free**
16	SGMIIPLL_BLP	**LPF bandwidth control**
8	SGMIIPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode**
		0: Integer mode
		1: Fractional mode
6:4	SGMIIPLL_POSDIV	**Post divide ratio**
		000: /1
		001: /2
		010: /4
		011: /8
		100: /16
2	SGMIIPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	SGMIIPLL_EN	**Enables PLL**

1001E234 **SGMIIPLL_CON1** **SGMIIPLL Control Register 1** **82000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMIIPLL_SDM_PCW															
Type	RW															
Reset	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMIIPLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SGMIIPLL_SDM_PCW	**Feedback divide ratio**

1001E23C SGMIIPLL_PWR_CON0 SGMIIPLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMIIPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SGMIIPLL_SDM_ISO_EN	SGMIIPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	SGMIIPLL_SDM_PWR_ACK	**SGMIIPLL power ack**
1	SGMIIPLL_SDM_ISO_EN	**Enables SGMIIPLL ISO**
0	SGMIIPLL_SDM_PWR_ON	**SGMIIPLL power-on**

1001E240 WEDMCUPLL_CON0 WEDMCUPLL Control Register 0 10010144

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WEDMCUPLL_DIV2_EN	WEDMCUPLL_DIV3_EN	WEDMCUPLL_DIV4_EN	WEDMCUPLL_DIV5_EN	WEDMCUPLL_DIV7_EN	WEDMCUPLL_DIV8_EN		WEDMCUPLL_DIV9_EN	WEDMCUPLL_DIV_RSTB						WEDMCUPLL_GLITCH_FREE_EN	WEDMCUPLL_BLP
Type	RW	RW	RW	RW	RW	RW		RW	RW						RW	RW
Reset	0	0	0	1	0	0		0	0						0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								WEDMCUPLL_SDM_FRA_EN		WEDMCUPLL_POSDIV				WEDMCUPLL_SDM_PCW_CHG		WEDMCUPLL_EN
Type								RW		RW				RW		RW
Reset								1		1	0	0		1		0

Bit(s)	Name	Description
31	WEDMCUPLL_DIV2_EN	**Enables WEDMCUPLL DIV2**
30	WEDMCUPLL_DIV3_EN	**Enables WEDMCUPLL DIV3**
29	WEDMCUPLL_DIV4_EN	**Enables WEDMCUPLL DIV4**
28	WEDMCUPLL_DIV5_EN	**Enables WEDMCUPLL DIV5**
27	WEDMCUPLL_DIV7_EN	**Enables WEDMCUPLL DIV7**
26	WEDMCUPLL_DIV8_EN	**Enables WEDMCUPLL DIV8**
24	WEDMCUPLL_DIV9_EN	**No use**
23	WEDMCUPLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
17	WEDMCUPLL_GLITCH_FREE_EN	**Enables glitch free**
16	WEDMCUPLL_BLP	**LPF bandwidth control**
8	WEDMCUPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4	WEDMCUPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16

Bit(s)	Name	Description
2	WEDMCUPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	WEDMCUPLL_EN	**Enables PLL**

1001E244 **WEDMCUPLL_CON1** **WEDMCUPLL Control Register 1** **A6666666**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WEDMCUPLL_SDM_PCW															
Type	RW															
Reset	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WEDMCUPLL_SDM_PCW															
Type	RW															
Reset	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

Bit(s)	Name	Description
31:0	WEDMCUPLL_SDM_PCW	**Feedback divide ratio**

1001E24C **WEDMCUPLL_PWR_CON0** **WEDMCUPLL Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WEDMCUPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WEDMCUPLL_SDM_ISO_EN	WEDMCUPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	WEDMCUPLL_SDM_PWR_ACK	**WEDMCUPLL power ack**
1	WEDMCUPLL_SDM_ISO_EN	**Enables WEDMCUPLL ISO**
0	WEDMCUPLL_SDM_PWR_ON	**WEDMCUPLL power-on**

1001E250 **NET1PLL_CON0** **NET1PLL Control Register 0** **32010104**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NET1PLL_DIV2_EN	NET1PLL_DIV3_EN	NET1PLL_DIV4_EN	NET1PLL_DIV5_EN	NET1PLL_DIV6_EN	NET1PLL_DIV7_EN	NET1PLL_DIV8_EN	NET1PLL_DIV9_EN	NET1PLL_DIV_RSTB						NET1PLL_GLITCH_FREE_EN	NET1PLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW						RW	RW
Reset	0	0	1	1	0	0	1	0	0						0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								NET1PLL_SDM_FRA_EN		NET1PLL_POSDIV				NET1PLL_SDM_PCW_CHG		NET1PLL_EN
Type								RW		RW				RW		RW
Reset								1		0	0	0		1		0

Bit(s)	Name	Description
31	NET1PLL_DIV2_EN	**Enables NET1PLL DIV2**
30	NET1PLL_DIV3_EN	**Enables NET1PLL DIV3**
29	NET1PLL_DIV4_EN	**Enables NET1PLL DIV4**
28	NET1PLL_DIV5_EN	**Enables NET1PLL DIV5**
27	NET1PLL_DIV6_EN	**Enables NET1PLL DIV6**
26	NET1PLL_DIV7_EN	**Enables NET1PLL DIV7**
25	NET1PLL_DIV8_EN	**Enables NET1PLL DIV8**
24	NET1PLL_DIV9_EN	**Enables NET1PLL DIV9**
23	NET1PLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
17	NET1PLL_GLITCH_FREE_EN	**Enables glitch free**
16	NET1PLL_BLP	**LPF bandwidth control**
8	NET1PLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4	NET1PLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16

Bit(s)	Name	Description
2	NET1PLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	NET1PLL_EN	**Enables PLL**

1001E254 **NET1PLL_CON1** **NET1PLL Control Register 1** **7D000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NET1PLL_SDM_PCW															
Type	RW															
Reset	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NET1PLL_SDM_PCW															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NET1PLL_SDM_PCW	**Feedback divide ratio**

1001E25C NET1PLL_PWR_CON0 NET1PLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NET1PLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															NET1PLL_SDM_ISO_EN	NET1PLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	NET1PLL_SDM_PWR_ACK	**NET1PLL power ack**
1	NET1PLL_SDM_ISO_EN	**Enables NET1PLL ISO**
0	NET1PLL_SDM_PWR_ON	**NET1PLL power-on**

1001E260 MPLL_CON0 MPLL Control Register 0 E2010124

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPLL_DIV2_EN	MPLL_DIV3_EN	MPLL_DIV4_EN	MPLL_DIV5_EN	MPLL_DIV6_EN	MPLL_DIV7_EN	MPLL_DIV8_EN	MPLL_DIV9_EN	MPLL_DIV_RSTB						MPLL_GLITCH_FREE_EN	MPLL_BLP
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW						RW	RW
Reset	1	1	1	0	0	0	1	0	0						0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MPLL_SDM_FRA_EN		MPLL_POSDIV				MPLL_SDM_PCW_CHG		MPLL_EN
Type								RW		RW				RW		RW
Reset								1		0	1	0		1		0

Bit(s)	Name	Description
31	MPLL_DIV2_EN	**Enables MPLL DIV2**
30	MPLL_DIV3_EN	**Enables MPLL DIV3**
29	MPLL_DIV4_EN	**Enables MPLL DIV4**
28	MPLL_DIV5_EN	**Enables MPLL DIV5**
27	MPLL_DIV6_EN	**Enables MPLL DIV6**
26	MPLL_DIV7_EN	**Enables MPLL DIV7**
25	MPLL_DIV8_EN	**Enables MPLL DIV8**
24	MPLL_DIV9_EN	**Enables MPLL DIV9**
23	MPLL_DIV_RSTB	**PLL divider reset bar** 0: Reset 1: Enable
17	MPLL_GLITCH_FREE_EN	**Enables glitch free**
16	MPLL_BLP	**LPF bandwidth control**
8	MPLL_SDM_FRA_EN	**Enables SDMPLL fractional mode** 0: Integer mode 1: Fractional mode
6:4	MPLL_POSDIV	**Post divide ratio** 000: /1 001: /2 010: /4 011: /8 100: /16

Bit(s)	Name	Description
2	MPLL_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	MPLL_EN	**Enables PLL**

1001E264 **MPLL_CON1** **MPLL Control Register 1** **53333333**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPLL_SDM_PCW															
Type	RW															
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Bit(s)	Name	Description
31:0	MPLL_SDM_PCW	**Feedback divide ratio**

1001E26C **MPLL_CON3** **MPLL Control Register 3** **53333333**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPLL_TUNER_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MPLL_TUNER_SDM_PCW															
Type	RW															
Reset	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Bit(s)	Name	Description
31:0	MPLL_TUNER_SDM_PCW	**Tune divide ratio**

1001E270 MPLL_PWR_CON0 MPLL Power Control Register 0 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MPLL_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															MPLL_SDM_ISO_EN	MPLL_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	MPLL_SDM_PWR_ACK	**MPLL power ack**
1	MPLL_SDM_ISO_EN	**Enables MPLL ISO**
0	MPLL_SDM_PWR_ON	**MPLL power-on**

1001E278 APLL2_CON0 APLL2 Control Register 0 00010134

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															APLL2_GLITCH_FREE_EN	APLL2_BLP
Type															RW	RW
Reset															0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								APLL2_SDM_FRA_EN		APLL2_POSDIV				APLL2_SDM_PCW_CHG		APLL2_EN
Type								RW		RW				RW		RW
Reset								1		0	1	1		1		0

Bit(s)	Name	Description
17	APLL2_GLITCH_FREE_EN	**Enables glitch free**
16	APLL2_BLP	**LPF bandwidth control**
8	APLL2_SDM_FRA_EN	**Enables SDAPLL2 fractional mode**
		0: Integer mode
		1: Fractional mode
6:4	APLL2_POSDIV	**Post divide ratio**
		000: /1
		001: /2
		010: /4
		011: /8
		100: /16
2	APLL2_SDM_PCW_CHG	**Feedback divide ratio update signal**
0	APLL2_EN	**Enables PLL**

1001E27C **APLL2_CON1** **APLL2 Control Register 1** **4EA4A8C1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL2_SDM_PCW															
Type	RW															
Reset	0	1	0	0	1	1	1	0	1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APLL2_SDM_PCW															
Type	RW															
Reset	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	APLL2_SDM_PCW	**Feedback divide ratio**

1001E284 **APLL2_CON3** **APLL2 Control Register 3** **4EA4A8C1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL2_TUNER_SDM_PCW															
Type	RW															
Reset	0	1	0	0	1	1	1	0	1	0	1	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APLL2_TUNER_SDM_PCW															
Type	RW															
Reset	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	APLL2_TUNER_SDM_PCW	**Tune divide ratio**

1001E288 **APLL2_PWR_CON0** **APLL2 Power Control Register 0** **00000002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	APLL2_SDM_PWR_ACK															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															APLL2_SDM_ISO_EN	APLL2_SDM_PWR_ON
Type															RW	RW
Reset															1	0

Bit(s)	Name	Description
31	APLL2_SDM_PWR_ACK	**APLL2 power ack**
1	APLL2_SDM_ISO_EN	**Enables APLL2 ISO**
0	APLL2_SDM_PWR_ON	**APLL2 power-on**

1001E28C **MMPLL_D3_CON0** **MMPLL D3 Control Register 0** **10000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMPLL_D3_DIV2_EN	MMPLL_D3_DIV3_EN	MMPLL_D3_DIV4_EN	MMPLL_D3_DIV5_EN	MMPLL_D3_DIV6_EN	MMPLL_D3_DIV7_EN	MMPLL_D3_DIV8_EN	MMPLL_D3_DIV9_EN								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	1	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	MMPLL_D3_DIV2_EN	**Enables MMPLL D3 DIV2 for the pll clk divider inside cksys**
30	MMPLL_D3_DIV3_EN	**Enables MMPLL D3 DIV3**
29	MMPLL_D3_DIV4_EN	**Enables MMPLL D3 DIV4**
28	MMPLL_D3_DIV5_EN	**Enables MMPLL D3 DIV5**
27	MMPLL_D3_DIV6_EN	**Enables MMPLL D3 DIV6**
26	MMPLL_D3_DIV7_EN	**Enables MMPLL D3 DIV7**
25	MMPLL_D3_DIV8_EN	**Enables MMPLL D3 DIV8**
24	MMPLL_D3_DIV9_EN	**Enables MMPLL D3 DIV9**

1001E3AC **DRAMC_CON** **DRAMC PLL setting** **00005209**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RG_RPHYPLL_FBKSEL	RG_RPHYPLL_EN	RG_RPHYPLL_RESETB	RG_OCCCLK_FORM_MEMPLL								
Type					RW	RW	RW	RW								
Reset					0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_RPHYPLL_SDM_PCW															
Type	RW															
Reset	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
27	RG_RPHYPLL_FBKSEL	**RPHYPLL_FBK select**
26	RG_RPHYPLL_EN	**RPHYPLL enable**
25	RG_RPHYPLL_RESETB	**RPHYPLL resetb**
24	RG_OCCCLK_FORM_MEMPLL	**OCCCLK_FORM_MEMPLL select**
15:0	RG_RPHYPLL_SDM_PCW	**Feedback divide ratio** 8-bit integer + 24-bit fractional Default value: 16'h5209

1001E3A0 **POR_CON0** **POR Control Register 0** **00010011**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RG_STRUP_UVLO_BYPASS				RG_STRUP_OT_BYPASS				RG_STRUP_POR_BYPASS				RG_STRUP_OT_EN
Type				RW				RW				RW				RW
Reset				0				0				0				1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_STRUP_BG_UNCHOP_PH				RG_STRUP_BG_UNCHOP_Q				RG_STRUP_BG_UNCHOP				RG_STRUP_BG_SC_EN
Type				RW				RW				RW				RW
Reset				0				0				1				1

Bit(s)	Name	Description
28	RG_STRUP_UVLO_BYPASS	**Bypass UVLO** 0: Disable (Default) 1: Enable
24	RG_STRUP_OT_BYPASS	**Bypass OT** 0: Disable (Default) 1: Enable
20	RG_STRUP_POR_BYPASS	**Bypass POR** 0: Disable (Default) 1: Enable
16	RG_STRUP_OT_EN	**Over Temp** 0: Disable 1: Enable (Default)
12	RG_STRUP_BG_UNCHOP_PH	**BandGap Chopper CLK control_2** 0: (Default)
8	RG_STRUP_BG_UNCHOP_Q	**BandGap Chopper CLK control_3** 0: (Default)
4	RG_STRUP_BG_UNCHOP	**BandGap Chopper CLK control_1** 1: (Default)
0	RG_STRUP_BG_SC_EN	**BandGap Chopper EN** 1: EN (Default)

1001E3A4 **POR_CON1** **POR Control Register 1** **00200008**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RG_STRUP_POR_SEL			RG_STRUP_BG_TC_TRIM		
Type											RW			RW		
Reset											1	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_STRUP_BG_UNCHOP_Q_PH		RG_STRUP_BG_VC_TRIM								RG_STRUP_BGCLK_TRIM			
Type			RW		RW								RW			
Reset			0	0	0	0	0	0					1	0	0	0

Bit(s)	Name	Description
21:20	RG_STRUP_POR_SEL	**POR Level Sel** 11:1.1v 10:1v(Default) 01:0.9v 00:0.8v
18:16	RG_STRUP_BG_TC_TRIM	**BandGap TC Trim** 000: Good TC (Default)
13:12	RG_STRUP_BG_UNCHOP_Q_PH	**BandGap Chopper CLK control_4** 00: (Default)
11:8	RG_STRUP_BG_VC_TRIM	**BandGap VC Trim** 0000: Good VC (Default)
3:0	RG_STRUP_BGCLK_TRIM	**RG_STRUP_BGCLK_TRIM**

1001E3A8 **POR_CON2** **POR Control Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				AD_PMU_RSTB_STATUS				AD_BGRDY_STATUS				AD_OT_STATUS				AD_UVLO_STATUS
Type				RO				RO				RO				RO
Reset				0				0				0				0

Bit(s)	Name	Description
12	AD_PMU_RSTB_STATUS	**RSTB Status**
8	AD_BGRDY_STATUS	**BG Ready Status**
4	AD_OT_STATUS	**Over Temp Status**
0	AD_UVLO_STATUS	**UVLO Status**

1001E400 **AP_AUXADC_CON0** **AUXADC Control Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUXADC_RSV															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												AUXADC_FS	AUXADC_CALI			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Name	Description
31:24	AUXADC_RSV	**Reserved**
4	AUXADC_FS	**Reserved**
3:0	AUXADC_CALI	**ADC core bias current calibration** 0000: 1X 0001: 1.25X 0010: 1.5X 0011: 1.75X 0100: 2X 1000: 1X 1001: 0.8X 1010: 0.67X 1011: 0.57X 1100: 0.5X

1001E600 TS_CON0 Thermal Sensor Control Register 0 02020004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BGR_RSV								BGR_TCTRL							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BGR_CTRL				BGR_RSEL							BGR_UGB	BGR_BUFIN	BGR_FSETUP	BGR_UNCHOP_PH	BGR_UNCHOP
Type	RW				RW							RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0				0	0	1	0	0

Bit(s)	Name	Description
31:24	BGR_RSV	**RG_BGR_RSV[7:1]: Reserved register** RG_BGR_RSV[0]: Enable VBGR output to PAD_TESTIIN 0: Disable 1: Enable
23:16	BGR_TCTRL	**BGR_TCTRL[1:0]: BGR Replica VBE TSensor chopping control** 00: Unchop, PH = 0 01: Unchop, PH = 1 10: Chop 11: Disable The current for VBE TSensor is also as the reference of calibrating VBE TSensor for 00/01/10 mode. By setting RG_BGR_CTRL[3] = 1 and RG_BGR_TCTRL[1:0] = 11,the current source of calibrating VBE can be applied externally (drawn from PD_TESTIIN). BGR_TCTRL[3:2]: PAD_TSOUT output selection 00: Disable TSOUT 01: IPTAT_OUT (for VBE calibration) 10: VBE_MCU 11: VBE_ABB RG_BGR_TCTRL[7:4]: IPTAT VBE TSensor current selection 0000: 100000000 for 1I calibrating VBE 0001: 010000000 for 1I calibrating VBE 0010: 001000000 for 1I calibrating VBE 0011: 000100000 for 1I calibrating VBE

Bit(s)	Name	Description
		0100: 000010000 for 1I calibrating VBE
		0101: 000001000 for 1I calibrating VBE
		0110: 000000100 for 1I calibrating VBE
		0111: 000000010 for 1I calibrating VBE
		1000: 000000001 for 1I calibrating VBE
		1001: 111000000 for 3I calibrating VBE
		1010: 000111000 for 3I calibrating VBE
		1011: 000000111 for 3I calibrating VBE
		1100: 111111111 for 9I calibrating VBE
15:12	BGR_CTRL	**RG_BGR_CTRL[2:0]: BGR resistor selection for denominator**
		RG_BGR_CTRL[3]: Enable test current input
		0: Disable test current
		1: Enable test current. In this mode, PAD_TESTIIN is used for applying calibrating VBE TSensor current. (see RG_BGR_TCTRL[1:0].)
11:8	BGR_RSEL	**Selects BGR resistor for numerator**
4	BGR_UGB	**BGR VBUFFER force unity gain mode**
		0: Disable
		1: Enable
3	BGR_BUFIN	**BGR VBUFFER external input mode**
		0: Disable
		1: Enable
2	BGR_FSETUP	**BGR fast setup control**
		0: Disable resistor in low pass filter, speed up settling
		1: Enable low pass filter
1	BGR_UNCHOP_PH	**Selects BGR unchop mode phase**
0	BGR_UNCHOP	**BGR unchop mode**
		0: Chop
		1: Unchop

1001E604 TS_CON1 Thermal Sensor Control Register 1 00040030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														ADCMUXIN	MONITOR	
Type														RW	RW	
Reset														1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											TS2AUXADC			VBE_SEL		
Type											RW			RW		
Reset											1	1		0	0	0

Bit(s)	Name	Description
18	ADCMUXIN	**Enable AUXADC INPUT MUX** If PAD is in monitor, please set RG_ADCMUXIN = 0 or the monitor signal will go into AUXADC 1'b0: Disable PAD_AUXIN0 and PAD_AUXIN1 to MUX path 1'b1: Enable PAD_AUXIN0 and PAD_AUXIN1 to MUX path
17:16	MONITOR	**MONITOR output MUX control** 2'b00: Disable monitor MUX and PLLGP PAD out, PAD_AUXIN1 = NS_PLLGP_PAD_TN, PAD_AUXIN3 = NS_PLLGP_PAD_TP 2'b01: Monitor SSUSB, PAD_AUXIN0 = ADA_SATA_MONOUT, PAD_AUXIN1 = ADA_SSUSB_MONOUT, PAD_AUXIN2 = ADA_PCIE_MONOUT, PAD_AUXIN3 = ADA_XSGMII_MONOUT 2'b10: Monitor PLLGP/POR, PAD_AUXIN0 = GND, PAD_AUXIN1 = ADA_POR_MONITOR_18, PAD_AUXIN2 = ADA_PLLGP_TST_VC, PAD_AUXIN3 = ADA_NS_TANA_IN_FE 2'b11: Monitor BTRF, PAD_AUXIN0 = ADA_BT_TEST_IP, PAD_AUXIN1 = ADA_BT_TEST_QP, PAD_AUXIN2 = ADA_BT_TEST_IN, PAD_AUXIN3 = ADA_BT_TEST_QN
5:4	TS2AUXADC	**Enables output buffer and selects TS output to AUXADC** 00: Buffer on, TSMCU to AUXADC 01: Buffer on, TSABB to AUXADC 10: Buffer on, VBGR to AUXADC 11: Buffer off
2:0	VBE_SEL	**Selects VBE**

2.4 Thermal Controller

2.4.1 Register Definition

Module name: ptp_therm_ctrl Base address: (+0x1100_C000)

Address	Name	Width	Register Function
1100C800	TEMPMONCTL0	32	Temperature Monitoring Control 0
1100C804	TEMPMONCTL1	32	Temperature Monitoring Control 1
1100C808	TEMPMONCTL2	32	Temperature Monitoring Control 2
1100C80C	TEMPMONINT	32	Temperature Monitoring Interrupt Enable
1100C810	TEMPMONINTSTS	32	Temperature Monitoring Interrupt Status
1100C814	TEMPMONIDET0	32	Sensing Point 0 Temperature Monitoring Detection
1100C818	TEMPMONIDET1	32	Sensing Point 1 Temperature Monitoring Detection
1100C81C	TEMPMONIDET2	32	Sensing Point 2 Temperature Monitoring Detection
1100C824	TEMPH2NTHRE	32	Temperature HOT2NORMAL Threshold
1100C828	TEMPHTHRE	32	Temperature Hot Threshold
1100C82C	TEMPCTHRE	32	Temperature Cold Threshold
1100C830	TEMPOFFSETH	32	Temperature High Offset Threshold
1100C834	TEMPOFFSETL	32	Temperature Low Offset Threshold
1100C838	TEMPMSRCTL0	32	Temperature Measure Control 0
1100C83C	TEMPMSRCTL1	32	Temperature Measure Control 1
1100C840	TEMPAHBPOLL	32	Temperature AHB Polling
1100C844	TEMPAHBTO	32	Temperature AHB Polling Timeout
1100C848	TEMPADCPNP0	32	ADC Mux Selection Value
1100C84C	TEMPADCPNP1	32	ADC Mux Selection Value
1100C850	TEMPADCPNP2	32	ADC Mux Selection Value
1100C854	TEMPADCMUX	32	ADC Mux Selection
1100C858	TEMPADCEXT	32	ADC Extra Write
1100C85C	TEMPADCEXT1	32	ADC Extra Write 1
1100C860	TEMPADCEN	32	ADC Enable
1100C864	TEMPPNPMUXADDR	32	PNP Mux Selection Address
1100C868	TEMPADCMUXADDR	32	ADC Mux Selection Address
1100C86C	TEMPADCEXTADDR	32	ADC Extra Write Address
1100C870	TEMPADCEXT1ADDR	32	ADC Extra Write Address 1
1100C874	TEMPADCENADDR	32	ADC Enable Address
1100C878	TEMPADCVALIDADDR	32	ADC Voltage Valid Reading Address
1100C87C	TEMPADCVOLTADDR	32	ADC Voltage Reading Address
1100C880	TEMPRDCTRL	32	ADC Voltage Read Control
1100C884	TEMPADCVALIDMASK	32	ADC Valid Mask
1100C888	TEMPADCVOLTAGESHIFT	32	ADC Voltage Shift
1100C88C	TEMPADCWRITECTRL	32	ADC Write Control
1100C890	TEMPMSR0	32	Temperature Measure Reading 0
1100C894	TEMPMSR1	32	Temperature Measure Reading 1
1100C898	TEMPMSR2	32	Temperature Measure Reading 2
1100C89C	TEMPADCHADDR	32	ADC Voltage Reading Address
1100C8A0	TEMPIMMD0	32	Temperature IMMD Measure Reading 0
1100C8A4	TEMPIMMD1	32	Temperature IMMD Measure Reading 1
1100C8A8	TEMPIMMD2	32	Temperature IMMD Measure Reading 2
1100C8B0	TEMPMONIDET3	32	Sensing Point 3 Temperature Monitoring Detection
1100C8B4	TEMPADCPNP3	32	ADC Mux Selection Value
1100C8B8	TEMPMSR3	32	Temperature Measure Reading 3
1100C8BC	TEMPIMMD3	32	Temperature IMMD Measure Reading 3
1100C8C0	TEMPPROTCTL	32	Thermal Protection Sensor Selection
1100C8C4	TEMPPROTTA	32	Temperature Protection Stage 1
1100C8C8	TEMPPROTTB	32	Temperature Protection Stage 2

Address	Name	Width	Register Function
1100C8CC	**TEMPPROTTC**	32	Temperature Protection Stage 3
1100C8F0	**TEMPSPARE0**	32	Spare Register for Debug 0
1100C8F4	**TEMPSPARE1**	32	Spare Register for Debug 1
1100C8F8	**TEMPSPARE2**	32	Spare Register for Debug 2
1100C8FC	**TEMPSPARE3**	32	REV_ID

1100C800 TEMPMONCTL0 Temperature Monitoring Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SENSE3_EN	SENSE2_EN	SENSE1_EN	SENSE0_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	SENSE3_EN	**Enables periodic temperature measurement on sensing point 2** 0: Disable 1: Enable
2	SENSE2_EN	**Enables periodic temperature measurement on sensing point 2** 0: Disable 1: Enable
1	SENSE1_EN	**Enables periodic temperature measurement on sensing point 1** 0: Disable 1: Enable
0	SENSE0_EN	**Enables periodic temperature measurement on sensing point 0** 0: Disable 1: Enable

1100C804 TEMPMONCTL1 Temperature Monitoring Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																HOTINT_SEL3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HOTINT_SEL2	HOTINT_SEL1	HOTINT_SEL0				PERIOD_UNIT									
Type	RW	RW	RW				RW									
Reset	0	0	0				0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	HOTINT_SEL3	**Selects hot interrupt for sensing point 2** 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
15	HOTINT_SEL2	**Selects hot interrupt for sensing point 2** 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
14	HOTINT_SEL1	**Selects hot interrupt for sensing point 1** 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
13	HOTINT_SEL0	**Selects hot interrupt for sensing point 0** 0: All when normal to over hot threshold 1: Only the first time when normal to over hot threshold
9:0	PERIOD_UNIT	**Calculating period unit in bus clock with x256 scaling-up (i.e. period_unit*bus_clock_period*256)**

1100C808 **TEMPMONCTL2** **Temperature Monitoring Control 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FILT_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SEN_INTRVAL									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:16	FILT_INTRVAL	**Interval unit in PERIOD_UNIT (between each sample within the same sensing point)**
9:0	SEN_INTRVAL	**Interval unit in PERIOD_UNIT (between sensing points)**

1100C80C **TEMPMONINT** **Temperature Monitoring Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_EN	STAGE2_INT_EN	STAGE1_INT_EN	FILTER_INT_EN_3	IMMD_INT_EN_3	NOHOTINTEN3	HOFSINTEN3	LOFSINTEN3	HINTEN3	CINTEN3	FILTER_INT_EN_2	FILTER_INT_EN_1	FILTER_INT_EN_0	IMMD_INT_EN_2	IMMD_INT_EN_1	IMMD_INT_EN_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIME_OUT_INT_EN	NOHOTINTEN2	HOFSINTEN2	LOFSINTEN2	HINTEN2	CINTEN2	NOHOTINTEN1	HOFSINTEN1	LOFSINTEN1	HINTEN1	CINTEN1	NOHOTINTEN0	HOFSINTEN0	LOFSINTEN0	HINTEN0	CINTEN0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STAGE3_INT_EN	**Enables interrupt for thermal protection stage 3** 0: Disable 1: Enable
30	STAGE2_INT_EN	**Enables interrupt for thermal protection stage 2** 0: Disable 1: Enable
29	STAGE1_INT_EN	**Enables interrupt for thermal protection stage 1** 0: Disable 1: Enable
28	FILTER_INT_EN_3	**Enables filter sense interrupt for sensing point 2** 0: Disable 1: Enable
27	IMMD_INT_EN_3	**Enables immediate sense interrupt for sensing point 2** 0: Disable 1: Enable
26	NOHOTINTEN3	**Enables hot to normal interrupt for sensing point 3** 0: Disable 1: Enable
25	HOFSINTEN3	**Enables high offset interrupt for sensing point 3** 0: Disable 1: Enable
24	LOFSINTEN3	**Enables low offset interrupt for sensing point 3** 0: Disable

Bit(s)	Name	Description
		1: Enable
23	HINTEN3	**Enables hot threshold interrupt for sensing point 3** 0: Disable 1: Enable
22	CINTEN3	**Enables cold threshold interrupt for sensing point 3** 0: Disable 1: Enable
21	FILTER_INT_EN_2	**Enables filter sense interrupt for sensing point 2** 0: Disable 1: Enable
20	FILTER_INT_EN_1	**Enables filter sense interrupt for sensing point 1** 0: Disable 1: Enable. This register is fixed at 0 when RTC_POWERKEY1 and RTC_POWERKEY2 unmatch the correct values.
19	FILTER_INT_EN_0	**Enables filter sense interrupt for sensing point 0** 0: Disable 1: Enable
18	IMMD_INT_EN_2	**Enables immediate sense interrupt for sensing point 2** 0: Disable 1: Enable
17	IMMD_INT_EN_1	**Enables immediate sense interrupt for sensing point 1** 0: Disable 1: Enable
16	IMMD_INT_EN_0	**Enables immediate sense interrupt for sensing point 0** 0: Disable 1: Enable. This register activates or deactivates IRQ generation when the TC counter reaches its maximum value.
15	TIME_OUT_INT_EN	**Enables AHB polling temperature timeout interrupt** 0: Disable 1: Enable
14	NOHOTINTEN2	**Enables hot to normal interrupt for sensing point 2** 0: Disable 1: Enable

Bit(s)	Name	Description
13	HOFSINTEN2	**Enables high offset interrupt for sensing point 2** 0: Disable 1: Enable
12	LOFSINTEN2	**Enables low offset interrupt for sensing point 2** 0: Disable 1: Enable
11	HINTEN2	**Enables hot threshold interrupt for sensing point 2** 0: Disable 1: Enable
10	CINTEN2	**Enables cold threshold interrupt for sensing point 2** 0: Disable 1: Enable
9	NOHOTINTEN1	**Enables hot to normal interrupt for sensing point 1** 0: Disable 1: Enable
8	HOFSINTEN1	**Enables high offset interrupt for sensing point 1** 0: Disable 1: Enable
7	LOFSINTEN1	**Enables low offset interrupt for sensing point 1** 0: Disable 1: Enable
6	HINTEN1	**Enables hot threshold interrupt for sensing point 1** The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in this register is masked. Warning: If you set all bits to 1 in RTC_AL_MASK (i.e. RTC_AL_MASK = 0x7f) and PWREN = 1 in RTC_BBPU, the alarm will come every second, not disabled. 0: Disable 1: Enable
5	CINTEN1	**Enables cold threshold interrupt for sensing point 1** 0: Disable 1: Enable
4	NOHOTINTEN0	**Enables hot to normal interrupt for sensing point 0** 0: Disable

Bit(s)	Name	Description
		1: Enable
3	HOFSINTEN0	**Enables high offset interrupt for sensing point 0** 0: Disable 1: Enable
2	LOFSINTEN0	**Enables low offset interrupt for sensing point 0** 0: Disable 1: Enable
1	HINTEN0	**Enables hot threshold interrupt for sensing point 0** 0: Disable 1: Enable
0	CINTEN0	**Enables cold threshold interrupt for sensing point 0** 0: Disable 1: Enable

1100C810 TEMPMONINTSTS Temperature Monitoring Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAGE3_INT_STAT	STAGE2_INT_STAT	STAGE1_INT_STAT	FILTER_INT_STAT_3	IMMD_INT_STAT_3	NOHOTINTSTS3	HOFSINTSTS3	LOFSINTSTS3	HINTSTS3	LINTSTS3	FILTER_INT_STAT_2	FILTER_INT_STAT_1	FILTER_INT_STAT_0	IMMD_INT_STAT_2	IMMD_INT_STAT_1	IMMD_INT_STAT_0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMEOUTINTSTS	NOHOTINTSTS2	HOFSINTSTS2	LOFSINTSTS2	HINTSTS2	LINTSTS2	NOHOTINTSTS1	HOFSINTSTS1	LOFSINTSTS1	HINTSTS1	LINTSTS1	NOHOTINTSTS0	HOFSINTSTS0	LOFSINTSTS0	HINTSTS0	LINTSTS0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STAGE3_INT_STAT	**Interrupt status for thermal protection stage 3** 0: Disable 1: Enable
30	STAGE2_INT_STAT	**Interrupt status for thermal protection stage 2** 0: Disable 1: Enable
29	STAGE1_INT_STAT	**Interrupt status for thermal protection stage 1** 0: Disable 1: Enable
28	FILTER_INT_STAT_3	**Filter sense interrupt status for sensing point 3** 0: Disable 1: Enable
27	IMMD_INT_STAT_3	**Immediate sense interrupt status for sensing point 3** 0: Disable 1: Enable
26	NOHOTINTSTS3	**Hot to normal interrupt status for sensing point 3** 0: No interrupt 1: Interrupt exists.
25	HOFSINTSTS3	**High offset interrupt status for sensing point 3** 0: No interrupt 1: Interrupt exists.
24	LOFSINTSTS3	**Low offset interrupt status for sensing point 3** 0: No interrupt

Bit(s)	Name	Description
		1: Interrupt exists.
23	HINTSTS3	**Hot threshold interrupt status for sensing point 3** 0: No interrupt 1: Interrupt exists.
22	LINTSTS3	**Cold threshold interrupt status for sensing point 3** 0: No interrupt 1: Interrupt exists.
21	FILTER_INT_STAT_2	**Filter sense interrupt status for sensing point 2** 0: Disable 1: Enable
20	FILTER_INT_STAT_1	**Filter sense interrupt status for sensing point 1** 0: Disable 1: Enable
19	FILTER_INT_STAT_0	**Filter sense interrupt status for sensing point 0** 0: Disable 1: Enable
18	IMMD_INT_STAT_2	**Immediate sense interrupt status for sensing point 2** 0: Disable 1: Enable
17	IMMD_INT_STAT_1	**Immediate sense interrupt status for sensing point 1** 0: Disable 1: Enable
16	IMMD_INT_STAT_0	**Immediate sense interrupt status for sensing point 0** 0: Disable 1: Enable
15	TIMEOUTINTSTS	**AHB polling ADC result timeout interrupt status** 0: No interrupt 1: Interrupt exists.
14	NOHOTINTSTS2	**High to normal offset interrupt status for sensing point 2** 0: No interrupt 1: Interrupt exists.
13	HOFSINTSTS2	**High offset interrupt status for sensing point 2**

Bit(s)	Name	Description
		0: No interrupt
		1: Interrupt exists.
12	LOFSINTSTS2	**Low offset interrupt status for sensing point 2**
		0: No interrupt
		1: Interrupt exists.
11	HINTSTS2	**Hot threshold interrupt status for sensing point 2**
		0: No interrupt
		1: Interrupt exists.
10	LINTSTS2	**Cold threshold interrupt status for sensing point 2**
		0: No interrupt
		1: Interrupt exists.
9	NOHOTINTSTS1	**Hot to normal interrupt status for sensing point 1**
		0: No interrupt
		1: Interrupt exists.
8	HOFSINTSTS1	**High offset interrupt status for sensing point 1**
		0: No interrupt
		1: Interrupt exists.
7	LOFSINTSTS1	**Low offset interrupt status for sensing point 1**
		0: No interrupt
		1: Interrupt exists.
6	HINTSTS1	**Hot threshold interrupt status for sensing point 1**
		0: No interrupt
		1: Interrupt exists.
5	LINTSTS1	**Cold threshold interrupt status for sensing point 1**
		0: No interrupt
		1: Interrupt exists.
4	NOHOTINTSTS0	**Hot to normal interrupt status for sensing point 0**
		0: No interrupt
		1: Interrupt exists.
3	HOFSINTSTS0	**High offset interrupt status for sensing point 0**
		0: No interrupt
		1: Interrupt exists.

Bit(s)	Name	Description
2	LOFSINTSTS0	**Low offset interrupt status for sensing point 0** 0: No interrupt 1: Interrupt exists.
1	HINTSTS0	**Hot threshold interrupt status for sensing point 0** 0: No interrupt 1: Interrupt exists.
0	LINTSTS0	**Cold threshold interrupt status for sensing point 0** 0: No interrupt 1: Interrupt exists.

1100C814 **TEMPMONIDET0** **Sensing Point 0 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	**Times for hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	**Times for high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	**Times for low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	**Times for hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	**Times for cold threshold interrupt occurrence** 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100C818 TEMPMONIDET1 Sensing Point 1 Temperature Monitoring Detection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	**Times for hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	**Times for high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	**Times for low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	**Times for hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	**Times for cold threshold interrupt occurrence** 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100C81C **TEMPMONIDET2** **Sensing Point 2 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	**Times for hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	**Times for high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	**Times for low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	**Times for hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	**Times for cold threshold interrupt occurrence** 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100C824 TEMPH2NTHRE Temperature HOT2NORMAL Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HOT2NORMAL_THRE											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	HOT2NORMAL_THRE	**Threshold for hot to normal**

1100C828 **TEMPHTHRE** **Temperature Hot Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HOT_THRE											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	HOT_THRE	**Threshold for hot temperature**

1100C82C **TEMPCTHRE** **Temperature Cold Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**COLD_THRE**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	COLD_THRE	**Threshold for cold temperature**

1100C830 TEMPOFFSETH Temperature High Offset Threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					HIGH_OFFSET											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	HIGH_OFFSET	**Hight offset for monitoring temperature**

1100C834 **TEMPOFFSETL** **Temperature Low Offset Threshold** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**LOW_OFFSET**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	LOW_OFFSET	**Low offset for monitoring temperature**

1100C838 TEMPMSRCTL0 Temperature Measure Control 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					MSRCTL3			MSRCTL2			MSRCTL1			MSRCTL0		
Type					RW			RW			RW			RW		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	MSRCTL3	**Temperature measurement control for sensing point 3** 000: 1 sampling 001: Average 2 samplings 010: 4 samplings, drop max. and min. then average 2 samples 011: 6 samplings, drop max. and min. then average 4 samples 100: 10 samplings, drop max. and min. then average 8 samples 101: 18 samplings, drop max. and min. then average 16 samples Others: 1 sampling
8:6	MSRCTL2	**Temperature measurement control for sensing point 2** 000: 1 sampling 001: Average 2 samplings 010: 4 samplings, drop max. and min. then average 2 samples 011: 6 samplings, drop max. and min. then average 4 samples 100: 10 samplings, drop max. and min. then average 8 samples 101: 18 samplings, drop max. and min. then average 16 samples Others: 1 sampling
5:3	MSRCTL1	**Temperature measurement control for sensing point 1** 000: 1 sampling 001: Average 2 samplings 010: 4 samplings, drop max. and min. then average 2 samples 011: 6 samplings, drop max. and min. then average 4 samples 100: 10 samplings, drop max. and min. then average 8 samples 101: 18 samplings, drop max. and min. then average 16 samples Others: 1 sampling

Bit(s)	Name	Description
2:0	MSRCTL0	**Temperature measurement control for sensing point 0** 000: 1 sampling 001: Average 2 samplings 010: 4 samplings, drop max. and min. then average 2 samples 011: 6 samplings, drop max. and min. then average 4 samples 100: 10 samplings, drop max. and min. then average 8 samples 101: 18 samplings, drop max. and min. then average 16 samples Others: 1 sampling

1100C83C **TEMPMSRCTL1** **Temperature Measure Control 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MSR3IMM	PAUSE3	MSRSTS1	MSR2IMM	MSR1IMM	MSR0IMM	PAUSE2	PAUSE1	PAUSE0	MSRSTS0
Type							RW	RW	RO	RW	RW	RW	RW	RW	RW	RO
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	MSR3IMM	**Sensing point 3 immediate measurement disregards TEMPMONCTL0.** 0: Disable 1: Enable
8	PAUSE3	**Pauses periodic temperature measurement for sensing point 3** 0: Release pause 1: Pause
7	MSRSTS1	**Temperature measurement bus status[1]** 00: IDLE 01: Write transaction 10: Read transaction 11: Waiting for read after write
6	MSR2IMM	**Sensing point 2 immediate measurement disregards TEMPMONCTL0.** 0: Disable 1: Enable
5	MSR1IMM	**Sensing point 1 immediate measurement disregards TEMPMONCTL0.** 0: Disable 1: Enable
4	MSR0IMM	**Sensing point 0 immediate measurement disregards TEMPMONCTL0.** 0: Disable 1: Enable
3	PAUSE2	**Pauses periodic temperature measurement for sensing point 2** 0: Release pause 1: Pause
2	PAUSE1	**Pauses periodic temperature measurement for sensing point 1**

Bit(s)	Name	Description
		0: Release pause
		1: Pause
1	PAUSE0	**Pauses periodic temperature measurement for sensing point 0**
		0: Release pause
		1: Pause
0	MSRSTS0	**Temperature measurement bus status[0]**
		00: IDLE
		01: Write transaction
		10: Read transaction
		11: Waiting for read after write

1100C840 TEMPAHBPOLL Temperature AHB Polling 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_POLL_INTVL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_POLL_INTVL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_POLL_INTVL	**Time interval for AHB polling the temperature voltage from AUXADC** Unit: AHB clock

1100C844 **TEMPAHBTO** **Temperature AHB Polling Timeout** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_TIMEOUT															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_TIMEOUT															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	ADC_TIMEOUT	**Timeout time for AHB polling the temperature voltage from AUXADC without getting any response** Unit: slow_clk period

1100C848 TEMPADCPNP0 ADC Mux Selection Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TEMPADCPNP0	**HW will automatically switch the AUXADC mux with this value for PNP 0.**

1100C84C **TEMPADCPNP1** **ADC Mux Selection Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TEMPADCPNP1	**HW will automatically switch the AUXADC mux with this value for PNP 1.**

1100C850 TEMPADCPNP2 ADC Mux Selection Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TEMPADCPNP2	**HW will automatically switch the AUXADC mux with this value for PNP 2.**

1100C854 **TEMPADCMUX** **ADC Mux Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_MUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_MUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_MUX	**AHB value for AUXADC mux selection**

1100C858 TEMPADCEXT ADC Extra Write 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_EXT	**AHB value for AUXADC extra write access**

1100C85C TEMPADCEXT1 ADC Extra Write 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_EXT1	**AHB value for AUXADC extra write access 1**

1100C860 **TEMPADCEN** **ADC Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_EN	**Enables AHB value for AUXADC**

1100C864 **TEMPPNPMUXADDR** **PNP Mux Selection Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_PNP_MUX_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_PNP_MUX_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_PNP_MUX_ADDR	**AHB address for PNP sensor mux selection**

1100C868 TEMPADCMUXADDR ADC Mux Selection Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_MUX_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_MUX_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_MUX_ADDR	**AHB address for AUXADC mux selection**

1100C86C TEMPADCEXTADDR ADC Extra Write Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_EXT_ADDR	**AHB address for AUXADC extra write access**

1100C870 TEMPADCEXT1ADDR ADC Extra Write Address 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EXT1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EXT1_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_EXT1_ADDR	**AHB address for AUXADC extra write access 1**

1100C874 **TEMPADCENADDR** **ADC Enable Address** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_EN_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_EN_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_EN_ADDR	**AHB address for AUXADC enable**

1100C878 TEMPADCVALIDADDR ADC Voltage Valid Reading Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_VALID_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_VALID_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_VALID_ADDR	**AHB address for AUXADC valid bit**

1100C87C TEMPADCVOLTADDR ADC Voltage Reading Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADC_VOLT_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_VOLT_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADC_VOLT_ADDR	**AHB address for AUXADC voltage output**

1100C880 **TEMPRDCTRL** **ADC Voltage Read Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RD_CTRL_DIFF
Type																RW
Reset																0

Bit(s)	Name	Description
0	RD_CTRL_DIFF	0: Read valid and voltage are at the same register. 1: Read valid and voltage are at different registers.

1100C884 **TEMPADCVALIDMASK** **ADC Valid Mask** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**ADC_RD_VALID_POLARITY**	**ADC_RD_VALID_POS_**				
Type											RW	RW				
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	ADC_RD_VALID_POLARITY	0: Valid bit is active low. 1: Valid bit is active high.
4:0	ADC_RD_VALID_POS_	**Indicates where the valid bit is in a register**

1100C888 TEMPADCVOLTAGESHIFT ADC Voltage Shift 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**ADC_VOLTAGE_SHIFT**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	ADC_VOLTAGE_SHIFT	**If voltage is at [16:5], this register should be set to 5.** Default: 0

1100C88C **TEMPADCWRITECTRL** **ADC Write Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**ADC_EXTRA1_WRITE**	**ADC_EXTRA_WRITE**	**ADC_MUX_WRITE**	**ADC_PNP_WRITE**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	ADC_EXTRA1_WRITE	**Enables adc_extra1_write address**
2	ADC_EXTRA_WRITE	**Enables adc_extra_write address**
1	ADC_MUX_WRITE	**Enables adc_mux_write address**
0	ADC_PNP_WRITE	**Enables adc_pnp_write address**

1100C890 TEMPMSR0 Temperature Measure Reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID0				MSRREADING0											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	MSRVALID0	**Temperature measurement reading valid of sensing point 0**
11:0	MSRREADING0	**Temperature measurement reading of sensing point 0**

1100C894 TEMPMSR1 Temperature Measure Reading 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID1				MSRREADING1											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	MSRVALID1	**Temperature measurement reading valid of sensing point 1**
11:0	MSRREADING1	**Temperature measurement reading of sensing point 1**

1100C898 **TEMPMSR2** **Temperature Measure Reading 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID2				MSRREADING2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	MSRVALID2	**Temperature measurement reading valid of sensing point 2**
11:0	MSRREADING2	**Temperature measurement reading of sensing point 2**

1100C89C TEMPADCHADDR ADC Voltage Reading Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ADC_HADDR	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	ADC_HADDR	**AHB higher bits address (bit34-33)**

1100C8A0 TEMPIMMD0 Temperature IMMD Measure Reading 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID0				IMMDMSRREADING0											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	IMMDMSRVALID0	**Immediate temperature measurement reading valid of sensing point 0**
11:0	IMMDMSRREADING0	**Immediate temperature measurement reading of sensing point 0**

1100C8A4 TEMPIMMD1 Temperature IMMD Measure Reading 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID1				IMMDMSRREADING1											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	IMMDMSRVALID1	**Immediate temperature measurement reading valid of sensing point 1**
11:0	IMMDMSRREADING1	**Immediate temperature measurement reading of sensing point 1**

1100C8A8 TEMPIMMD2 Temperature IMMD Measure Reading 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID2				IMMDMSRREADING2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	IMMDMSRVALID2	**Immediate temperature measurement reading valid of sensing point 2**
11:0	IMMDMSRREADING2	**Immediate temperature measurement reading of sensing point 2**

1100C8B0 **TEMPMONIDET3** **Sensing Point 3 Temperature Monitoring Detection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							NOHOTIMES		HOTIMES		LOTIMES		HTIMES		CTIMES	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	NOHOTIMES	**Times for hot to normal interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
7:6	HOTIMES	**Times for high offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
5:4	LOTIMES	**Times for low offset interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
3:2	HTIMES	**Times for hot threshold interrupt occurrence** 00: 1 01: 2 10: 3 11: 4
1:0	CTIMES	**Times for cold threshold interrupt occurrence** 00: 1 01: 2 10: 3

Bit(s)	Name	Description
		11: 4

1100C8B4 TEMPADCPNP3 ADC Mux Selection Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEMPADCPNP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPADCPNP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TEMPADCPNP3	**HW will automatically switch the AUXADC mux with this value for PNP 3.**

1100C8B8 TEMPMSR3 Temperature Measure Reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSRVALID3				MSRREADING3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	MSRVALID3	**Temperature measurement reading valid of sensing point 3**
11:0	MSRREADING3	**Temperature measurement reading of sensing point 3**

1100C8BC TEMPIMMD3 Temperature IMMD Measure Reading 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IMMDMSRVALID3				IMMDMSRREADING3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	IMMDMSRVALID3	**Immediate temperature measurement reading valid of sensing point 3**
11:0	IMMDMSRREADING3	**Immediate temperature measurement reading of sensing point 3**

1100C8C0 TEMPPROTCTL Thermal Protection Sensor Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													PROTSELECTION		PROTSTRATEGY	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PROTOFFSET											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	PROTSELECTION	00: Sensing point 0 01: Sensing point 1 10: Sensing point 2 11: Sensing point 3
17:16	PROTSTRATEGY	00: Average of 4 sensing points 01: Max. of 4 sensing points 10: Selected sensing point 11: Reserved
11:0	PROTOFFSET	**Thermal protection temperature offset**

1100C8C4 **TEMPPROTTA** **Temperature Protection Stage 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PROTSTAGE1THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	PROTSTAGE1THRES	**Thermal protection stage 1 threshold**

1100C8C8 TEMPPROTTB Temperature Protection Stage 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PROTSTAGE2THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	PROTSTAGE2THRES	**Thermal protection stage 2 threshold**

1100C8CC **TEMPPROTTC** **Temperature Protection Stage 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PROTSTAGE3THRES											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	PROTSTAGE3THRES	**Thermal protection stage 3 threshold**

1100C8F0 TEMPSPARE0 Spare Register for Debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE0	**Debug register 0**

1100C8F4 **TEMPSPARE1** **Spare Register for Debug 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE1	**Debug register 1**

1100C8F8 **TEMPSPARE2** **Spare Register for Debug 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPARE2	**Debug register 2**

1100C8FC TEMPSPARE3 REV_ID 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPARE3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPARE3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:0	SPARE3	**REV_ID**

3 General System

3.1 System Timer (sys_timer)

3.1.1 Register Definition

Module name: sys_timer Base address: (+0x1001_7000)

Address	Name	Width	Register Function
10017000	CNTCR	32	System Counter Control Register
10017004	CNTSR	32	System Counter Status Register
10017008	CNTCV_L	32	System Counter Count Value Low
1001700C	CNTCV_H	32	System Counter Count Value High
10017010	CNTWACR	32	System Counter Write Access Control Register
10017014	CNTRACR	32	System Counter Read Access Control Register
10017018	CNTACR_LOCK	32	System Counter Access Control Lock Register
1001701C	CHICKEN	32	Spare Register
10017020	CNTFID0	32	System Counter Frequency Table Entry 0
10017024	CNTFID1	32	System Counter Frequency Table Entry 1
10017028	CNTFID2	32	System Counter Frequency Table Entry 2
1001702C	CNTFIDE	32	System Counter frequency Table Entry End of Line
10017030	VERSION	32	Version of System Timer
10017034	CNTR_32K_L	32	Low Part of 64-bit 32K Counter
10017038	CNTR_32K_H	32	High Part of 64-bit 32K Counter
1001703C	CNT_RCON	32	Latch-Value Read Control Register
10017040	CNTTVAL0_CON	32	System Counter Timer 0 Control Register
10017044	CNTTVAL0	32	System Counter Timer 0 Value Register
10017048	CNTTVAL1_CON	32	System Counter Timer 1 Control Register
1001704C	CNTTVAL1	32	System Counter Timer 1 Value Register
10017050	CNTTVAL2_CON	32	System Counter Timer 2 Control Register
10017054	CNTTVAL2	32	System Counter Timer 2 Value Register
10017058	CNTTVAL3_CON	32	System Counter Timer 3 Control Register
1001705C	CNTTVAL3	32	System Counter Timer 3 Value Register
10017060	CNTTVAL4_CON	32	System Counter Timer 4 Control Register
10017064	CNTTVAL4	32	System Counter Timer 4 Value Register
10017068	CNTTVAL5_CON	32	System Counter Timer 5 Control Register
1001706C	CNTTVAL5	32	System Counter Timer 5 Value Register
10017070	CNTTVAL6_CON	32	System Counter Timer 6 Control Register
10017074	CNTTVAL6	32	System Counter Timer 6 Value Register
10017078	CNTTVAL7_CON	32	System Counter Timer 7 Control Register
1001707C	CNTTVAL7	32	System Counter Timer 7 Value Register
10017080	DOMAIN_DIS	32	Domain Disable
10017084	DOMAIN_VAL	32	Domain Value
10017090	CNTRV_L_0	32	Low-32-bit Timer Value Set 0
10017094	CNTRV_H_0	32	High-32-bit Timer Value Set 0
10017098	CNTRV_L_1	32	Low-32-bit Timer Value Set 1
1001709C	CNTRV_H_1	32	High-32-bit Timer Value Set 1
100170A0	CNTRV_L_2	32	Low-32-bit Timer Value Set 2
100170A4	CNTRV_H_2	32	High-32-bit Timer Value Set 2
100170A8	CNTRV_L_3	32	Low-32-bit Timer Value Set 3
100170AC	CNTRV_H_3	32	High-32-bit Timer Value Set 3
100170B0	CNTRV_L_4	32	Low-32-bit Timer Value Set 4
100170B4	CNTRV_H_4	32	High-32-bit Timer Value Set 4
100170B8	CNTRV_L_5	32	Low-32-bit Timer Value Set 5

Address	Name	Width	Register Function
100170BC	CNTRV_H_5	32	High-32-bit Timer Value Set 5
100170C0	CNTRV_L_6	32	Low-32-bit Timer Value Set 6
100170C4	CNTRV_H_6	32	High-32-bit Timer Value Set 6
100170C8	CNTRV_L_7	32	Low-32-bit Timer Value Set 7
100170CC	CNTRV_H_7	32	High-32-bit Timer Value Set 7

10017000 CNTCR System Counter Control Register 00001815

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R_32K_DEBEN														
Type		RW														
Reset		0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			KP_LSB9b_EN	COMP_25_EN	COMP_20_EN	COMP_15_EN							TIE_0_EN	CNT_32K_AS_EN	HDBG_EN	CNT_EN
Type			RW	RW	RW	RW							RW	RW	RW	RW
Reset			0	1	1	0							0	1	0	1

Bit(s)	Name	Description
30	R_32K_DEBEN	**Enable to read 32K counter for debugging** 0: Disable 1: Enable
13	KP_LSB9b_EN	**The 10 LSBs will be kept 0 when the clock switches to 32 KHz if this bit is set.** 0: Disable 1: Enable
12	COMP_25_EN	**v2.5 solves dis-continuity of v2.0.** v2.5 and v2.0 need to be enabled together. v2.0 can be enabled alone. 0: Disable 1: Enable
11	COMP_20_EN	**v2.0 is only based on 32K to tick sys_timer.** However, this architecture causes dis-continuity of sys_timer value. Some v8.0 CPUs need continuous values. HPT implements an option to eliminate this limitation in some v8.0 CPUs and all v8.2 CPUs. 0: Disable 1: Enable
10	COMP_15_EN	**v1.5 is based on 13M and 32K to tick sys_timer.** 0: Disable 1: Enable
3	TIE_0_EN	**No need to enable it when v2.5 is enabled** 0: Disable 1: Enable
2	CNT_32K_AS_EN	**Enables 32K auto-switch function of system timer counter** 0: Disable

Bit(s)	Name	Description
		1: Enable
1	HDBG_EN	**Enables halt-on debug function of system timer counter** 0: Disable 1: Enable
0	CNT_EN	**Enables system timer counter** 0: Disable 1: Enable

10017004 CNTSR System Counter Status Register 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**clk_sel**									**DBGACK**	
Type						RO									RO	
Reset						0									0	

Bit(s)	Name	Description
10	clk_sel	**Selects system timer frequency** 0: 26M 1: 32K
1	DBGACK	**Timer is halted in debug mode.** 0: Run 1: Halt

10017008 CNTCV_L System Counter Count Value Low 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTCV_L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTCV_L															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTCV_L	**Low part of 64-bit system timer counter**

1001700C CNTCV_H System Counter Count Value High 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTCV_H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTCV_H															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTCV_H	**High part of 64-bit system timer counter**

10017010 CNTWACR System Counter Write Access Control Register 0000FFF0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTWACR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTWACR															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	CNTWACR	**Configures write access permission for each register** Bit0: CNTCR Bit1: CNTSR Bit2: CNTCV_L Bit3: CNTCV_H Bit8: CNTFID0 Bit9: CNTFID1 Bit10: CNTFID2 Bit11: CNTFIDE Bit16: CNTTVAL0_CON & CNTTVAL0 Bit17: CNTTVAL1_CON & CNTTVAL1 Bit18: CNTTVAL2_CON & CNTTVAL2 Bit19: CNTTVAL3_CON & CNTTVAL3 Bit20: CNTTVAL4_CON & CNTTVAL4 Bit21: CNTTVAL5_CON & CNTTVAL5 Bit22: CNTTVAL6_CON & CNTTVAL6 Bit23: CNTTVAL7_CON & CNTTVAL7 Bit24: CNTTVAL8_CON & CNTTVAL8 Bit25: CNTTVAL9_CON & CNTTVAL9 0: Disable NS access 1: Enable NS access

10017014 CNTRACR System Counter Read Access Control Register 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTWACR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTWACR															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	CNTWACR	**Configures read access permission for each register** Bit0: CNTCR Bit1: CNTSR Bit2: CNTCV_L Bit3: CNTCV_H Bit8: CNTFID0 Bit9: CNTFID1 Bit10: CNTFID2 Bit11: CNTFIDE Bit16: CNTTVAL0_CON & CNTTVAL0 Bit17: CNTTVAL1_CON & CNTTVAL1 Bit18: CNTTVAL2_CON & CNTTVAL2 Bit19: CNTTVAL3_CON & CNTTVAL3 Bit20: CNTTVAL4_CON & CNTTVAL4 Bit21: CNTTVAL5_CON & CNTTVAL5 Bit22: CNTTVAL6_CON & CNTTVAL6 Bit23: CNTTVAL7_CON & CNTTVAL7 Bit24: CNTTVAL8_CON & CNTTVAL8 Bit25: CNTTVAL9_CON & CNTTVAL9 0: Disable NS access 1: Enable NS access

10017018 CNTACR_LOCK System Counter Access Control Lock Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTACR_LOCK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTACR_LOCK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTACR_LOCK	**Locks corresponding CNTRACR and CNTWACR bits** This bit can program once only. 0: Unlock 1: Lock

1001701C CHICKEN Spare Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHICKEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHICKEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CHICKEN	**Spare register**

10017020 CNTFID0 System Counter Frequency Table Entry 0 018CBA80

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFID0															
Type	RO															
Reset	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFID0															
Type	RO															
Reset	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFID0	**Frequency table entry 0**

10017024 CNTFID1 System Counter Frequency Table Entry 1 00C65D40

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFID1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFID1															
Type	RO															
Reset	0	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFID1	**Frequency table entry 1**

10017028 CNTFID2 System Counter Frequency Table Entry 2 00632EA0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFID2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFID2															
Type	RO															
Reset	0	0	1	0	1	1	1	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFID2	**Frequency table entry 2**

1001702C **CNTFIDE** **System Counter frequency Table Entry End of Line** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTFIDE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTFIDE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTFIDE	**Frequency table entry - end of line**

10017030 VERSION Version of System Timer 00000209

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VERSION															
Type	RO															
Reset	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1

Bit(s)	Name	Description
15:0	VERSION	**Version of System Timer**

10017034 CNTR_32K_L Low Part of 64-bit 32K Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTR_32K_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTR_32K_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTR_32K_L	Low part of 32K counter

10017038 CNTR_32K_H High Part of 64-bit 32K Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTR_32K_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTR_32K_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTR_32K_H	High part of 32K counter

1001703C CNT_RCON Latch-Value Read Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNT_RCON															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNT_RCON															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNT_RCON	0: Disable 1: Enable

10017040 CNTTVAL0_CON System Counter Timer 0 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ0_STA**			**IRQ0_EN**	**CNTTVAL0_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ0_STA	**Enables system timer 0 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ0_EN	**Enables system timer 0 interrupt** 0: Disable 1: Enable
0	CNTTVAL0_EN	**Enables system timer 0** 0: Disable 1: Enable

10017044 CNTTVAL0 System Counter Timer 0 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL0	**System timer 0 down counter** Write to set up timeout value; read as 32-bit down counter.

10017048 CNTTVAL1_CON System Counter Timer 1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ1_STA**			**IRQ1_EN**	**CNTTVAL1_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ1_STA	**Enables system timer 1 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ1_EN	**Enable system timer 1 interrupt** 0: Disable 1: Enable
0	CNTTVAL1_EN	**Enable system timer 1** 0: Disable 1: Enable

1001704C CNTTVAL1 System Counter Timer 1 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL1	**System timer 1 down counter** Write to set up timeout value; read as 32-bit down counter.

10017050 CNTTVAL2_CON System Counter Timer 2 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ2_STA**			**IRQ2_EN**	**CNTTVAL2_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ2_STA	**Enables system timer 2 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ2_EN	**Enables system timer 2 interrupt** 0: Disable 1: Enable
0	CNTTVAL2_EN	**Enables system timer 2** 0: Disable 1: Enable

10017054 CNTTVAL2 System Counter Timer 2 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL2	**System timer 3 down counter** Write to set up timeout value; read as 32-bit down counter.

10017058 CNTTVAL3_CON System Counter Timer 3 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ3_STA**			**IRQ3_EN**	**CNTTVAL3_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ3_STA	**Enables system timer 3 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ3_EN	**Enables system timer 3 interrupt** 0: Disable 1: Enable
0	CNTTVAL3_EN	**Enables system timer 3** 0: Disable 1: Enable

1001705C CNTTVAL3 System Counter Timer 3 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL3	**System timer 3 down counter** Write to set up timeout value; read as 32-bit down counter.

10017060 CNTTVAL4_CON System Counter Timer 4 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ4_STA**			**IRQ4_EN**	**CNTTVAL4_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ4_STA	**Enables system timer 4 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ4_EN	**Enables system timer 4 interrupt** 0: Disable 1: Enable
0	CNTTVAL4_EN	**Enables system timer 4** 0: Disable 1: Enable

10017064 CNTTVAL4 System Counter Timer 4 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL4	**System timer 4 down counter** Write to set up timeout value; read as 32-bit down counter.

10017068 CNTTVAL5_CON System Counter Timer 5 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ5_STA**			**IRQ5_EN**	**CNTTVAL5_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ5_STA	**Enables system timer 5 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ5_EN	**Enables system timer 5 interrupt** 0: Disable 1: Enable
0	CNTTVAL5_EN	**Enables system timer 5** 0: Disable 1: Enable

1001706C CNTTVAL5 System Counter Timer 5 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL5	**System timer 5 down counter** Write to set up timeout value; read as 32-bit down counter.

10017070 CNTTVAL6_CON System Counter Timer 6 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ6_STA**			**IRQ6_EN**	**CNTTVAL6_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ6_STA	**Enables system timer 6 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ6_EN	**Enables system timer 6 interrupt** 0: Disable 1: Enable
0	CNTTVAL6_EN	**Enables system timer 6** 0: Disable 1: Enable

10017074 CNTTVAL6 System Counter Timer 6 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL6	**System timer 6 down counter** Write to set up timeout value; read as 32-bit down counter.

10017078 CNTTVAL7_CON System Counter Timer 7 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**IRQ7_STA**			**IRQ7_EN**	**CNTTVAL7_EN**
Type												RW			RW	RW
Reset												0			0	0

Bit(s)	Name	Description
4	IRQ7_STA	**Enables system timer 7 interrupt status** Write 0 to clear interrupt event. 0: Clear IRQ event 1: Assert IRQ
1	IRQ7_EN	**Enables system timer 7 interrupt** 0: Disable 1: Enable
0	CNTTVAL7_EN	**Enables system timer 7** 0: Disable 1: Enable

1001707C CNTTVAL7 System Counter Timer 7 Value Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CNTTVAL7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CNTTVAL7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CNTTVAL7	**System timer 8 down counter** Write to set up timeout value; read as 32-bit down counter.

10017080 DOMAIN_DIS Domain Disable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_DOMAIN_DIS								RD_DOMAIN_DIS							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	WR_DOMAIN_DIS	**Disable domain check for writing control registers of interrupts.** Bits 7 to 0 are for interrupts 7 to 0. 1: Disable domain check for write
7:0	RD_DOMAIN_DIS	**Disable domain check for reading control registers of interrupts.** Bits 7 to 0 are for interrupts 7 to 0. 1: Disable domain check for read

10017084 DOMAIN_VAL Domain Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DOMAIN_VAL_7				DOMAIN_VAL_6				DOMAIN_VAL_5				DOMAIN_VAL_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOMAIN_VAL_3				DOMAIN_VAL_2				DOMAIN_VAL_1				DOMAIN_VAL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	DOMAIN_VAL_7	**Domain value of interrupt 7**
27:24	DOMAIN_VAL_6	**Domain value of interrupt 6**
23:20	DOMAIN_VAL_5	**Domain value of interrupt 5**
19:16	DOMAIN_VAL_4	**Domain value of interrupt 4**
15:12	DOMAIN_VAL_3	**Domain value of interrupt 3**
11:8	DOMAIN_VAL_2	**Domain value of interrupt 2**
7:4	DOMAIN_VAL_1	**Domain value of interrupt 1**
3:0	DOMAIN_VAL_0	**Domain value of interrupt 0**

10017090 CNTRV_L_0 Low-32-bit Timer Value Set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_0	**Low-32 binary values of timer. 8 sets are created for multicores.**

10017094 CNTRV_H_0 High-32-bit Timer Value Set 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_0	**High-32 binary values of timer**

10017098 CNTRV_L_1 Low-32-bit Timer Value Set 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_1	**Low-32 binary values of timer. 8 sets are created for multicores.**

1001709C CNTRV_H_1 High-32-bit Timer Value Set 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_1	**High-32 binary values of timer**

100170A0 CNTRV_L_2 Low-32-bit Timer Value Set 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_2	**Low-32 binary values of timer. 8 sets are created for multicores.**

100170A4 CNTRV_H_2 High-32-bit Timer Value Set 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_2	**High-32 binary values of timer**

100170A8 CNTRV_L_3 Low-32-bit Timer Value Set 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_3	**Low-32 binary values of timer. 8 sets are created for multicores.**

100170AC CNTRV_H_3 High-32-bit Timer Value Set 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_3	**High-32 binary values of timer**

100170B0 CNTRV_L_4 Low-32-bit Timer Value Set 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_4	**Low-32 binary values of timer. 8 sets are created for multicores.**

100170B4 CNTRV_H_4 High-32-bit Timer Value Set 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_4	**High-32 binary values of timer**

100170B8 CNTRV_L_5 Low-32-bit Timer Value Set 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_5	**Low-32 binary values of timer. 8 sets are created for multicores.**

100170BC CNTRV_H_5 High-32-bit Timer Value Set 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_5	**High-32 binary values of timer**

100170C0 CNTRV_L_6 Low-32-bit Timer Value Set 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_6	**Low-32 binary values of timer. 8 sets are created for multicores.**

100170C4 CNTRV_H_6 High-32-bit Timer Value Set 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_6	**High-32 binary values of timer**

100170C8 CNTRV_L_7 Low-32-bit Timer Value Set 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_low_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_low_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_low_7	**Low-32 binary values of timer. 8 sets are created for multicores.**

100170CC **CNTRV_H_7** **High-32-bit Timer Value Set 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ST_CTR_BIN_high_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CTR_BIN_high_7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ST_CTR_BIN_high_7	**High-32 binary values of timer**

3.2 Audio

3.2.1 Register Definition

Module name: AFE Base address: (+0x1121_0000)

Address	Name	Width	Register Function
11210000	AUDIO_TOP_CON0	32	Audio Top Control Register 0
11210008	AUDIO_TOP_CON2	32	Audio Top Control Register 2
11210010	AUDIO_TOP_CON4	32	Audio Top Control Register 4
11210014	AUDIO_ENGEN_CON0	32	Audio engen Control Register 0
11210020	AFE_SINEGEN_CON0	32	AFE Sine-wave Gen Config 0
11210024	AFE_SINEGEN_CON1	32	AFE Sine-wave Gen Config 1
11210028	AFE_SINEGEN_CON2	32	AFE Sine-wave Gen Config 2
1121002C	AFE_SINEGEN_CON3	32	AFE Sine-wave Gen Config 2
11210038	AFE_APLL2_TUNER_CFG	32	AFE TUNER2 Control Register
1121003C	AFE_APLL2_TUNER_MON0	32	AFE TUNER2 Monitor Register
1121006C	AUDIO_TOP_IP_VERSION	32	Audio Top IP version
11210100	AFE_IRQ_MCU_EN	32	AFE IRQ MCU Enable0 Register
11210120	AFE_IRQ_MCU_STATUS	32	AFE IRQ MCU Status Register
11210124	AFE_CUSTOM_IRQ_MCU_STATUS	32	AFE CUSTOM IRQ MCU Status Register
11210128	AFE_IRQ_MCU_CLR	32	AFE IRQ Clear Register
1121012C	AFE_IRQ_MCU_MISS_CLR	32	AFE IRQ Miss Flag Clear Register
11210130	AFE_CUSTOM_IRQ_MCU_CLR	32	AFE CUSTOM IRQ Clear Register
11210134	AFE_CUSTOM_IRQ_MCU_MISS_CLR	32	AFE CUSTOM IRQ Miss Flag Clear Register
11210140	AFE_IRQ0_MCU_CFG0	32	AFE IRQ0 MCU Control Register 0
11210144	AFE_IRQ0_MCU_CFG1	32	AFE IRQ0 MCU Control Register 1
11210148	AFE_IRQ1_MCU_CFG0	32	AFE IRQ1 MCU Control Register 0
1121014C	AFE_IRQ1_MCU_CFG1	32	AFE IRQ1 MCU Control Register 1
11210150	AFE_IRQ2_MCU_CFG0	32	AFE IRQ2 MCU Control Register 0
11210154	AFE_IRQ2_MCU_CFG1	32	AFE IRQ2 MCU Control Register 1
11210308	AFE_IRQ_MCU_MON2	32	AFE IRQ MCU Monitor Register 2
11210310	AFE_IRQ0_CNT_MON	32	AFE IRQ0 Count Monitor Register
11210314	AFE_IRQ1_CNT_MON	32	AFE IRQ1 Count Monitor Register
11210318	AFE_IRQ2_CNT_MON	32	AFE IRQ2 Count Monitor Register
112113F0	ETDM_IN5_CON0	32	ETDM_IN5 Control Register 0
112113F4	ETDM_IN5_CON1	32	ETDM_IN5 Control Register 1
112113F8	ETDM_IN5_CON2	32	ETDM_IN5 Control Register 2
112113FC	ETDM_IN5_CON3	32	ETDM_IN5 Control Register3
11211400	ETDM_IN5_CON4	32	ETDM_IN5 Control Register4
11211404	ETDM_IN5_CON5	32	ETDM_IN5 Control Register5
11211410	ETDM_IN5_CON8	32	ETDM_IN5 Control Register8
11211418	ETDM_IN5_MON	32	ETDM IN5 Monitor
11211464	ETDM_OUT5_MON	32	ETDM OUT5 Monitor
11211570	ETDM_OUT5_CON0	32	ETDM_OUT5 Control Register 0
11211574	ETDM_OUT5_CON1	32	ETDM_OUT5 Control Register 1
11211578	ETDM_OUT5_CON2	32	ETDM_OUT5 Control Register 2
1121157C	ETDM_OUT5_CON3	32	ETDM_OUT5 Control Register 3
11211580	ETDM_OUT5_CON4	32	ETDM_OUT5 Control Register 4
11211584	ETDM_OUT5_CON5	32	ETDM_OUT5 Control Register 5
11211590	ETDM_OUT5_CON8	32	ETDM_OUT5 Control Register 8
112115E0	ETDM_4_7_COWORK_CON0	32	ETDM_4_7 Co-work Control Register 0
112115E4	ETDM_4_7_COWORK_CON1	32	ETDM_4_7 Co-work Control Register 1
11213900	AFE_CONN_MON_CFG	32	AFE CONNECTION MONITOR CONTROL REGISTER
11213904	AFE_CONN_MON0	32	AFE CONNECTION MONITOR0
11213908	AFE_CONN_MON1	32	AFE CONNECTION MONITOR1

Address	Name	Width	Register Function
1121390C	AFE_CONN_MON2	32	AFE CONNECTION MONITOR2
11213910	AFE_CONN_MON3	32	AFE CONNECTION MONITOR3
11213914	AFE_CONN_MON4	32	AFE CONNECTION MONITOR4
11213918	AFE_CONN_MON5	32	AFE CONNECTION MONITOR5
11213920	AFE_CONN_RS_0	32	AFE CONNECTION RIGHT SHIFT REGISTER
1121392C	AFE_CONN_RS_3	32	AFE CONNECTION RIGHT SHIFT REGISTER
11213960	AFE_CONN_16BIT_0	32	AFE CONNECTION 16BIT REGISTER
1121396C	AFE_CONN_16BIT_3	32	AFE CONNECTION 16BIT REGISTER
11213980	AFE_CONN_24BIT_0	32	AFE CONNECTION 24BIT REGISTER
1121398C	AFE_CONN_24BIT_3	32	AFE CONNECTION 24BIT REGISTER
11213D98	AFE_MEMIF_CON0	32	MEMIF related configuration
11213D9C	AFE_MEMIF_RW_MON_CFG	32	MEMIF RW Monitor
11213DA0	AFE_MEMIF_RD_MON	32	MEMIF RD Data
11213DA4	AFE_MEMIF_WR_MON	32	MEMIF WR Data
11213DA8	AFE_BUS_MON1	32	BUS Monitor1
11213DAC	AFE_BUS_MON2	32	Bus Monitor2
11213DB0	AFE_BUS_CFG0	32	BUS Debug Config
11211B44	AFE_CONN018_1	32	AFE Connection Register 018_1
11211B50	AFE_CONN018_4	32	AFE Connection Register 018_4
11211B64	AFE_CONN019_1	32	AFE Connection Register 019_1
11211B70	AFE_CONN019_4	32	AFE Connection Register 019_4
11212884	AFE_CONN124_1	32	AFE Connection Register 124_1
11212890	AFE_CONN124_4	32	AFE Connection Register 124_4
112128A4	AFE_CONN125_1	32	AFE Connection Register 125_1
112128B0	AFE_CONN125_4	32	AFE Connection Register 125_4
11213E40	AFE_DL0_BASE_MSB	32	AFE DL0 Base Address Register MSB
11213E44	AFE_DL0_BASE	32	AFE DL0 Base Address Register
11213E48	AFE_DL0_CUR_MSB	32	AFE DL0 Cursor Register MSB
11213E4C	AFE_DL0_CUR	32	AFE DL0 Cursor Register
11213E50	AFE_DL0_END_MSB	32	AFE DL0 End Address Register MSB
11213E54	AFE_DL0_END	32	AFE DL0 End Address Register
11213E58	AFE_DL0_RCH_MON	32	AFE Memory Interface Monitor Register RCH
11213E5C	AFE_DL0_LCH_MON	32	AFE Memory Interface Monitor Register LCH
11213E60	AFE_DL0_CON0	32	AFE DL0 Agent Control Register
11214220	AFE_VUL0_BASE_MSB	32	AFE VUL0 Base Address Register MSB
11214224	AFE_VUL0_BASE	32	AFE VUL0 Base Address Register
11214228	AFE_VUL0_CUR_MSB	32	AFE VUL0 Cursor Register MSB
1121422C	AFE_VUL0_CUR	32	AFE VUL0 Cursor Register
11214230	AFE_VUL0_END_MSB	32	AFE VUL0 End Address Register MSB
11214234	AFE_VUL0_END	32	AFE VUL0 End Address Register
11214238	AFE_VUL0_CON0	32	AFE VUL0 Agent Control Register

11210000 AUDIO_TOP_CON0 Audio Top Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															pdn_memif_hop_clk	pdn_memif_intbus_clk
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	pdn_memif_hop_clk	**Powers down memif hopping clock** 0: Does not power down memif hopping clk 1: Power down memif hopping clk
0	pdn_memif_intbus_clk	**Powers down memif intbus clock** 0: Does not power down memif intbus clk 1: Power down memif intbus clk

11210008 AUDIO_TOP_CON2 Audio Top Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		pdn_etdm_out5							pdn_etdm_in5							
Type		RW							RW							
Reset		0							0							

Bit(s)	Name	Description
14	pdn_etdm_out5	**Sets to 1 to gate eTDM OUT5 engine clock** 0: Not clock-gated 1: Clock-gated
7	pdn_etdm_in5	**Sets to 1 to gate eTDM IN5 engine clock** 0: Not clock-gated 1: Clock-gated

11210010 AUDIO_TOP_CON4 Audio Top Control Register 4 00003FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**PDN_APLL_TUNER2**									**CG_APLL2_CK**		**CG_AUDIO_F26M_CK**	**CG_AUDIO_HOPPING_CK**
Type				RW									RW		RW	RW
Reset				1									1		1	1

Bit(s)	Name	Description
12	PDN_APLL_TUNER2	**PDN control for apll2 tuner.** 0: Power on apll_tuner clock. 1: Power down apll_tuner clock.
3	CG_APLL2_CK	**PDN control for 49M.** 0: Power on apll2 49M clock. 1: Power down apll2 49M clock.
1	CG_AUDIO_F26M_CK	**PDN control for F26M CLK.** 0: Power on fix 26M clock. 1: Power down fix 26M clock.
0	CG_AUDIO_HOPPING_CK	**PDN control for HOPPING CLK.** 0: Power on hopping clock. 1: Power down hopping clock.

11210014 AUDIO_ENGEN_CON0 Audio engen Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AUDIO_F26M_EN_RST					AUDIO_APLL2_EN_ON			AUDIO_26M_EN_ON
Type								RW					RW			RW
Reset								0					0			0

Bit(s)	Name	Description
8	AUDIO_F26M_EN_RST	**SW reset the enabling of the f26m en** 0: Off 1: On
3	AUDIO_APLL2_EN_ON	**Controls the enabling of the apll2 en** 0: Off 1: On
0	AUDIO_26M_EN_ON	**Controls the enabling of the 26m en** 0: Off 1: On

11210020 AFE_SINEGEN_CON0 AFE Sine-wave Gen Config 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						dac_en	tie_sw_ch2	tie_sw_ch1		amp_div_ch2						freq_div_ch2
Type						RW	RW	RW		RW						RW
Reset						0	0	0		0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	freq_div_ch2					amp_div_ch1						freq_div_ch1				
Type	RW					RW						RW				
Reset	0	0	0	0		0	0	0				0	0	0	0	0

Bit(s)	Name	Description
26	dac_en	**Enables sinewave generator** 0: Untie sigen 1: tie sigen
25	tie_sw_ch2	**Sinewave generator tie constent for ch2** 0: Untie sigen 1: tie sigen
24	tie_sw_ch1	**Sinewave generator tie constent for ch1** 0: Unmute sigen 1: Mute sigen
22:20	amp_div_ch2	**Selects sinewave generator amplitude for ch2** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
16:12	freq_div_ch2	**Sinewave generator frequency selection for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch2** 0: DC output 1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period
10:8	amp_div_ch1	**Selects sinewave generator amplitude for ch1** 0: sinewave_out/128 1: sinewave_out/64 2: sinewave_out/32 3: sinewave_out/16 4: sinewave_out/8 5: sinewave_out/4 6: sinewave_out/2 7: sinewave_out/1
4:0	freq_div_ch1	**Sinewave generator frequency selection for ch2 sampled by signal timing generator selection bit[23:20] (or bit[31:28]) for ch1** 0: DC output

Bit(s)	Name	Description
		1: 64/1 samples/period 2: 64/2 samples/period 3: 64/3 samples/period 4: 64/4 samples/period 5: 64/5 samples/period 6: 64/6 samples/period x: 64/x samples/period 31: 64/31 samples/period

11210024 AFE_SINEGEN_CON1 AFE Sine-wave Gen Config 1 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										sine_domain						sine_mode
Type										RW						RW
Reset										0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sine_mode							INNER_LOOP_BACKI_SEL	INNER_LOOP_BACK_MODE							
Type	RW							RW	RW							
Reset	0	0	0	0				0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
22:20	sine_domain	**Enables sinewave generator domain selection** 0: Fix 26m domain 1: APLL domain 2: SPDIF domain 3: HDMI domain 4: eARC domain 5: Linein domain 6: Slave domain
16:12	sine_mode	**Enables sinewave generator timing selection** 0: 8k 1: 11.025k 2: 12k 4: 16k 5: 22.05k 6: 24k 8: 32k 9: 44.1k 10: 48k 13: 88.2k 14: 96k 17: 176.4k 18: 192k 21: 352.8k 22: 384k
8	INNER_LOOP_BACKI_SEL	0: Force interconn input port 1: Force interconn output port
7:0	INNER_LOOP_BACK_MODE	**Loopback mode testing for audio_conn.** 0: Sine generator ch1/ch2 force at interconn port 0/1 1: Sine generator ch1/ch2 force at interconn port 2/3 2: Sine generator ch1/ch2 force at interconn port 4/5 3: Sine generator ch1/ch2 force at interconn port 6/7 4: Sine generator ch1/ch2 force at interconn port 8/9 x: Sine generator ch1/ch2 force at interconn port 2x/2x-1

11210028 AFE_SINEGEN_CON2 AFE Sine-wave Gen Config 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tie_ch1_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tie_ch1_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tie_ch1_constent	**constent value for tie ch1**

1121002C AFE_SINEGEN_CON3 AFE Sine-wave Gen Config 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tie_ch2_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tie_ch2_constent															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tie_ch2_constent	**constent value for tie ch2**

11210038 AFE_APLL2_TUNER_CFG AFE TUNER2 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	upper_bound								apll_div					xtal_en_128fs_sel		freq_tuner_en
Type	RW								RW					RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
15:8	upper_bound	**Upper bound setting for changing PCW**
7:4	apll_div	**Divider setting of APLL 128fs**
2:1	xtal_en_128fs_sel	2'b00: 32 kHz*128 2'b01: 44.1 kHz*128 2'b10: 48 kHz*128 2'b11: 0
0	freq_tuner_en	1: Enable APLL tuner

1121003C **AFE_APLL2_TUNER_MON0** AFE TUNER2 Monitor Register **00100000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	tuner_mon															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	tuner_mon															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	tuner_mon	**Frequency difference count value** [9:0]: freq_diff [16]: lower_freq_sel [20]: trig_pcw_chg

1121006C AUDIO_TOP_IP_VERSION Audio Top IP version 10000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	audio_top_ip_version															
Type	RO															
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	audio_top_ip_version															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	audio_top_ip_version	**IP version**

11210100 AFE_IRQ_MCU_EN AFE IRQ MCU Enable0 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_IRQ_MCU_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ_MCU_EN															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	AFE_IRQ_MCU_EN	**IRQ to MCU enable control** 0: Disable IRQ 1: Enable IRQ

11210120 AFE_IRQ_MCU_STATUS AFE IRQ MCU Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IRQ26_MCU	IRQ25_MCU	IRQ24_MCU	IRQ23_MCU	IRQ22_MCU	IRQ21_MCU	IRQ20_MCU	IRQ19_MCU	IRQ18_MCU	IRQ17_MCU	IRQ16_MCU
Type						RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ15_MCU	IRQ14_MCU	IRQ13_MCU	IRQ12_MCU	IRQ11_MCU	IRQ10_MCU	IRQ9_MCU	IRQ8_MCU	IRQ7_MCU	IRQ6_MCU	IRQ5_MCU	IRQ4_MCU	IRQ3_MCU	IRQ2_MCU	IRQ1_MCU	IRQ0_MCU
Type	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	IRQ26_MCU	**This bit reads the status for IRQ26_MCU** 0: No interrupt 1: IRQ26 interrupt
25	IRQ25_MCU	**This bit reads the status for IRQ25_MCU** 0: No interrupt 1: IRQ25 interrupt
24	IRQ24_MCU	**This bit reads the status for IRQ24_MCU** 0: No interrupt 1: IRQ24 interrupt
23	IRQ23_MCU	**This bit reads the status for IRQ23_MCU** 0: No interrupt 1: IRQ23 interrupt
22	IRQ22_MCU	**This bit reads the status for IRQ22_MCU** 0: No interrupt 1: IRQ22 interrupt
21	IRQ21_MCU	**This bit reads the status for IRQ21_MCU** 0: No interrupt 1: IRQ21 interrupt
20	IRQ20_MCU	**This bit reads the status for IRQ20_MCU** 0: No interrupt 1: IRQ20 interrupt
19	IRQ19_MCU	**This bit reads the status for IRQ19_MCU** 0: No interrupt 1: IRQ19 interrupt
18	IRQ18_MCU	**This bit reads the status for IRQ18_MCU** 0: No interrupt 1: IRQ18 interrupt
17	IRQ17_MCU	**This bit reads the status for IRQ17_MCU** 0: No interrupt 1: IRQ17 interrupt
16	IRQ16_MCU	**This bit reads the status for IRQ16_MCU** 0: No interrupt 1: IRQ16 interrupt
15	IRQ15_MCU	**This bit reads the status for IRQ15_MCU** 0: No interrupt 1: IRQ15 interrupt
14	IRQ14_MCU	**This bit reads the status for IRQ14_MCU** 0: No interrupt 1: IRQ14 interrupt
13	IRQ13_MCU	**This bit reads the status for IRQ13_MCU** 0: No interrupt

Bit(s)	Name	Description
		1: IRQ13 interrupt
12	IRQ12_MCU	**This bit reads the status for IRQ12_MCU** 0: No interrupt 1: IRQ12 interrupt
11	IRQ11_MCU	**This bit reads the status for IRQ11_MCU** 0: No interrupt 1: IRQ11 interrupt
10	IRQ10_MCU	**This bit reads the status for IRQ10_MCU** 0: No interrupt 1: IRQ10 interrupt
9	IRQ9_MCU	**This bit reads the status for IRQ9_MCU** 0: No interrupt 1: IRQ9 interrupt
8	IRQ8_MCU	**This bit reads the status for IRQ8_MCU** 0: No interrupt 1: IRQ8 interrupt
7	IRQ7_MCU	**This bit reads the status for IRQ7_MCU** 0: No interrupt 1: IRQ7 interrupt
6	IRQ6_MCU	**This bit reads the status for IRQ6_MCU** 0: No interrupt 1: IRQ6 interrupt
5	IRQ5_MCU	**This bit reads the status for IRQ5_MCU** 0: No interrupt 1: IRQ5 interrupt
4	IRQ4_MCU	**This bit reads the status for IRQ4_MCU** 0: No interrupt 1: IRQ4 interrupt
3	IRQ3_MCU	**This bit reads the status for IRQ3_MCU** 0: No interrupt 1: IRQ3 interrupt
2	IRQ2_MCU	**This bit reads the status for IRQ2_MCU** 0: No interrupt 1: IRQ2 interrupt
1	IRQ1_MCU	**This bit reads the status for IRQ1_MCU** 0: No interrupt 1: IRQ1 interrupt
0	IRQ0_MCU	**This bit reads the status for IRQ0_MCU** 0: No interrupt 1: IRQ0 interrupt

11210124 AFE_CUSTOM_IRQ_MCU_STATUS AFE CUSTOM IRQ MCU Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CUSTOM_IRQ21_MCU	CUSTOM_IRQ20_MCU	CUSTOM_IRQ19_MCU	CUSTOM_IRQ18_MCU	CUSTOM_IRQ17_MCU	CUSTOM_IRQ16_MCU
Type											RU	RU	RU	RU	RU	RU
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CUSTOM_IRQ7_MCU	CUSTOM_IRQ6_MCU	CUSTOM_IRQ5_MCU	CUSTOM_IRQ4_MCU	CUSTOM_IRQ3_MCU	CUSTOM_IRQ2_MCU	CUSTOM_IRQ1_MCU	CUSTOM_IRQ0_MCU
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	CUSTOM_IRQ21_MCU	**This bit reads the status for CUSTOM_IRQ21_MCU** 0: No interrupt 1: CUSTOM_IRQ21 interrupt
20	CUSTOM_IRQ20_MCU	**This bit reads the status for CUSTOM_IRQ20_MCU** 0: No interrupt 1: CUSTOM_IRQ20 interrupt
19	CUSTOM_IRQ19_MCU	**This bit reads the status for CUSTOM_IRQ19_MCU** 0: No interrupt 1: CUSTOM_IRQ19 interrupt
18	CUSTOM_IRQ18_MCU	**This bit reads the status for CUSTOM_IRQ18_MCU** 0: No interrupt 1: CUSTOM_IRQ18 interrupt
17	CUSTOM_IRQ17_MCU	**This bit reads the status for CUSTOM_IRQ17_MCU** 0: No interrupt 1: CUSTOM_IRQ17 interrupt
16	CUSTOM_IRQ16_MCU	**This bit reads the status for CUSTOM_IRQ16_MCU** 0: No interrupt 1: CUSTOM_IRQ16 interrupt
7	CUSTOM_IRQ7_MCU	**This bit reads the status for CUSTOM_IRQ7_MCU** 0: No interrupt 1: CUSTOM_IRQ7 interrupt
6	CUSTOM_IRQ6_MCU	**This bit reads the status for CUSTOM_IRQ6_MCU** 0: No interrupt 1: CUSTOM_IRQ6 interrupt
5	CUSTOM_IRQ5_MCU	**This bit reads the status for CUSTOM_IRQ5_MCU** 0: No interrupt 1: CUSTOM_IRQ5 interrupt
4	CUSTOM_IRQ4_MCU	**This bit reads the status for CUSTOM_IRQ4_MCU** 0: No interrupt 1: CUSTOM_IRQ4 interrupt
3	CUSTOM_IRQ3_MCU	**This bit reads the status for CUSTOM_IRQ3_MCU** 0: No interrupt 1: CUSTOM_IRQ3 interrupt
2	CUSTOM_IRQ2_MCU	**This bit reads the status for CUSTOM_IRQ2_MCU** 0: No interrupt 1: CUSTOM_IRQ2 interrupt
1	CUSTOM_IRQ1_MCU	**This bit reads the status for CUSTOM_IRQ1_MCU**

Bit(s)	Name	Description
		0: No interrupt 1: CUSTOM_IRQ1 interrupt
0	CUSTOM_IRQ0_MCU	**This bit reads the status for CUSTOM_IRQ0_MCU** 0: No interrupt 1: CUSTOM_IRQ0 interrupt

11210128 AFE_IRQ_MCU_CLR AFE IRQ Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IRQ26_MCU_CLR	IRQ25_MCU_CLR	IRQ24_MCU_CLR	IRQ23_MCU_CLR	IRQ22_MCU_CLR	IRQ21_MCU_CLR	IRQ20_MCU_CLR	IRQ19_MCU_CLR	IRQ18_MCU_CLR	IRQ17_MCU_CLR	IRQ16_MCU_CLR
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ15_MCU_CLR	IRQ14_MCU_CLR	IRQ13_MCU_CLR	IRQ12_MCU_CLR	IRQ11_MCU_CLR	IRQ10_MCU_CLR	IRQ9_MCU_CLR	IRQ8_MCU_CLR	IRQ7_MCU_CLR	IRQ6_MCU_CLR	IRQ5_MCU_CLR	IRQ4_MCU_CLR	IRQ3_MCU_CLR	IRQ2_MCU_CLR	IRQ1_MCU_CLR	IRQ0_MCU_CLR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	IRQ26_MCU_CLR	**Clears the status for IRQ26_MCU; only works at write action.** 0: No operation 1: Clear IRQ26 Interrupt
25	IRQ25_MCU_CLR	**Clears the status for IRQ25_MCU; only works at write action.** 0: No operation 1: Clear IRQ25 Interrupt
24	IRQ24_MCU_CLR	**Clears the status for IRQ24_MCU; only works at write action.** 0: No operation 1: Clear IRQ24 Interrupt
23	IRQ23_MCU_CLR	**Clears the status for IRQ23_MCU; only works at write action.** 0: No operation 1: Clear IRQ23 Interrupt
22	IRQ22_MCU_CLR	**Clears the status for IRQ22_MCU; only works at write action.** 0: No operation 1: Clear IRQ22 Interrupt
21	IRQ21_MCU_CLR	**Clears the status for IRQ21_MCU; only works at write action.** 0: No operation 1: Clear IRQ21 Interrupt
20	IRQ20_MCU_CLR	**Clears the status for IRQ20_MCU; only works at write action.** 0: No operation 1: Clear IRQ20 Interrupt
19	IRQ19_MCU_CLR	**Clears the status for IRQ19_MCU; only works at write action.** 0: No operation 1: Clear IRQ19 Interrupt
18	IRQ18_MCU_CLR	**Clears the status for IRQ18_MCU; only works at write action.** 0: No operation 1: Clear IRQ18 Interrupt
17	IRQ17_MCU_CLR	**Clears the status for IRQ17_MCU; only works at write action.** 0: No operation 1: Clear IRQ17 Interrupt
16	IRQ16_MCU_CLR	**Clears the status for IRQ16_MCU; only works at write action.** 0: No operation 1: Clear IRQ16 Interrupt
15	IRQ15_MCU_CLR	**Clears the status for IRQ15_MCU; only works at write action.** 0: No operation 1: Clear IRQ15 Interrupt
14	IRQ14_MCU_CLR	**Clears the status for IRQ14_MCU; only works at write action.** 0: No operation 1: Clear IRQ14 Interrupt

Bit(s)	Name	Description
13	IRQ13_MCU_CLR	**Clears the status for IRQ13_MCU; only works at write action.** 0: No operation 1: Clear IRQ13 Interrupt
12	IRQ12_MCU_CLR	**Clears the status for IRQ12_MCU; only works at write action.** 0: No operation 1: Clear IRQ12 Interrupt
11	IRQ11_MCU_CLR	**Clears the status for IRQ11_MCU; only works at write action.** 0: No operation 1: Clear IRQ11 Interrupt
10	IRQ10_MCU_CLR	**Clears the status for IRQ10_MCU; only works at write action.** 0: No operation 1: Clear IRQ10 Interrupt
9	IRQ9_MCU_CLR	**Clears the status for IRQ9_MCU; only works at write action.** 0: No operation 1: Clear IRQ9 Interrupt
8	IRQ8_MCU_CLR	**Clears the status for IRQ8_MCU; only works at write action.** 0: No operation 1: Clear IRQ8 Interrupt
7	IRQ7_MCU_CLR	**Clears the status for IRQ7_MCU; only works at write action.** 0: No operation 1: Clear IRQ7 Interrupt
6	IRQ6_MCU_CLR	**Clears the status for IRQ6_MCU; only works at write action.** 0: No operation 1: Clear IRQ6 interrupt
5	IRQ5_MCU_CLR	**Clears the status for IRQ5_MCU; only works at write action.** 0: No operation 1: Clear IRQ5 interrupt
4	IRQ4_MCU_CLR	**Clears the status for IRQ4_MCU; only works at write action.** 0: No operation 1: Clear IRQ4 interrupt
3	IRQ3_MCU_CLR	**Clears the status for IRQ3_MCU; only works at write action.** 0: No operation 1: Clear IRQ3 interrupt
2	IRQ2_MCU_CLR	**Clears the status for IRQ2_MCU; only works at write action.** 0: No operation 1: Clear IRQ2 interrupt
1	IRQ1_MCU_CLR	**Clears the status for IRQ1_MCU; only works at write action.** 0: No operation 1: Clear IRQ1 interrupt
0	IRQ0_MCU_CLR	**Clears the status for IRQ0_MCU; only works at write action.** 0: No operation 1: Clear IRQ0 interrupt

1121012C AFE_IRQ_MCU_MISS_CLR AFE IRQ Miss Flag Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						IRQ26_MCU_MISS_CNT_CLR	IRQ25_MCU_MISS_CNT_CLR	IRQ24_MCU_MISS_CNT_CLR	IRQ23_MCU_MISS_CNT_CLR	IRQ22_MCU_MISS_CNT_CLR	IRQ21_MCU_MISS_CNT_CLR	IRQ20_MCU_MISS_CNT_CLR	IRQ19_MCU_MISS_CNT_CLR	IRQ18_MCU_MISS_CNT_CLR	IRQ17_MCU_MISS_CNT_CLR	IRQ16_MCU_MISS_CNT_CLR
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IRQ15_MCU_MISS_CNT_CLR	IRQ14_MCU_MISS_CNT_CLR	IRQ13_MCU_MISS_CNT_CLR	IRQ12_MCU_MISS_CNT_CLR	IRQ11_MCU_MISS_CNT_CLR	IRQ10_MCU_MISS_CNT_CLR	IRQ9_MCU_MISS_CNT_CLR	IRQ8_MCU_MISS_CNT_CLR	IRQ7_MCU_MISS_CNT_CLR	IRQ6_MCU_MISS_CNT_CLR	IRQ5_MCU_MISS_CNT_CLR	IRQ4_MCU_MISS_CNT_CLR	IRQ3_MCU_MISS_CNT_CLR	IRQ2_MCU_MISS_CNT_CLR	IRQ1_MCU_MISS_CNT_CLR	IRQ0_MCU_MISS_CNT_CLR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	IRQ26_MCU_MISS_CNT_CLR	**Clears the status of IRQ26 miss count flag, only works at write action.** 0: No operation 1: Clear IRQ26 miss cnt
25	IRQ25_MCU_MISS_CNT_CLR	**Clears the status of IRQ25 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ25 miss cnt
24	IRQ24_MCU_MISS_CNT_CLR	**Clears the status of IRQ24 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ24 miss cnt
23	IRQ23_MCU_MISS_CNT_CLR	**Clears the status of IRQ23 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ23 miss cnt
22	IRQ22_MCU_MISS_CNT_CLR	**Clears the status of IRQ22 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ22 miss cnt
21	IRQ21_MCU_MISS_CNT_CLR	**Clears the status of IRQ21 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ21 miss cnt
20	IRQ20_MCU_MISS_CNT_CLR	**Clears the status of IRQ20 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ20 miss cnt
19	IRQ19_MCU_MISS_CNT_CLR	**Clears the status of IRQ19 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ19 miss cnt
18	IRQ18_MCU_MISS_CNT_CLR	**Clears the status of IRQ18 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ18 miss cnt
17	IRQ17_MCU_MISS_CNT_CLR	**Clears the status of IRQ17 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ17 miss cnt
16	IRQ16_MCU_MISS_CNT_CLR	**Clears the status of IRQ16 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ16 miss cnt
15	IRQ15_MCU_MISS_CNT_CLR	**Clears the status of IRQ15 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ15 miss cnt

Bit(s)	Name	Description
14	IRQ14_MCU_MISS_CNT_CLR	**Clears the status of IRQ14 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ14 miss cnt
13	IRQ13_MCU_MISS_CNT_CLR	**Clears the status of IRQ13 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ13 miss cnt
12	IRQ12_MCU_MISS_CNT_CLR	**Clears the status of IRQ12 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ12 miss cnt
11	IRQ11_MCU_MISS_CNT_CLR	**Clears the status of IRQ11 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ11 miss cnt
10	IRQ10_MCU_MISS_CNT_CLR	**Clears the status of IRQ10 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ10 miss cnt
9	IRQ9_MCU_MISS_CNT_CLR	**Clears the status of IRQ9 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ9 miss cnt
8	IRQ8_MCU_MISS_CNT_CLR	**Clears the status of IRQ8 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ8 miss cnt
7	IRQ7_MCU_MISS_CNT_CLR	**Clears the status of IRQ7 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ7 miss cnt
6	IRQ6_MCU_MISS_CNT_CLR	**Clears the status of IRQ6 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ6 miss cnt
5	IRQ5_MCU_MISS_CNT_CLR	**Clears the status of IRQ5 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ5 miss cnt
4	IRQ4_MCU_MISS_CNT_CLR	**Clears the status of IRQ4 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ4 miss cnt
3	IRQ3_MCU_MISS_CNT_CLR	**Clears the status of IRQ3 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ3 miss cnt
2	IRQ2_MCU_MISS_CNT_CLR	**Clears the status of IRQ2 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ2 miss cnt
1	IRQ1_MCU_MISS_CNT_CLR	**Clears the status of IRQ1 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ1 miss cnt
0	IRQ0_MCU_MISS_CNT_CLR	**Clears the status of IRQ0 miss count flag; only works at write action.** 0: No operation 1: Clear IRQ0 miss cnt

11210130 AFE_CUSTOM_IRQ_MCU_CLR AFE CUSTOM IRQ Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CUSTOM_IRQ21_MCU_CLR	CUSTOM_IRQ20_MCU_CLR	CUSTOM_IRQ19_MCU_CLR	CUSTOM_IRQ18_MCU_CLR	CUSTOM_IRQ17_MCU_CLR	CUSTOM_IRQ16_MCU_CLR
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CUSTOM_IRQ7_MCU_CLR	CUSTOM_IRQ6_MCU_CLR	CUSTOM_IRQ5_MCU_CLR	CUSTOM_IRQ4_MCU_CLR	CUSTOM_IRQ3_MCU_CLR	CUSTOM_IRQ2_MCU_CLR	CUSTOM_IRQ1_MCU_CLR	CUSTOM_IRQ0_MCU_CLR
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	CUSTOM_IRQ21_MCU_CLR	**Clears the status for CUSTOM_IRQ21_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ21 Interrupt
20	CUSTOM_IRQ20_MCU_CLR	**Clears the status for CUSTOM_IRQ20_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ20 Interrupt
19	CUSTOM_IRQ19_MCU_CLR	**Clears the status for CUSTOM_IRQ19_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ19 Interrupt
18	CUSTOM_IRQ18_MCU_CLR	**Clears the status for CUSTOM_IRQ18_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ18 Interrupt
17	CUSTOM_IRQ17_MCU_CLR	**Clears the status for CUSTOM_IRQ17_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ17 Interrupt
16	CUSTOM_IRQ16_MCU_CLR	**Clears the status for CUSTOM_IRQ16_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ16 Interrupt
7	CUSTOM_IRQ7_MCU_CLR	**Clears the status for CUSTOM_IRQ7_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ7 Interrupt
6	CUSTOM_IRQ6_MCU_CLR	**Clears the status for CUSTOM_IRQ6_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ6 interrupt
5	CUSTOM_IRQ5_MCU_CLR	**Clears the status for CUSTOM_IRQ5_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ5 interrupt
4	CUSTOM_IRQ4_MCU_CLR	**Clears the status for CUSTOM_IRQ4_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ4 interrupt
3	CUSTOM_IRQ3_MCU_CLR	**Clears the status for CUSTOM_IRQ3_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ3 interrupt
2	CUSTOM_IRQ2_MCU_CLR	**Clears the status for CUSTOM_IRQ2_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ2 interrupt
1	CUSTOM_IRQ1_MCU_CLR	**Clears the status for CUSTOM_IRQ1_MCU; only works at write action.**

Bit(s)	Name	Description
0	CUSTOM_IRQ0_MCU_CLR	0: No operation 1: Clear CUSTOM_IRQ1 interrupt **Clears the status for CUSTOM_IRQ0_MCU; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ0 interrupt

11210134 AFE_CUSTOM_IRQ_MCU_MIS_CLR AFE CUSTOM IRQ Miss Flag Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											CUSTOM_IRQ21_MCU_MISS_CNT_CLR	CUSTOM_IRQ20_MCU_MISS_CNT_CLR	CUSTOM_IRQ19_MCU_MISS_CNT_CLR	CUSTOM_IRQ18_MCU_MISS_CNT_CLR	CUSTOM_IRQ17_MCU_MISS_CNT_CLR	CUSTOM_IRQ16_MCU_MISS_CNT_CLR
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CUSTOM_IRQ7_MCU_MISS_CNT_CLR	CUSTOM_IRQ6_MCU_MISS_CNT_CLR	CUSTOM_IRQ5_MCU_MISS_CNT_CLR	CUSTOM_IRQ4_MCU_MISS_CNT_CLR	CUSTOM_IRQ3_MCU_MISS_CNT_CLR	CUSTOM_IRQ2_MCU_MISS_CNT_CLR	CUSTOM_IRQ1_MCU_MISS_CNT_CLR	CUSTOM_IRQ0_MCU_MISS_CNT_CLR
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	CUSTOM_IRQ21_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ21 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ21 miss cnt
20	CUSTOM_IRQ20_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ20 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ20 miss cnt
19	CUSTOM_IRQ19_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ19 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ19 miss cnt
18	CUSTOM_IRQ18_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ18 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ18 miss cnt
17	CUSTOM_IRQ17_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ17 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ17 miss cnt
16	CUSTOM_IRQ16_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ16 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ16 miss cnt
7	CUSTOM_IRQ7_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ7 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ7 miss cnt
6	CUSTOM_IRQ6_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ6 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ6 miss cnt
5	CUSTOM_IRQ5_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ5 miss count flag; only works at write action.**

Bit(s)	Name	Description
		0: No operation 1: Clear CUSTOM_IRQ5 miss cnt
4	CUSTOM_IRQ4_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ4 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ4 miss cnt
3	CUSTOM_IRQ3_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ3 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ3 miss cnt
2	CUSTOM_IRQ2_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ2 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ2 miss cnt
1	CUSTOM_IRQ1_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ1 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ1 miss cnt
0	CUSTOM_IRQ0_MCU_MISS_CNT_CLR	**Clears the status of CUSTOM_IRQ0 miss count flag; only works at write action.** 0: No operation 1: Clear CUSTOM_IRQ0 miss cnt

11210140 AFE_IRQ0_MCU_CFG0 AFE IRQ0 MCU Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**AFE_IRQ0_MCU_DOMAIN**			**AFE_IRQ0_MCU_FS**								**AFE_IRQ0_MCU_ON**
Type					RW			RW								RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:9	AFE_IRQ0_MCU_DOMAIN	**Controls the IRQ0_MCU count domain** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
8:4	AFE_IRQ0_MCU_FS	**Controls the IRQ0_MCU count unit** 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k 5'h16: 384k
0	AFE_IRQ0_MCU_ON	**Controls the enabling of IRQ0_MCU** 0: Off 1: On

11210144 AFE_IRQ0_MCU_CFG1 AFE IRQ0 MCU Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ0_MCU_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ0_MCU_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ0_MCU_CNT	**Sets up the counter value for IRQ0 according to AFE_IRQ0_MCU_FS. The IRQ0 counter in AFE will count down from AFE_IRQ0_MCU_CNT0 and set up IRQ0 while IRQ0 counter reaches 1.**

11210148 AFE_IRQ1_MCU_CFG0 AFE IRQ1 MCU Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**AFE_IRQ1_MCU_DOMAIN**			**AFE_IRQ1_MCU_FS**								**AFE_IRQ1_MCU_ON**
Type					RW			RW								RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:9	AFE_IRQ1_MCU_DOMAIN	**Controls the IRQ1_MCU count domain** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h7: Slave clk domain
8:4	AFE_IRQ1_MCU_FS	**Controls the IRQ1_MCU count unit** 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k 5'h16: 384k
0	AFE_IRQ1_MCU_ON	**Controls the enabling of IRQ1_MCU** 0: Off 1: On

1121014C AFE_IRQ1_MCU_CFG1 AFE IRQ1 MCU Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ1_MCU_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_MCU_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ1_MCU_CNT	**Sets up the counter value for IRQ1 according to AFE_IRQ1_MCU_FS. The IRQ1 counter in AFE will count down from AFE_IRQ1_MCU_CNT0 and set up IRQ1 while IRQ1 counter reaches 1.**

11210150 AFE_IRQ2_MCU_CFG0 AFE IRQ2 MCU Control Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**AFE_IRQ2_MCU_DOMAIN**			**AFE_IRQ2_MCU_FS**								**AFE_IRQ2_MCU_ON**
Type					RW			RW								RW
Reset					0	0	0	0	0	0	0	0				0

Bit(s)	Name	Description
11:9	AFE_IRQ2_MCU_DOMAIN	**Controls the IRQ2_MCU count domain** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h8: Slave clk domain
8:4	AFE_IRQ2_MCU_FS	**Controls the IRQ2_MCU count unit** 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k 5'h16: 384k
0	AFE_IRQ2_MCU_ON	**Controls the enabling of IRQ2_MCU** 0: Off 2: On

11210154 AFE_IRQ2_MCU_CFG1 AFE IRQ2 MCU Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ2_MCU_CNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_MCU_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ2_MCU_CNT	**Sets up the counter value for IRQ2 according to AFE_IRQ2_MCU_FS. The IRQ2 counter in AFE will count down from AFE_IRQ2_MCU_CNT0 and set up IRQ2 while IRQ2 counter reaches 1.**

11210308 AFE_IRQ_MCU_MON2 AFE IRQ MCU Monitor Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AFE_CUSTOM_IRQ_MCU_MISS_FLAG_CLR_PHASE	AFE_CUSTOM_IRQ_MCU_CLR_PHASE	AFE_IRQ_MCU_MISS_FLAG_CLR_PHASE	AFE_IRQ_MCU_CLR_PHASE												
Type	RU	RU	RU	RU												
Reset	0	0	0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	AFE_CUSTOM_IRQ_MCU_MISS_FLAG_CLR_PHASE	**Read only register to monitor if custom miss_flag_clr trigger**
30	AFE_CUSTOM_IRQ_MCU_CLR_PHASE	**Read only register to monitor if custom irq_clr trigger**
29	AFE_IRQ_MCU_MISS_FLAG_CLR_PHASE	**Read only register to monitor if miss_flag_clr trigger**
28	AFE_IRQ_MCU_CLR_PHASE	**Read only register to monitor if irq_clr trigger**

11210310 AFE_IRQ0_CNT_MON AFE IRQ0 Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ0_CNT_MON							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ0_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ0_CNT_MON	**Monitors the counter value for IRQ0 according to AFE_IRQ0_MODE. The IRQ0 counter in AFE will count down from AFE_IRQ0_CNT.**

11210314 AFE_IRQ1_CNT_MON AFE IRQ1 Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ1_CNT_MON							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ1_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ1_CNT_MON	**Monitors the counter value for IRQ1 according to AFE_IRQ1_MODE. The IRQ1 counter in AFE will count down from AFE_IRQ1_CNT.**

11210318 AFE_IRQ2_CNT_MON AFE IRQ2 Count Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									AFE_IRQ2_CNT_MON							
Type									RU							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AFE_IRQ2_CNT_MON															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	AFE_IRQ2_CNT_MON	**Monitors the counter value for IRQ2 according to AFE_IRQ2_MODE. The IRQ2 counter in AFE will count down from AFE_IRQ2_CNT.**

112113F0 ETDM_IN5_CON0 ETDM_IN5 Control Register 0 009FF800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_valid_together	reg_relatch_1x_en_domain_sel			reg_ch_num							reg_word_length				
Type	RW	RW			RW							RW				
Reset	0	0	0	0	0	0	0	0	1			1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_bit_length							reg_fmt			reg_slave_mode	reg_soft_rst	reg_lsb_first		reg_sync_mode	reg_etdm_in_en
Type	RW							RW			RW	RW	RW		RW	RW
Reset	1	1	1	1	1			0	0	0	0	0	0		0	0

Bit(s)	Name	Description
31	reg_valid_together	**When reg_bit_length < reg_word_length, the valid data are arranged together or not (not: fill 0)** 0: Not together 1: Together
30:28	reg_relatch_1x_en_domain_sel	**Selects clock domain of re-latch 1x_en.** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
27:23	reg_ch_num	**The channel number of ETDM in. If ETDM in is multi-IP mode, the channel number should be set as 2ch.** 0: 1 1: 2 n: n+1
20:16	reg_word_length	**The BCK number in each channel. Reg_word_length should be larger than reg_bit_length.** 31: 32 bits 30: 31 bits N: N+1 bits 6: 7 bits Others: Not allowed.
15:11	reg_bit_length	**The valid bit number in each channel.** 31: 32 bits 30: 31 bits N: N+1 bits 6: 7 bits Others: Not allowed.
8:6	reg_fmt	**Sets the interface protocol of ETDM in.** 0: I2S 1: LJ 2: RJ 3: EIAJ 4: DSPA/TDM_delay/PCMA(2CH) 5: DSPB/TDM/PCMB(2CH) 6: DSD Others: Not allowed.

Bit(s)	Name	Description
5	reg_slave_mode	**ETDM in is master mode or slave mode.** 0: Master mode 1: Slave mode
4	reg_soft_rst	**Reset ETDM in hardware when this bit is high.** 0: Normal work 1: Reset valid
3	reg_lsb_first	**The first serial data is LSB or MSB.** 0: MSB first 1: LSB first
1	reg_sync_mode	**Disable/Enable sync mode of ETDM in.** 0: Disable 1: Enable
0	reg_etdm_in_en	**Disable/Enable ETDM in.** 0: Disable 1: Enable

112113F4 **ETDM_IN5_CON1** **ETDM_IN5 Control Register 1** **800985CE**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_direct_input_master_bck														
Type		RW														
Reset		0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		reg_no_align_1x_en														
Type		RW														
Reset		0														

Bit(s)	Name	Description
30	reg_direct_input_master_bck	**Master BCK generated mode.** 0: Master BCK generated by 1x_en 1: Master BCK generated by divider
14	reg_no_align_1x_en	**ETDM start time will align with 1x_en timing or not.** 0: Align with 1x_en 1: Not align with 1x_en

112113F8 ETDM_IN5_CON2 ETDM_IN5 Control Register 2 0410C062

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_multi_ip_mode	reg_lrck_delay_bck_inv	reg_lrck_delay_0p5t_en	reg_sdata_delay_bck_inv	reg_sdata_delay_0p5t_en	reg_update_point_auto							reg_multi_ip_total_chnum			
Type	RW	RW	RW	RW	RW	RW							RW			
Reset	0	0	0	0	0	1							0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_multi_ip_total_chnum	reg_ck_en_sel_auto		reg_clock_source_sel								reg_update_point				
Type	RW	RW		RW								RW				
Reset	1	1		0	0	0						0	0	0	1	0

Bit(s)	Name	Description
31	reg_multi_ip_mode	**ETDM in use multi-IP mode or multi-ch mode.** 0: One IP multi-ch mode (one sdata transfer 2ch or multi-ch) 1: Multi-IP 2ch mode (more than one sdata and every sdata transfer 2 channels)
30	reg_lrck_delay_bck_inv	**Invert LRCK delay BCK or not. If invert, the LRCK will delay 0.5T BCK, else the LRCK will delay 1T BCK.** 0: No invert BCK 1: Invert BCK
29	reg_lrck_delay_0p5t_en	**Whether to add 0.5T BCK delay for input LRCK.** 0: Disable 1: Enable
28	reg_sdata_delay_bck_inv	**Invert sdata delay BCK or not. If invert, the sdata will delay 0.5T BCK, else the sdata will delay 1T BCK.** 0: No invert BCK 1: Invert BCK
27	reg_sdata_delay_0p5t_en	**Whether to add 0.5T BCK delay for input sdata.** 0: Disable 1: Enable
26	reg_update_point_auto	**Auto select update point according to reg_fmt and reg_ch_num.** 0: Disable 1: Enable
19:15	reg_multi_ip_total_chnum	**The total channel number for multi-IP mode.** 0: 1 1: 2 n: n+1
14	reg_ck_en_sel_auto	**Auto select timing or not, only valid in engen timing mode.** 0: Use manual mode to select timing (ETDM_IN_CON8[25:16]) 1: Auto select timing according to other settings
12:10	reg_clock_source_sel	**Select MCLK source for ETDM.** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
4:0	reg_update_point	**When latch the data transfer to next stage. Only valid when reg_update_point_auto is 0**

Bit(s)	Name	Description
		0: 0
		1: 1
		n: n

112113FC **ETDM_IN5_CON3** **ETDM_IN5 Control Register3** **01F80000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_fs_timing_sel														
Type		RW														
Reset		0	0	0	0	0										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_disable_out															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:26	reg_fs_timing_sel	**Select sample rate.** 0: 8 kHz 1: 12 kHz 2: 16 kHz 3: 24 kHz 4: 32 kHz 5: 48 kHz 7: 96 kHz 9: 192 kHz 11: 384 kHz 16: 11.025 kHz 17: 22.05 kHz 18: 44.1 kHz 19: 88.2 kHz 20: 176.4 kHz 21: 352.8 kHz else: 0
15:0	reg_disable_out	**Only valid when the ETDM direct connect to memif agent.** Bit 0: Disable out setting for channel 0/1 Bit 1: Disable out setting for channel 2/3 Bit n: Disable out setting for channel 2n/2n+1

11211400 ETDM_IN5_CON4 ETDM_IN5 Control Register4 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_wait_last_sample						reg_relatch_1x_en_sel					reg_master_ws_inv	reg_master_bck_inv	reg_slave_lrck_inv	reg_slave_bck_inv
Type		RW						RW					RW	RW	RW	RW
Reset		0						0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					reg_async_reset	reg_repack_word_length		reg_repack_auto_mode								
Type					RW	RW		RW								
Reset					0	0	0	1								

Bit(s)	Name	Description
30	reg_wait_last_sample	**Will wait for the last sample transfer done or not when ETDM off.** 0: Not wait for the last sample 1: Wait for the last sample
24:20	reg_relatch_1x_en_sel	**Re-latch stage sample rate select.** 0: 8 kHz 1: 11.025 kHz 2: 12 kHz 4: 16 kHz 5: 22.05 kHz 6: 24 kHz 8: 32 kHz 9: 44 kHz 10: 48 kHz 13: 88.2 kHz 14: 96 kHz 17: 176.4 kHz 18: 192 kHz 21: 352.8 kHz 22: 384 kHz Else: 0
19	reg_master_ws_inv	**This bit is only valid for output LRCK in master mode.** 0: Not inverse 1: Inverse
18	reg_master_bck_inv	**This bit is only valid for output BCK in master mode.** 0: Not inverse 1: Inverse
17	reg_slave_lrck_inv	**ETDM slave LRCK inverse or not.** 0: Not inverse 1: Inverse
16	reg_slave_bck_inv	**ETDM slave BCK inverse or not.** 0: Not inverse 1: Inverse
11	reg_async_reset	**Software asynchronous reset.** 0: Normal work 1: Asynchronous reset valid
10:9	reg_repack_word_length	**The valid bit length for data repacking.** 0: 32 bits 1: 24 bits

Bit(s)	Name	Description
		2: 16 bits
		3: 8 bits
8	reg_repack_auto_mode	**Auto select repack mode according to others setting or not.** 0: Manual mode 1: Auto mode

11211404 ETDM_IN5_CON5 ETDM_IN5 Control Register5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_lr_swap															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_odd_flag_en															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	reg_lr_swap	**Swap right channel and left channel or not.** Bit 0: For channel 0/1 Bit 1: For channel 2/3 Bit n: For channel 2n/2n+1
15:0	reg_odd_flag_en	**Only supports multi-ch mode in the case of ETDM direct connects to memif agent.** Bit 0: For channel 0/1 Bit 1: For channel 2/3 Bit n: For channel 2n/2n+1

11211410 ETDM_IN5_CON8 ETDM_IN5 Control Register8 40004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_afifo_threshold					reg_ck_en_sel_manual									
Type		RW					RW									
Reset		1	0				0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_afifo_sw_reset	reg_afifo_reset_sel					reg_afifo_auto_reset_dis	reg_etdm_use_afifo	reg_afifo_clock_domain_sel			reg_afifo_mode				
Type	RW	RW					RW	RW	RW			RW				
Reset	0	1					0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:29	reg_afifo_threshold	**INTERCONN can read data from AFIFO when AFIFO data number larger than this setting, 1 and 2 are recommended value for this setting.** 0: 0 1: 1 2: 2 3: 3
25:16	reg_ck_en_sel_manual	**When reg_ck_en_sel_auto is 0, this setting will replace the value of {reg_ch_num, reg_word_length}.**
15	reg_afifo_sw_reset	**Software reset for AFIFO.** 0: Normal 1: Software reset
14	reg_afifo_reset_sel	**Will reset AFIFO when ETDM on/off.** 0: Reset when ETDM on 1: Both reset when ETDM on and ETDM off
9	reg_afifo_auto_reset_dis	**When ETDM in off, AFIFO will reset in auto reset mode. Otherwise, AFIFO can only reset by software reset and global hardware reset.** 0: Auto reset 1: Disable auto reset
8	reg_etdm_use_afifo	**ETDM use AFIFO or not.** 0: Disable AFIFO 1: Enable AFIFO
7:5	reg_afifo_clock_domain_sel	**Select the clock domain of AFIFO read 1x_en.** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
4:0	reg_afifo_mode	**Read sample rate of AFIFO.** 0: 8 kHz 1: 11.025 kHz 2: 12 kHz 4: 16 kHz 5: 22.05 kHz 6: 24 kHz 8: 32 kHz 9: 44 kHz 10: 48 kHz

Bit(s)	Name	Description
		13: 88.2 kHz 14: 96 kHz 17: 176.4 kHz 18: 192 kHz 21: 352.8 kHz 22: 384 kHz Else: 0

11211418 ETDM_IN5_MON ETDM IN5 Monitor 040500A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					wfull	rempty	etdm_2x_ck_en	etdm_1x_ck_en	sdata0	current_status		bit_point				
Type					RO	RO	RO	RO	RO	RO		RO				
Reset					0	1	0	0	0	0	0	0	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bit_ch_count						bit_count					ch_count				
Type	RO						RO					RO				
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
27	wfull	**Async FIFO write full**
26	rempty	**Async FIFO read empty**
25	etdm_2x_ck_en	**2X_CK_EN of ETDM in, ENGEN is enabled if this bit is variable.**
24	etdm_1x_ck_en	**1X_CK_EN of ETDM in, ENGEN is enabled if this bit is variable.**
23	sdata0	**Monitor ETDM input serial data**
22:21	current_status	**ETDM status.** 00: ETDM is off 01: ETDM is off to on 10: ETDM is on to off 11: ETDM is on
20:16	bit_point	**The bit point of ETDM.**
15:10	bit_ch_count	**The bit channel counter of ETDM.**
9:5	bit_count	**The bit counter of ETDM.**
4:0	ch_count	**The channel counter of ETDM.**

11211464 ETDM_OUT5_MON ETDM OUT5 Monitor 000600A0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							etdm_2x_ck_en	etdm_1x_ck_en	sdata0	current_status		bit_point				
Type							RO	RO	RO	RO		RO				
Reset							0	0	0	0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	bit_ch_count						bit_count					ch_count				
Type	RO						RO					RO				
Reset	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
25	etdm_2x_ck_en	**2X_CK_EN of ETDM in, ENGEN is enabled if this bit is variable.**
24	etdm_1x_ck_en	**1X_CK_EN of ETDM in, ENGEN is enabled if this bit is variable.**
23	sdata0	**Monitor ETDM input serial data**
22:21	current_status	**ETDM status.** 00: ETDM is off 01: ETDM is off to on 10: ETDM is on to off 11: ETDM is on
20:16	bit_point	**The bit point of ETDM.**
15:10	bit_ch_count	**The bit channel counter of ETDM.**
9:5	bit_count	**The bit counter of ETDM.**
4:0	ch_count	**The channel counter of ETDM.**

11211570 ETDM_OUT5_CON0 ETDM_OUT5 Control Register 0 009FF800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_valid_together	reg_relatch_domain_sel			reg_ch_num							reg_word_length				
Type	RW	RW			RW							RW				
Reset	0	0	0	0	0	0	0	0	1			1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_bit_length							reg_fmt				reg_soft_rst	reg_lsb_first		reg_sync_mode	reg_etdm_out_en
Type	RW							RW				RW	RW		RW	RW
Reset	1	1	1	1	1			0	0	0		0	0		0	0

Bit(s)	Name	Description
31	reg_valid_together	**When reg_bit_length < reg_word_length, the valid data are arranged together or not (not: fill 0)** 0: Not together 1: Together
30:28	reg_relatch_domain_sel	**Selects clock domain of re-latch 1x_en.** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
27:23	reg_ch_num	**The channel number of ETDM out. If ETDM out is multi-IP mode, the channel number should be set as 2ch.** 0: 1 1: 2 n: n+1
20:16	reg_word_length	**The BCK number in each channel. Reg_word_length should be larger than reg_bit_length.** 31: 32 bits 30: 31 bits N: N+1 bits 6: 7bits Others: Not allowed.
15:11	reg_bit_length	**The valid bit number in each channel.** 31: 32 bits 30: 31 bits N: N+1 bits 6: 7bits Others: Not allowed.
8:6	reg_fmt	**Sets the interface protocol of ETDM out.** 0: I2S 1: LJ 2: RJ 3: EIAJ 4: DSPA/TDM_delay/PCMA(2CH) 5: DSPB/TDM/PCMB(2CH) 6: DSD Others: Not allowed.

Bit(s)	Name	Description
4	reg_soft_rst	**Reset ETDM out hardware when this bit is high.** 0: Normal work 1: Reset valid
3	reg_lsb_first	**The first serial data is LSB or MSB.** 0: MSB first 1: LSB first
1	reg_sync_mode	**Disable/Enable sync mode of ETDM out.** 0: Disable 1: Enable
0	reg_etdm_out_en	**Disable/Enable ETDM out.** 0: Disable 1: Enable

11211574 ETDM_OUT5_CON1 ETDM_OUT5 Control Register 1 200185CE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_16b_compact_mode	reg_direct_input_master_bck	reg_lrck_auto_mode	reg_lrck_width										reg_output_cr_en		
Type	RW	RW	RW	RW										RW		
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_lrck_reset	reg_no_align_1x_en														
Type	RW	RW														
Reset	1	0														

Bit(s)	Name	Description
31	reg_16b_compact_mode	**One 32bit data contains LCH ([15:0]) and RCH ([31:16]) data, only valid when reg_bit_length is less than 16.** 0: Disable 1: Enable
30	reg_direct_input_master_bck	**Master BCK generated mode.** 0: Master BCK generated by 1x_en 1: Master BCK generated by divider
29	reg_lrck_auto_mode	**Auto set LRCK high level width according to others setting.** 0: Manual mode 1: Auto mode
28:19	reg_lrck_width	**Sets the high pulse width of LRCK in master mode. Only valid when reg_lrck_auto_mode is 0.** 0: 1 BCK width 1: 2 BCK width n: n+1 BCK width
18	reg_output_cr_en	**Output register data for debugging.** 0: Output normal data 1: Output register data
15	reg_lrck_reset	**Reset ETDM's counters to initial value when LRCK edge comes.** 0: Disable 1: Enable
14	reg_no_align_1x_en	**ETDM start time will align with 1x_en timing or not.** 0: Align with 1x_en 1: Not align with 1x_en

11211578 ETDM_OUT5_CON2 ETDM_OUT5 Control Register 2 00F02406

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		reg_lrck_delay_bck_inv	reg_lrck_delay_0p5t_en	reg_sdata_delay_bck_inv	reg_sdata_delay_0p5t_en		reg_monitor_sel					reg_redundant_0			reg_off_cr_en	
Type		RW	RW	RW	RW		RW					RW			RW	
Reset		0	0	0	0		0	0				1			0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_shift_auto	reg_sdata_shift		reg_mask_auto	reg_mask_num					reg_in2latch_time				
Type			RW	RW		RW	RW					RW				
Reset			1	0	0	1	0	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
30	reg_lrck_delay_bck_inv	**Invert LRCK delay BCK or not. If invert, the LRCK will delay 0.5T BCK, else the LRCK will delay 1T BCK.** 0: No invert BCK 1: Invert BCK
29	reg_lrck_delay_0p5t_en	**Whether to add 0.5T BCK delay for output LRCK.** 0: Disable 1: Enable
28	reg_sdata_delay_bck_inv	**Invert sdata delay BCK or not. If invert, the sdata will delay 0.5T BCK, else the sdata will delay 1T BCK.** 0: No invert BCK 1: Invert BCK
27	reg_sdata_delay_0p5t_en	**Whether to add 0.5T BCK delay for output sdata.** 0: Disable 1: Enable
25:24	reg_monitor_sel	**Select monitor.** 1: Input LCH 0 2: Reorder output LCH 0 else: ETDM counter
20	reg_redundant_0	**If reg_bit_length < reg_word_length, the redundant bit will fill 0 or keep original input parallel data.** 0: Keep original input parallel data 1: Fill 0
17	reg_off_cr_en	**Output register data after ETDM out disable.** 0: Disable 1: Enable
13	reg_shift_auto	**When this bit is 0, sdata delay times decided by reg_sdata_shift, if this bit is 1 will auto select delay times according to reg_fmt.** 0: Manual mode 1: Auto mode
12:11	reg_sdata_shift	**Delay sdata before output. Only valid when reg_shift_auto is 0.** 0: No delay 1: Delay 1T 2: Delay 2T 3: Delay 3T
10	reg_mask_auto	**Auto select mask number according to reg_bit_length and reg_word_length.** 0: Disable 1: Enable
9:5	reg_mask_num	**Mask bit number, only valid when reg_mask_auto is invalid.**

Bit(s)	Name	Description
		0: 0
		1: 1
		n: n
		30: 30
		31: 31
4:0	reg_in2latch_time	**When latched data transfer to next stage.**
		0: 0
		1: 1
		n: n

1121157C ETDM_OUT5_CON3 ETDM_OUT5 Control Register 3 76543210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_start_ch_pair7				reg_start_ch_pair6				reg_start_ch_pair5				reg_start_ch_pair4			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_start_ch_pair3				reg_start_ch_pair2				reg_start_ch_pair1				reg_start_ch_pair0			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	reg_start_ch_pair7	**Selects ETDM OUT channel 14/15 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
27:24	reg_start_ch_pair6	**Selects ETDM OUT channel 12/13 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
23:20	reg_start_ch_pair5	**Selects ETDM OUT channel 10/11 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
19:16	reg_start_ch_pair4	**Selects ETDM OUT channel 8/9 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
15:12	reg_start_ch_pair3	**Selects ETDM OUT channel 6/7 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
11:8	reg_start_ch_pair2	**Selects ETDM OUT channel 4/5 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
7:4	reg_start_ch_pair1	**Selects ETDM OUT channel 2/3 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)

Bit(s)	Name	Description
3:0	reg_start_ch_pair0	**Selects ETDM OUT channel 0/1 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)

11211580 ETDM_OUT5_CON4 ETDM_OUT5 Control Register 4 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_always_open_1x_en	reg_wait_last_sample		reg_relatch_en_sel					reg_ck_en_sel_manual							
Type	RW	RW		RW					RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_ck_en_sel_manual				reg_async_reset	reg_ck_en_sel_auto		reg_clock_source_sel				reg_fs_timing_sel				
Type	RW				RW	RW		RW				RW				
Reset	0	0			0	1		0	0	0		0	0	0	0	0

Bit(s)	Name	Description
31	reg_always_open_1x_en	**No matter ETDM is enable or not, ENGEN will always send 1x_en to ETDM to generate master BCK.** 0: Disable 1: Enable
30	reg_wait_last_sample	**Will wait for the last sample transfer done or not when ETDM off.** 0: Dose not wait for the last sample 1: Wait for the last sample
28:24	reg_relatch_en_sel	**Select sample rate for ETDM out re-latch function.** Domain: slave clk domain 0: connsys_i2s_ext_1x_en 1: afe_pcm0_ext_1x_en 2: afe_pcm1_ext_1x_en 4: eTDM IN0 a1sys lrck pulse 5: eTDM IN1 a1sys lrck pulse 6: eTDM IN2 a1sys lrck pulse 7: eTDM IN3 a1sys lrck pulse 8: eTDM IN4 a1sys lrck pulse 9: eTDM IN5 a1sys lrck pulse 10: eTDM IN6 a1sys lrck pulse 11: eTDM IN7 a1sys lrck pulse 12: eTDM OUT0 a1sys lrck pulse 13: eTDM OUT1 a1sys lrck pulse 14: eTDM OUT2 a1sys lrck pulse 15: eTDM OUT3 a1sys lrck pulse 16: eTDM OUT4 a1sys lrck pulse 17: eTDM OUT5 a1sys lrck pulse 18: eTDM OUT6 a1sys lrck pulse 19: eTDM OUT7 a1sys lrck pulse Domain: else 0: 8 kHz 1: 11.025 kHz 2: 12 kHz 4: 16 kHz 5: 22.05 kHz 6: 24 kHz 8: 32 kHz 9: 44 kHz

Bit(s)	Name	Description
		10: 48 kHz 13: 88.2 kHz 14: 96 kHz 17: 176.4 kHz 18: 192 kHz 21: 352.8 kHz 22: 384 kHz Else: 0
23:14	reg_ck_en_sel_manual	**When reg_ck_en_sel_auto is 0, this setting will replace the value of {reg_ch_num, reg_word_length}.**
11	reg_async_reset	**Software asynchronous reset.** 0: Normal work 1: Asynchronous reset valid
10	reg_ck_en_sel_auto	**Auto select timing or not, only valid in engen timing mode.** 0: Use manual mode to select timing (ETDM_IN_CON8[25:16]) 1: Auto select timing according to other settings
8:6	reg_clock_source_sel	**Select ETDM clock source.** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
4:0	reg_fs_timing_sel	**Select sample rate.** 0: 8 kHz 1: 12 kHz 2: 16 kHz 3: 24 kHz 4: 32 kHz 5: 48 kHz 7: 96 kHz 9: 192 kHz 11: 384 kHz 16: 11.025 kHz 17: 22.05 kHz 18: 44.1 kHz 19: 88.2 kHz 20: 176.4 kHz 21: 352.8 kHz Else: 0

11211584 ETDM_OUT5_CON5 ETDM_OUT5 Control Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_lr_swap															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_lrck_div_2	reg_repack_24b_msb_align	reg_master_ws_inv	reg_master_bck_inv	reg_slave_lrck_inv	reg_slave_bck_inv		reg_repack_chnum				reg_repack_bitnum	
Type				RW	RW	RW	RW	RW	RW		RW				RW	
Reset				0	0	0	0	0	0		0	0	0	0	0	0

Bit(s)	Name	Description
31:16	reg_lr_swap	**Swap right channel and left channel or not.** Bit 0: For channel 0/1 Bit 1: For channel 2/3 Bit n: For channel 2n/2n+1
12	reg_lrck_div_2	**divide LRCK frequency by 2** 0: Not divide 2 1: Divide 2
11	reg_repack_24b_msb_align	**Select LSB or MSB alignment.** 0: LSB 24bits is valid 1: MSB 24bits is valid
10	reg_master_ws_inv	**This bit is only valid for output LRCK in master mode.** 0: Not inverse 1: Inverse
9	reg_master_bck_inv	**This bit is only valid for output BCK in master mode.** 0: Not inverse 1: Inverse
8	reg_slave_lrck_inv	**ETDM slave LRCK inverse or not.** 0: Not inverse 1: Inverse
7	reg_slave_bck_inv	**ETDM slave BCK inverse or not.** 0: Not inverse 1: Inverse
5:2	reg_repack_chnum	**ETDM out repack channel number.** 0: 1 1: 2 n: n+1
1:0	reg_repack_bitnum	**ETDM out repack bit number.** 0: 8 bits 1: 16 bits 2: 24 bits 3: 32 bits

11211590 ETDM_OUT5_CON8 ETDM_OUT5 Control Register 8 FEDCBA98

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	reg_start_ch_pair15				reg_start_ch_pair14				reg_start_ch_pair13				reg_start_ch_pair12			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_start_ch_pair11				reg_start_ch_pair10				reg_start_ch_pair9				reg_start_ch_pair8			
Type	RW				RW				RW				RW			
Reset	1	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:28	reg_start_ch_pair15	**Selects ETDM OUT channel 30/31 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
27:24	reg_start_ch_pair14	**Selects ETDM OUT channel 28/29 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
23:20	reg_start_ch_pair13	**Selects ETDM OUT channel 26/27 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
19:16	reg_start_ch_pair12	**Selects ETDM OUT channel 24/25 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
15:12	reg_start_ch_pair11	**Selects ETDM OUT channel 22/23 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
11:8	reg_start_ch_pair10	**Selects ETDM OUT channel 20/21 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)
7:4	reg_start_ch_pair9	**Selects ETDM OUT channel 18/19 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)

Bit(s)	Name	Description
3:0	reg_start_ch_pair8	**Selects ETDM OUT channel 16/17 start channel.** 0: Start channel is 0/1 1: Start channel is 2/3 2: Start channel is 4/5 3: Start channel is 6/7 n: Start channel is (2*n)/(2*n+1)

112115E0 ETDM_4_7_COWORK_CON0 ETDM_4_7 Co-work Control Register 0 81B2A908

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									etdm_out5_slave_sel				etdm_out5_sync_sel			
Type									RW				RW			
Reset									1	0	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	etdm_out5_data_sel															
Type	RW															
Reset	1	0	1	0												

Bit(s)	Name	Description
23:20	etdm_out5_slave_sel	**Select etdmout5 slave mode source.** 0: From etdmin4 master 1: From etdmin4 slave 2: From etdmin5 master 3: From etdmin5 slave 4: From etdmin6 master 5: From etdmin6 slave 6: From etdmin7 master 7: From etdmin7 slave 8: From etdmout4 master 9: From etdmout4 slave 10: 1'b0 11: From etdmout5_slave 12: From etdmout6 master 13: From etdmout6 slave 14: From etdmout7 master 15: From etdmout7 slave
19:16	etdm_out5_sync_sel	**Select etdmout5 sync mode source.** 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 12: From etdmout6 14: From etdmout7 Else: Not allowed.
15:12	etdm_out5_data_sel	**Select etdmout5 data source.** 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 downlink 10: From etdmout5 downlink 12: From etdmout6 downlink 14: From etdmout7 downlink Else: Not allowed.

112115E4 ETDM_4_7_COWORK_CON1 ETDM_4_7 Co-work Control Register 1 0022A300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									etdm_in5_sdata1_15_sel				etdm_in5_sdata0_sel			
Type									RW				RW			
Reset									0	0	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	etdm_in5_sync_sel				etdm_in5_slave_sel											
Type	RW				RW											
Reset	1	0	1	0	0	0	1	1								

Bit(s)	Name	Description
23:20	etdm_in5_sdata1_15_sel	**Select etdmin5 sdata1 ~ sdata15 data source.** 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 10: From etdmout5 12: From etdmout6 14: From etdmout7 Else: Not allowed.
19:16	etdm_in5_sdata0_sel	**Select etdmin5 sdata0 data source.** 0: From etdmin4 2: From etdmin5 4: From etdmin6 6: From etdmin7 8: From etdmout4 10: From etdmout5 12: From etdmout6 14: From etdmout7 Else: Not allowed.
15:12	etdm_in5_sync_sel	**Select etdmin5 sync mode source.** 0: From etdmin4 4: From etdmin6 6: From etdmin7 8: From etdmout4 10: From etdmout5 12: From etdmout6 14: From etdmout7 Else: Not allowed.
11:8	etdm_in5_slave_sel	**Select etdmin5 slave mode source.** 0: From etdmin4 master 1: From etdmin4 slave 2: 1'b0 3: From etdmin5 slave 4: From etdmin6 master 5: From etdmin6 slave 6: From etdmin7 master 7: From etdmin7 slave 8: From etdmout4 master 9: From etdmout4 slave 10: From etdmout5_master

Bit(s)	Name	Description
		11: From etdmout5_slave 12: From etdmout6 master 13: From etdmout6 slave 14: From etdmout7 master 15: From etdmout7 slave

11213900 AFE_CONN_MON_CFG AFE CONNECTION MONITOR CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon_cfg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon_cfg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon_cfg	**AFE CONNECTION MONITOR CONTROL REGISTER**

11213904 AFE_CONN_MON0 AFE CONNECTION MONITOR0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon0	**AFE CONNECTION MONITOR0**

11213908 AFE_CONN_MON1 AFE CONNECTION MONITOR1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon1	**AFE CONNECTION MONITOR1**

1121390C AFE_CONN_MON2 AFE CONNECTION MONITOR2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon2	**AFE CONNECTION MONITOR2**

11213910 AFE_CONN_MON3 AFE CONNECTION MONITOR3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon3	**AFE CONNECTION MONITOR3**

11213914 AFE_CONN_MON4 AFE CONNECTION MONITOR4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon4	**AFE CONNECTION MONITOR4**

11213918 AFE_CONN_MON5 AFE CONNECTION MONITOR5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	afe_conn_mon5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	afe_conn_mon5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	afe_conn_mon5	**AFE CONNECTION MONITOR5**

11213920 AFE_CONN_RS_0 AFE CONNECTION RIGHT SHIFT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													O019_RS	O018_RS		
Type													RW	RW		
Reset													0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	O019_RS	0: No shift 1: Right shift 1 bit
18	O018_RS	0: No shift 1: Right shift 1 bit

1121392C AFE_CONN_RS_3 AFE CONNECTION RIGHT SHIFT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O125_RS	O124_RS												
Type			RW	RW												
Reset			0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29	O125_RS	0: No shift 1: Right shift 1 bit
28	O124_RS	0: No shift 1: Right shift 1 bit

11213960 AFE_CONN_16BIT_0 AFE CONNECTION 16BIT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													O019_16BIT	O018_16BIT		
Type													RW	RW		
Reset													0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	O019_16BIT	0: 32-bit 1: 16-bit
18	O018_16BIT	0: 32-bit 1: 16-bit

1121396C AFE_CONN_16BIT_3 AFE CONNECTION 16BIT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O125_16BIT	O124_16BIT												
Type			RW	RW												
Reset			0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29	O125_16BIT	0: 32-bit 1: 16-bit
28	O124_16BIT	0: 32-bit 1: 16-bit

11213980 AFE_CONN_24BIT_0 AFE CONNECTION 24BIT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													O019_24BIT	O018_24BIT		
Type													RW	RW		
Reset													0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	O019_24BIT	0: 32-bit 1: 24-bit
18	O018_24BIT	0: 32-bit 1: 24-bit

1121398C AFE_CONN_24BIT_3 AFE CONNECTION 24BIT REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			O125_24BIT	O124_24BIT												
Type			RW	RW												
Reset			0	0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29	O125_24BIT	0: 32-bit 1: 24-bit
28	O124_24BIT	0: 32-bit 1: 24-bit

11213D98 AFE_MEMIF_CON0 MEMIF related configuration 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**CPU_COMPACT_MODE**	**CPU_HD_ALIGN**	**SYSRAM_SIGN**
Type														RW	RW	RW
Reset														0	0	1

Bit(s)	Name	Description
2	CPU_COMPACT_MODE	**Selects valid 24-bit data from 32-bit write data bus** 0: 24-bit use normal mode 1: 24-bit use compact mode
1	CPU_HD_ALIGN	**Selects valid 24-bit data from 32-bit write data bus** 0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
0	SYSRAM_SIGN	**Signed extension 24-bit data to 32-bit for bus read SYSRAM** 0: Append 0 1: bit[23] signed extension

11213D9C AFE_MEMIF_RW_MON_CFG MEMIF RW Monitor 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MEMIF_RD_MON_CFG				MEMIF_WR_MON_CFG			
Type									RW				RW			
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:4	MEMIF_RD_MON_CFG	MEMIF Read Monitor CFG
3:0	MEMIF_WR_MON_CFG	MEMIF Write Monitor CFG

11213DA0 AFE_MEMIF_RD_MON MEMIF RD Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMIF_RD_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMIF_RD_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMIF_RD_MON	MEMIF RD Data

11213DA4 AFE_MEMIF_WR_MON MEMIF WR Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMIF_WR_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMIF_WR_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMIF_WR_MON	MEMIF WR Data

11213DA8 AFE_BUS_MON1 BUS Monitor1 00000000

Bit	31	30		29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		BUS_MON1															
Type		RO															
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14		13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BUS_MON1															
Type		RO															
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUS_MON1	BUS Monitor1

11213DAC **AFE_BUS_MON2** **Bus Monitor2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUS_MON2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUS_MON2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUS_MON2	Bus Monitor2

11213DB0 AFE_BUS_CFG0 BUS Debug Config 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									BUS_MON2_CFG				BUS_MON1_CFG			
Type									RW				RW			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23:20	BUS_MON2_CFG	0000b: mem_slv1_wdata[63:32] 0001b: mem_slv1_wdata[95:64] 0010b: mem_slv1_rdata[63:32] 0011b: mem1_wdata[63:32] 0100b: mem1_rdata[63:32] 0101b: afe_int_sysram_hwdata 0110b: ahb_slv_hrdata
19:16	BUS_MON1_CFG	0000b: mem_slv1_wdata[31:0] 0001b: mem_slv1_wdata[95:64] 0010b: mem_slv1_rdata[31:0] 0011b: mem1_wdata[31:0] 0100b: mem1_rdata[31:0] 0101b: ahb_slv_hwdata 0110b: ahb_slv_hrdata

11211B44 AFE_CONN018_1 AFE Connection Register 018_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**I033_O018_S**	**I032_O018_S**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O018_S	**Controls the path from I033 to O018.** 0: Off 1: On
0	I032_O018_S	**Controls the path from I032 to O018.** 0: Off 1: On

11211B50 AFE_CONN018_4 AFE Connection Register 018_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O018_S	I150_O018_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O018_S	**Controls the path from I151 to O018.** 0: Off 1: On
22	I150_O018_S	**Controls the path from I150 to O018.** 0: Off 1: On

11211B64 **AFE_CONN019_1** **AFE Connection Register 019_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**I033_O019_S**	**I032_O019_S**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O019_S	**Controls the path from I033 to O019.** 0: Off 1: On
0	I032_O019_S	**Controls the path from I032 to O019.** 0: Off 1: On

11211B70 AFE_CONN019_4 AFE Connection Register 019_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O019_S	I150_O019_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O019_S	**Controls the path from I151 to O019.** 0: Off 1: On
22	I150_O019_S	**Controls the path from I150 to O019.** 0: Off 1: On

11212884 AFE_CONN124_1 AFE Connection Register 124_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**I033_O124_S**	**I032_O124_S**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O124_S	**Controls the path from I033 to O124.** 0: Off 1: On
0	I032_O124_S	**Controls the path from I032 to O124.** 0: Off 1: On

11212890 AFE_CONN124_4 AFE Connection Register 124_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O124_S	I150_O124_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O124_S	**Controls the path from I151 to O124.** 0: Off 1: On
22	I150_O124_S	**Controls the path from I150 to O124.** 0: Off 1: On

112128A4 **AFE_CONN125_1** **AFE Connection Register 125_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															I033_O125_S	I032_O125_S
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	I033_O125_S	**Controls the path from I033 to O125.** 0: Off 1: On
0	I032_O125_S	**Controls the path from I032 to O125.** 0: Off 1: On

112128B0 AFE_CONN125_4 AFE Connection Register 125_4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									I151_O125_S	I150_O125_S						
Type									RW	RW						
Reset									0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23	I151_O125_S	**Controls the path from I151 to O125.** 0: Off 1: On
22	I150_O125_S	**Controls the path from I150 to O125.** 0: Off 1: On

11213E40 AFE_DL0_BASE_MSB AFE DL0 Base Address Register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DL0_BASE__ADDR_MSB**		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DL0_BASE__ADDR_MSB	AFE DL0 Base Address Register MSB

11213E44 AFE_DL0_BASE AFE DL0 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	DL0_BASE_ADDR	**Base address of the DL input at master mode. Please always set AFE_DL_BASE[3:0] = 4'h0 for the convenience of the hardware implementation**

11213E48 **AFE_DL0_CUR_MSB** **AFE DL0 Cursor Register MSB** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DL0_CUR_PTR_MSB**		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DL0_CUR_PTR_MSB	AFE DL0 Cursor Register MSB

11213E4C AFE_DL0_CUR AFE DL0 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DL0_CUR_PTR	**Indicates the current address of the DL input buffer**

11213E50 **AFE_DL0_END_MSB** **AFE DL0 End Address Register MSB** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**DL0_END_ADDR_MSB**		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	DL0_END_ADDR_MSB	AFE DL0 End Address Register MSB

11213E54 **AFE_DL0_END** **AFE DL0 End Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	DL0_END_ADDR	**Ending address of the DL input at master mode. Please always set AFE_DL_END[3:0] = 4'hf for the convenience of the hardware implementation**

11213E58 AFE_DL0_RCH_MON AFE Memory Interface Monitor Register RCH 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_RCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DL0_RCH_DATA	**Monitors rch memory interface output.**

11213E5C AFE_DL0_LCH_MON AFE Memory Interface Monitor Register LCH 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DL0_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_LCH_DATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DL0_LCH_DATA	**Monitors lch memory interface output.**

11213E60 AFE_DL0_CON0 AFE DL0 Agent Control Register 00310068

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DL0_ON					DL0_MINLEN				DL0_MAXLEN			
Type				RW					RW				RW			
Reset				0					0	0	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DL0_SEL_DOMAIN			DL0_SEL_FS					DL0_SW_CLEAR_BUF_EMPTY	DL0_PBUF_SIZE		DL0_MONO	DL0_NORMAL_MODE	DL0_HALIGN	DL0_HD_MODE	
Type	RW			RW					RW	RW		RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0

Bit(s)	Name	Description
28	DL0_ON	**Controls the enabling of DL memory interface path** 0: Off 1: On
23:20	DL0_MINLEN	**The minimum number of data remaining in PBUF** 0: 0 byte 1: 8 bytes 2:16 bytes 3:32 bytes 4~15: not supported
19:16	DL0_MAXLEN	0: not support 1: 16-byte burst 2: 32-byte burst 3: 64-byte burst 4~15: not supported
15:13	DL0_SEL_DOMAIN	**Controls the sampling domain** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
12:8	DL0_SEL_FS	**Controls the sampling frequency** 5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k 5'h16: 384k

Bit(s)	Name	Description
7	DL0_SW_CLEAR_BUF_EMPTY	**Clears the buf_empty monitor**
6:5	DL0_PBUF_SIZE	0: 32 bytes 1: 64 bytes 2: 128 bytes 3: 256 bytes
4	DL0_MONO	**Controls the data mode.** 0: Stereo 1: Mono
3	DL0_NORMAL_MODE	0: 24-bit use compact mode 1: 24-bit use normal mode
2	DL0_HALIGN	0: {8'b0, 24 bits data} 1: {24 bits data, 8'b0}
1:0	DL0_HD_MODE	0: 16-bit format 1: 24-bit format 2, 3: Not supported

11214220 AFE_VUL0_BASE_MSB AFE VUL0 Base Address Register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														VUL0_BASE_ADDR_MSB		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VUL0_BASE_ADDR_MSB	AFE VUL0 Base Address Register MSB

11214224 AFE_VUL0_BASE AFE VUL0 Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VUL0_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL0_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:4	VUL0_BASE_ADDR	**Base address of the VUL input at master mode. Please always set AFE_VUL_BASE[3:0] = 4'h0 for the convenience of the hardware implementation**

11214228 AFE_VUL0_CUR_MSB AFE VUL0 Cursor Register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**VUL0_CUR_PTR_MSB**		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VUL0_CUR_PTR_MSB	AFE VUL0 Cursor Register MSB

1121422C AFE_VUL0_CUR AFE VUL0 Cursor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VUL0_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL0_CUR_PTR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VUL0_CUR_PTR	**Indicates the current address of the VUL input buffer.**

11214230 AFE_VUL0_END_MSB AFE VUL0 End Address Register MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**VUL0_END_ADDR_MSB**		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	VUL0_END_ADDR_MSB	AFE VUL0 End Address Register MSB

11214234 AFE_VUL0_END AFE VUL0 End Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VUL0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:3	VUL0_END_ADDR	**Ending address of the VUL input at master mode. Please always set AFE_VUL_END[3:0] = 4'hf for the convenience of the hardware implementation**

11214238 AFE_VUL0_CON0 AFE VUL0 Agent Control Register 00000048

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				VUL0_ON												
Type				RW												
Reset				0												
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VUL0_SEL_DOMAIN			VUL0_SEL_FS					VUL0_SW_CLEAR_BUF_FULL	VUL0_WR_SIGN	VUL0_R_MONO	VUL0_MONO	VUL0_NORMAL_MODE	VUL0_HALIGN	VUL0_HD_MODE	
Type	RW			RW					RW	RW	RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
28	VUL0_ON	**Controls the enabling of VUL memory interface path** 0: Off 1: On
15:13	VUL0_SEL_DOMAIN	**Controls the sampling frequency** 3'h0: Hopping clk domain 3'h1: APLL clk domain 3'h2: SPDIF clk domain 3'h3: HDMI clk domain 3'h4: eARC clk domain 3'h5: Linein clk domain 3'h6: Slave clk domain
12:8	VUL0_SEL_FS	5'h00: 8k 5'h01: 11k 5'h02: 12k 5'h04: 16k 5'h05: 22k 5'h06: 24k 5'h08: 32k 5'h09: 44k 5'h0a: 48k 5'h0d: 88k 5'h0e: 96k 5'h11: 176k 5'h12: 192k 5'h15: 352k 5'h16: 384k
7	VUL0_SW_CLEAR_BUF_FULL	**Clear the buf_full monitor**
6	VUL0_WR_SIGN	**Signed extension 24-bit data to 32-bit for VUL memory agent** 0: append 0 1: bit[23] signed extension
5	VUL0_R_MONO	**Controls the data mono type for voice uplink memory interface path.** 0: Mono use L channel 1: Mono use R channel
4	VUL0_MONO	**Controls the data mode.** 0: Stereo 1: Mono
3	VUL0_NORMAL_MODE	0: 24-bit use compact mode 1: 24-bit use normal mode
2	VUL0_HALIGN	0: {8'b0, 24 bits data}

Bit(s)	Name	Description
1:0	VUL0_HD_MODE	1: {24 bits data, 8'b0} 0: 16-bit format 1: 24-bit format 2, 3: Not supported

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