MT7981B
Wi-Fi 6 Generation Router Platform: Registers Part 2

Open Version

Part 1: MCU and Bus Fabric
Clock and Power Control, General System
Part 2: Peripherals, Connectivity

Version: 1.0
Release Date: 2024-03-25

Version History

Version	Date	Description
1.0	2024-03-25	Initial release

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4 Peripherals

4.1 Serial Peripheral Interface (SPI) Master

4.1.1 Register Definition

Module name: spi0 Base address: (+0x1100A000)

Module name: spi1 Base address: (+0x1100B000)

Module name: spi2 Base address: (+0x11009000)

Address	Name	Width	Register Function
1100A000	SPI_CFG0	32	SPI Configuration 0 Register
1100A004	SPI_CFG1	32	SPI Configuration 1 Register
1100A008	SPI_TX_SRC	32	SPI Tx Source Address Register
1100A00C	SPI_RX_DST	32	SPI Rx Destination Address Register
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1100A030	SPI_RX_EXT_ADDR	32	SPI_DMA_RX_src_extend_address
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1100A000 SPI_CFG0 SPI Configuration 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CS_SETUP_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CS_HOLD_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CS_SETUP_COUNT	**Chip select setup time = (CS_SETUP_COUNT + 1)*CLK_PERIOD; CLK_PERIOD is the cycle time of the clock SPI engine adopts.**
15:0	CS_HOLD_COUNT	**Chip select hold time = (CS_HOLD_COUNT+1)*CLK_PERIOD**

1100A004 **SPI_CFG1** **SPI Configuration 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PACKET_LOOP_CNT								CS_IDLE_COUNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PACKET_LENGTH	**Packet length** The transmission on the SPI bus consists of unit bytes. Hence, PACKET_LENGTH[15:0] define the number of bytes in one packet. Number of bytes in one packet = PACKET_LENGTH + 1
15:8	PACKET_LOOP_CNT	**PACKET_LENGTH[15:0] define the number of bytes in one packet; PACKET_LOOP_CNT[7:0] define the number of packets within one transaction.** Number of bytes in one packet = PACKET_LENGTH + 1 Number of packets in one transaction = PACKET_LOOP_CNT + 1 Total bytes of one transaction = (PACKET_LENGTH + 1)*(PACKET_LOOP_CNT + 1)
7:0	CS_IDLE_COUNT	**Chip select idle time between consecutive transaction = (CS_IDLE_COUNT + 1)*CLK_PERIOD**

1100A008 SPI_TX_SRC SPI Tx Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_SRC	**If TX_DMA_EN is set, the data to be put on the MOSI line will be kept in memory in advance, and the SPI controller will automatically read the data from memory.** SPI_TX_SRC defines the memory address from which SPI controller starts to read data.

1100A00C SPI_RX_DST SPI Rx Destination Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DST	**If RX_DMA_EN is set, the received data from the MISO line will be moved to memory automatically by the SPI controller.** SPI_RX_DST defines the memory address to which the SPI controller starts to store the data.

1100A010 SPI_TX_DATA SPI Tx Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_TX_DATA	**The depth of the Tx FIFO is 32*4 bytes.** Writing to this register will write 4 bytes to Tx FIFO. The Tx FIFO pointer will automatically move towards the next four bytes. Reading from this register will read 4 bytes from FIFO, and the Tx FIFO pointer will automatically move towards the next four bytes.

1100A014 SPI_RX_DATA SPI Rx Data FIFO 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPI_RX_DATA	**The depth of the Rx FIFO is 32*4 bytes.** Reading from this register will read 4 bytes from Rx FIFO. The Rx FIFO pointer will automatically move towards the next four bytes. Writing to this register will write 4 bytes to FIFO, and the Rx FIFO pointer will automatically move towards the next four bytes.

1100A018 SPI_CMD SPI Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								GET_TICK_DLY			SPIM_LOOP		NONIDLE_MODE	CS_PIN_SEL	PAUSE_IE	FINISH_IE
Type								RW			RW		RW	RW	RW	RW
Reset								0	0	0	0		0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_ENDIAN	RX_ENDIAN	RXMSBF	TXMSBF	TX_DMA_EN	RX_DMA_EN	CPOL	CPHA	CS_POL	SAMPLE_SEL	CS_DEASSERT_EN	PAUSE_EN		RST	RESUME	CMD_ACT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0

Bit(s)	Name	Description
24:22	GET_TICK_DLY	**If the speed of SPI is not fast enough, these three bits can help tolerate get_tick timing.** The timing range between get_tick is one cycle depending on the SPI system clock.
21	SPIM_LOOP	**Set up SPM_LOOP, and MISO will connect to MOSI.**
19	NONIDLE_MODE	**Set NONIDLE_MODE = 1, and SPI will transfer without idle time until the packet length is done.**
18	CS_PIN_SEL	**Selects the CS pin to use** If enabled, the CS pin will depend on reg_CS_POL. 0: Select CS_N 1: Select GPIO
17	PAUSE_IE	**Interrupt enable bit of the pause flag in SPI status register**
16	FINISH_IE	**Interrupt enable bit of the finish flag in SPI status register**
15	TX_ENDIAN	**Defines whether to reverse the endian order of the data DMA from memory** Only supported in DMA mode. 0: Not reverse (default)
14	RX_ENDIAN	**Defines whether to reverse the endian order of the data DMA to memory** 0: Not reverse (default)
13	RXMSBF	**Indicates data received from MISO line is MSB first or not** Set RXMSBF to 1 for MSB first; otherwise set it to 0.
12	TXMSBF	**Indicates data sent on MOSI line is MSB first or not** Set TXMSBF to 1 for MSB first; otherwise set it to 0.
11	TX_DMA_EN	**DMA mode enable bit of the data to be transmitted** 0: Not enable (default)

Bit(s)	Name	Description
10	RX_DMA_EN	**DMA mode enable bit of the data received** 0: Not enable (default)
9	CPOL	**Control bit of SCK polarity** 0: CPOL = 0 1: CPOL = 1
8	CPHA	**Defines SPI Clock Format 0 or SPI Clock Format 1 during transmission** 0: CPHA = 0 1: CPHA = 1
7	CS_POL	**Control bit of chip select polarity revert** 0: Active low 1: Active high
6	SAMPLE_SEL	**Control bit of sample edge of MISO** 0: Positive edge 1: Negative edge
5	CS_DEASSERT_EN	**Enable bit of chip select deassertion mode** Set this to 1 to enable this mode.
4	PAUSE_EN	**Enable bit of pause mode** Set this to 1 to enable this mode.
2	RST	**Software reset bit** When this is active, all modules of SPI except for SPI registers will be reset. When this bit is 1, software reset will be active high. Default: 0
1	RESUME	**Used when controller is in PAUSE IDLE state** Write 1 to this bit to trigger the SPI controller to resume transfer from PAUSE IDLE state.
0	CMD_ACT	**Command activate bit** Write 1 to this bit to trigger the SPI controller to start the transaction.

1100A01C SPI_IRQ SPI IRQ Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**PAUSE**	**FINISH**
Type															RC	RC
Reset															0	0

Bit(s)	Name	Description
1	PAUSE	**Interrupt status bit in pause mode** Will be set by the SPI controller when it completes the transaction, entering the PAUSE IDLE state.
0	FINISH	**Interrupt status bit in non-pause mode** Will be set by the SPI controller when it completes the transaction, entering the IDLE state.

1100A020 SPI_STATUS SPI Status Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**BUSY**
Type																RO
Reset																1

Bit(s)	Name	Description
0	BUSY	**Status flag reflecting SPI controller is busy or not** This bit is low active; 0 means the SPI controller is busy now. 1'b0: Busy 1'b1: Idle

1100A028 **SPI_CFG2** **SPI_CFG2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCK_LOW_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCK_HIGH_COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SCK_LOW_COUNT	**SCK clock low time = (SCK_LOW_COUNT + 1)*CLK_PERIOD**
15:0	SCK_HIGH_COUNT	**SCK clock high time = (SCK_HIGH_COUNT + 1)*CLK_PERIOD**

1100A02C SPI_TX_EXT_ADDR SPI_DMA_TX_src_extend_address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_TX_EXTEND_ADDR			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_TX_EXTEND_ADDR	**SPI DMA read extend base address**

1100A030 SPI_RX_EXT_ADDR SPI_DMA_RX_src_extend_address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_RX_EXTEND_ADDR			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_RX_EXTEND_ADDR	**SPI DMA write extend base address**

1100A040 SPI_CFG3 SPI_CFG3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SPI_DUMMY_BITLEN			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPI_ADDR_BYTELEN				SPI_CMD_BYTELEN						SPI_NODATA_FLAG	SPI_XMODE_EN	SPI_HALF_DUPLEX_EN	SPI_HALF_DUPLEX_DIR	SPI_PIN_MODE	
Type	RW				RW						RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
19:16	SPI_DUMMY_BITLEN	**SPI dummy data bit length** If set to 0, there will be no dummy data transferred. This register is valid only when SPI_CMD_BYTELEN is not 0.
15:12	SPI_ADDR_BYTELEN	**SPI address byte length** If set to 0, there will be no address transferred. This register is valid only when SPI_CMD_BYTELEN is not 0.
11:8	SPI_CMD_BYTELEN	**SPI command byte length** If set to 0, there will be no command transferred.
5	SPI_NODATA_FLAG	**SPI data phase flag bit** If set to 1, there will be no data phase transferred when packet_length is 0.
4	SPI_XMODE_EN	**SPI XMODE enable bit** If XMODE is enabled, the address phase and dummy data phase will be transferred in single mode. Otherwise, they will be transferred in the same pin mode as data phase. 0: Disable 1: Enable
3	SPI_HALF_DUPLEX_EN	**SPI half-duplex mode enable bit** 0: Disable 1: Enable
2	SPI_HALF_DUPLEX_DIR	**SPI transfer direction for half-duplex mode** This bit is valid for single/dual/quad mode half-duplex. 0: Tx 1: Rx
1:0	SPI_PIN_MODE	**SPI pin mode** 0: Single mode

Bit(s)	Name	Description
		1: Dual mode 2: Quad mode

4.2 NAND Flash Interface (NFI)

4.2.1 Register Definition

Module name: NFI Base address: (+0x11005000)

Address	Name	Width	Register Function
11005000	NFI_CNFG	16	NFI Configuration
11005004	NFI_PAGEFMT	32	NFI Page Format Control Register
11005008	NFI_CON	32	NFI Operation Control Register
1100500C	NFI_ACCCON	32	NAND Flash Access Timing Control register
11005010	NFI_INTR_EN	32	NFI Interrupt Enable Register
11005014	NFI_INTR	32	NFI Interrupt Status Register
11005020	NFI_CMD	32	NFI Command Register
11005030	NFI_ADDRNOB	32	NFI Address Length Register
11005034	NFI_COLADDR	32	NFI Column Address Register
11005038	NFI_ROWADDR	32	NFI Row Address Register
11005040	NFI_STRDATA	16	NFI Data Transfer Start Trigger Register
11005044	NFI_CNRNB	16	NFI Check NAND Ready/Busy Register
11005050	NFI_DATAW	32	NFI Write Data Buffer
11005054	NFI_DATAR	32	NFI Read Data Buffer
11005058	NFI_PIO_DIRDY	16	PIO_mode Data Ready Register
11005060	NFI_STA	32	NFI State
11005064	NFI_FIFOSTA	16	NFI FIFO Status
11005070	NFI_ADDRCNTR	32	NFI Page Address Counter Register
11005080	NFI_STRADDR	32	NFI AHB Start Address Register
11005084	NFI_BYTELEN	32	NFI DMA Byte Length Register
11005090	NFI_CSEL	16	NFI Device Select Register
11005094	NFI_IOCON	32	NFI IO Control register
110050A0	NFI_FDM0L	32	NFI Least FDM Data for Sector 0 Register
110050A4	NFI_FDM0M	32	NFI Most FDM Data for Sector 0 Register
110050A8	NFI_FDM1L	32	NFI Least FDM Data for Sector 1 Register
110050AC	NFI_FDM1M	32	NFI Most FDM Data for Sector 1 Register
110050B0	NFI_FDM2L	32	NFI Least FDM Data for Sector 2 Register
110050B4	NFI_FDM2M	32	NFI Most FDM Data for Sector 2 Register
110050B8	NFI_FDM3L	32	NFI Least FDM Data for Sector 3 Register
110050BC	NFI_FDM3M	32	NFI Most FDM Data for Sector 3 Register
110050C0	NFI_FDM4L	32	NFI Least FDM Data for Sector 4 Register
110050C4	NFI_FDM4M	32	NFI Most FDM Data for Sector 4 Register
110050C8	NFI_FDM5L	32	NFI Least FDM Data for Sector 5 Register
110050CC	NFI_FDM5M	32	NFI Most FDM Data for Sector 5 Register
110050D0	NFI_FDM6L	32	NFI Least FDM Data for Sector 6 Register
110050D4	NFI_FDM6M	32	NFI Most FDM Data for Sector 6 Register
110050D8	NFI_FDM7L	32	NFI Least FDM Data for Sector 7 Register
110050DC	NFI_FDM7M	32	NFI Most FDM Data for Sector 7 Register
110050E0	NFI_FDM8L	32	NFI Least FDM Data for Sector 8 Register
110050E4	NFI_FDM8M	32	NFI Most FDM Data for Sector 8 Register
110050E8	NFI_FDM9L	32	NFI Least FDM Data for Sector 9 Register
110050EC	NFI_FDM9M	32	NFI Most FDM Data for Sector 9 Register
110050F0	NFI_FDMAL	32	NFI Least FDM Data for Sector A Register
110050F4	NFI_FDMAM	32	NFI Most FDM Data for Sector A Register
110050F8	NFI_FDMBL	32	NFI Least FDM Data for Sector B Register
110050FC	NFI_FDMBM	32	NFI Most FDM Data for Sector B Register
11005100	NFI_FDMCL	32	NFI Least FDM Data for Sector C Register

Address	Name	Width	Register Function
11005104	NFI_FDMCM	32	NFI Most FDM Data for Sector C Register
11005108	NFI_FDMDL	32	NFI Least FDM Data for Sector D Register
1100510C	NFI_FDMDM	32	NFI Most FDM Data for Sector D Register
11005110	NFI_FDMEL	32	NFI Least FDM Data for Sector E Register
11005114	NFI_FDMEM	32	NFI Most FDM Data for Sector E Register
11005118	NFI_FDMFL	32	NFI Least FDM Data for Sector F Register
1100511C	NFI_FDMFM	32	NFI Most FDM Data for Sector F Register
11005120	NFI_CRC01	32	NFI CRC Data for Sectors 0 and 1 Register
11005124	NFI_CRC23	32	NFI CRC Data for Sectors 2 and 3 Register
11005128	NFI_CRC45	32	NFI CRC Data for Sectors 4 and 5 Register
1100512C	NFI_CRC67	32	NFI CRC Data for Sectors 6 and 7 Register
11005130	NFI_CRC89	32	NFI CRC Data for Sectors 8 and 9 Register
11005134	NFI_CRCAB	32	NFI CRC Data for Sectors A and B Register
11005138	NFI_CRCCD	32	NFI CRC Data for Sectors C and D Register
1100513C	NFI_CRCEF	32	NFI CRC Data for Sectors E and F Register
11005190	NFI_FIFODATA0	32	NFI FIFO Content Data 0
11005194	NFI_FIFODATA1	32	NFI FIFO Content Data 1
11005198	NFI_FIFODATA2	32	NFI FIFO Content Data 2
1100519C	NFI_FIFODATA3	32	NFI FIFO Content Data 3
11005200	NFI_MCON	16	NFI LCD Monitor Control Register
11005204	NFI_TOTALCNT	32	NFI LCD Monitor Total Cycle Count
11005208	NFI_RQCNT	32	NFI LCD Monitor Request Cycle Count
1100520C	NFI_ACCNT	32	NFI LCD Monitor Access Cycle Count
11005220	NFI_DEBUG_CON1	32	NFI Debug Register
11005224	NFI_MASTER_STA	32	NFI Master Status
11005228	NFI_MASTER_RST	32	NFI Master Control Register
1100522C	NFI_SECCUS_SIZE	32	Customized Size for the Last Sector
11005230	NFI_SPIADDRCNTR	32	NFI AHB Start Address Register
11005234	NFI_SPIBYTELEN	32	NFI DMA Byte Length Register
11005238	NFI_RANDOM_CNFG	32	Randomizer Configuration
1100523C	NFI_ENMPTY_THRESH	32	Empty Threshold Setting
11005240	NFI_NAND_TYPE_CNFG	32	Toggle/Synchronous/Asynchronous Interface and Timing Mode Setting
11005244	NFI_ACCCON1	32	NFI Access Timing Setting1
11005248	NFI_DELAY_CTRL	32	DQS and DQ Delay Control
1100524C	RANDOM_TSB_SEED0	32	TOSHIBA seed0
11005250	RANDOM_TSB_SEED1	32	TOSHIBA seed1
11005254	RANDOM_TSB_SEED2	32	TOSHIBA seed2
11005258	RANDOM_TSB_SEED3	32	TOSHIBA seed3
1100525C	RANDOM_TSB_SEED4	32	TOSHIBA seed4
11005260	RANDOM_TSB_SEED5	32	TOSHIBA seed5
11005264	RANDOM_TSB_SEED6	32	TOSHIBA seed6
11005268	RANDOM_TSB_SEED7	32	TOSHIBA seed7
1100526C	RANDOM_TSB_SEED8	32	TOSHIBA seed8
11005270	RANDOM_TSB_SEED9	32	TOSHIBA seed9
11005274	RANDOM_TSB_SEED10	32	TOSHIBA seed10
11005278	RANDOM_TSB_SEED11	32	TOSHIBA seed11
1100527C	RANDOM_TSB_SEED12	32	TOSHIBA seed12
11005280	RANDOM_TSB_SEED13	32	TOSHIBA seed13
11005284	RANDOM_TSB_SEED14	32	TOSHIBA seed14
11005288	RANDOM_TSB_SEED15	32	TOSHIBA seed15
11005490	NFI_FLUSH	32	NFI Software Reset Status
11005500	SNF_MAC_CTL	32	Serial NAND Flash MAC Mode Control
11005504	SNF_MAC_OUTL	32	Serial NAND Flash MAC Mode Output Data Length
11005508	SNF_MAC_INL	32	Serial NAND Flash MAC Mode Input Data Length
1100550C	SNF_RD_CTL1	32	Serial NAND Flash Read Control 1

Address	Name	Width	Register Function
11005510	SNF_RD_CTL2	32	Serial NAND Flash Read Control 2
11005514	SNF_RD_CTL3	32	Serial NAND Flash Read Control 3
11005518	SNF_GF_CTL1	32	Serial NAND Flash Get Feature Control 1
11005520	SNF_GF_CTL3	32	Serial NAND Flash Get Feature Control3
11005524	SNF_PG_CTL1	32	Serial NAND Flash Program Control1
11005528	SNF_PG_CTL2	32	Serial NAND Flash Program Control2
1100552C	SNF_PG_CTL3	32	Serial NAND Flash Program Control3
11005530	SNF_ER_CTL	32	Serial NAND Flash Erase Control
11005534	SNF_ER_CTL2	32	Serial NAND Flash Erase Control 2
11005538	SNF_MISC_CTL	32	Serial NAND Flash MISC Control
1100553C	SNF_MISC_CTL2	32	Serial NAND Flash MISC Control 2
11005540	SNF_DLY_CTL1	32	Serial NAND Flash Delay Control Setting 1
11005544	SNF_DLY_CTL2	32	Serial NAND Flash Delay Control Setting 2
11005548	SNF_DLY_CTL3	32	Serial NAND Flash Control Setting 3
1100554C	SNF_DLY_CTL4	32	Serial NAND Flash Delay Control Setting 4
11005550	SNF_STA_CTL1	32	Serial NAND Flash Status1 Register
11005554	SNF_STA_CTL2	32	Serial NAND Flash Status2 Register
11005558	SNF_STA_CTL3	32	Serial NAND Flash Status3 Register
1100555C	SNF_SNF_CNFG	32	SPI/Parallel NAND Selection
11005560	SNF_DEBUG_SEL	32	DEBUG MUX Selection
11005800	SPI_GPRAM_ADDR	32	GPRAM Start Address

11005000 **NFI_CNFG** **NFI Configuration** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		OP_MODE					AUTO_FMT_EN	HW_ECC_EN	CRC_EN	BYTE_RW	SS_RANDOMIZER_SEL	RESEED_SEC_EN		DMA_BURST_EN	READ_MODE	DMA_MODE
Type		RW					RW	RW	RW	RW	RW	RW		RW	RW	RW
Reset		0	0	0			0	0	0	0	1	0		0	0	0

Bit(s)	Name	Description
14:12	OP_MODE	**The field controls the operating process flow of FSM for NFI.** 000b: Idle state 001b: Read Process. Recommended for basic read operations 010b: Single Read Process. Recommend for reading ID and reading status 011b: Program Process. Recommended for basic program operations 100b: Erase Process. Recommended for basic erase operations 101b: Reset Process. Recommended for basic reset operations 110b: Custom Process. Recommended for all advanced operations Others: Reserved
9	AUTO_FMT_EN	**Automatic HW ECC encode or decode enable** If this bit is enabled, the ECC parity from HW ECC engine and FDM data from register are written automatically to the spare area. If this bit is disabled, the spare data all come from PIO register, like DATAR, DATAW, (PIO Mode) or the memory (DMA Mode) as main area data.
8	HW_ECC_EN	**This field is used to enable encoding or decoding operation of HW ECC engine. If this bit is enabled, the data is transferring to ECC engine for encoding and decoding. The ECC engine should be configured as NFI encoding mode; otherwise, the NFI will hang.**
7	CRC_EN	**Enable CRC data auto generation after main data and fdm data.**
6	BYTE_RW	**Enable byte access. The valid bytes read from NFI_DATAR and NFI_DATAW are only DR0 and DW0 if BYTE_RW is enabled.**
5	SS_RANDOMIZER_SEL	0: TOSHIBA 1: Samsung
4	RESEED_SEC_EN	**If this bit is enabled, HW will reload initial seed to randomize for each sector; otherwise, it will reload seed for each page.** 0: Reseed for each page 1: Reseed for each sector

Bit(s)	Name	Description
2	DMA_BURST_EN	**When NFI is in DMA mode, single and burst (incremental) transition types are used. If start address is not aligned, single transition will automatically be issued till address is aligned when DMA_BURST_EN is enabled in DMA mode.** 0: Disable DMA burst transaction 1: Enable DMA burst transaction
1	READ_MODE	**This field is used to control the activity of read or write transfer.** 0: Write operation of DMA or PIO 1: Read operation of DMA or PIO
0	DMA_MODE	**This field is used to control the operation mode.** 0: PIO mode. All data (including read or write) are moved by MCU through APB access. 1: DMA mode. All data (including read or write) are moved by HW automation through AHB.

11005004 NFI_PAGEFMT NFI Page Format Control Register 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											SPARE_SIZE					
Type											RW					
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM_ECC_NUM				FDM_NUM								DBYTE_EN	SEC_SEL_512	DATA_AREA_PAGE_SIZE	
Type	RW				RW								RW	RW	RW	
Reset	0	0	0	0	0	0	0	0					0	1	0	0

Bit(s)	Name	Description
21:16	SPARE_SIZE	**The fields represent the spare size value for each sector. If sec_size is 1K (sel_sec_512 is 0), spare size will be doubled.** 0000b: 16 bytes 0001b: 26 bytes 0010b: 27 bytes 0011b: 28 bytes 0100b: 32 bytes 0101b: 36 bytes 0110b: 40 bytes 0111b: 44 bytes 1000b: 48 bytes 1001b: 49 bytes 1010b: 50 bytes 1011b: 51 bytes 1100b: 52 bytes 1101b: 62 bytes 1110b: 61 bytes 1111b: 63 bytes 10000b: 64 bytes 10001b: 67 bytes 10010b: 74 bytes
15:12	FDM_ECC_NUM	**The number of each FDM data for HW ECC protection. The valid number of bytes range is from 0 to 8.**
11:8	FDM_NUM	**The FDM data number for each spare area. The valid number of bytes range is from 0 to 8.**

Bit(s)	Name	Description
3	DBYTE_EN	**Enable 16-bit I/O bus interface** 1: 16-bit IOBUS 0: 8-bit IOBUS
2	SEC_SEL_512	**sec_size selection** 1: Sec size: 512B 0: Sec size: 1024B
1:0	DATA_AREA_PAGE_SIZE	**Page size of data area (The real page size will include data area and (spare_size* sec_num) bytes spare area). The field specifies the size of one page for the device. Some most widely used page sizes are supported.** 00b: The page size is 512B if sel_sec_size is 1; otherwise, page size is 2 KB. 01b: The page size is 2kB if sel_sec_size is 1; otherwise, page size is 4 KB. 10b: The page size is 4kB if sel_sec_size is 1; otherwise, page size is 8 KB. 11b: Reserved if sel_sec_size is 1; otherwise, page size is 16 KB.

11005008 NFI_CON NFI Operation Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SEC_NUM
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_NUM						BWR	BRD	NOB			SRD			NFI_RST	FIFO_FLUSH
Type	RW						RW	RW	RW			WO			WO	WO
Reset	0	0	0	0			0	0	0	0	0	0			0	0

Bit(s)	Name	Description
16:12	SEC_NUM	**The field represents the sector number to be retrieved from the device or DMA master. The valid number ranges from 1 to 16.**
9	BWR	**Burst write mode. Setting to be logic-1 enables the data burst write operation.**
8	BRD	**Burst read mode. Setting this field to be logic-1 enables the data read operation. The NFI core will issue read cycles to retrieve data from the device when the data FIFO is not full or the device is not in the busy state. The NFI core supports consecutive page reading.**
7:5	NOB	**The field represents the number of bytes to be retrieved from the device in single mode, and the number of bytes per APB transaction in both single and burst modes. If device is 16-bit IO or sync/toggle interface, the read bytes number will double.** 0: Read 8 bytes from the device. 1: Read 1 byte from the device. 2: Read 2 bytes from the device. 3: Read 3 bytes from the device. 4: Read 4 bytes from the device. 5: Read 5 byte from the device. 6: Read 6 bytes from the device. 7: Read 7 bytes from the device.
4	SRD	**Setting to be logic-1 initializes the one-shot data read operation. It is mainly used for read ID and read status command, which requires no more than 4 read cycles to retrieve data from the device. It is used when FIFO is empty or after resetting nficore.**
1	NFI_RST	**Reset the state machine, data FIFO (0x0000) and FDM data (0xffff)** One pulse valid
0	FIFO_FLUSH	**Flush the data FIFO** One pulse valid

1100500C NFI_ACCCON NAND Flash Access Timing Control register F3FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	POECS				PRECS						C2R					
Type	RW				RW						RW					
Reset	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	W2R				WH				WST				RLT			
Type	RW				RW				RW				RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:28	POECS	**The field represents the minimum required time for CS post-pulling down after the access to device.** Minimum required time = PRECS[1:0] + PRECS[2]*8 + PRECS[3]*64 (T)
27:22	PRECS	**The field represents the minimum required time for CS pre-pulling down before any access to device.** Minimum required time = PRECS[1:0] + PRECS[3:2]*8 + PRECS[5:4]*128 (T)
21:16	C2R	**The field represents the minimum required time from NCEB low to NREB low. It is in unit of 2T.** Minimum required time = C2R[5:0]*2 + 1 (T)
15:12	W2R	**The field represents the minimum required time from NWEB high to NREB low. It is in unit of 2T. So, the actual time ranges from 0T to 30T in step of 2T.** Minimum required time = W2R[3:0]*2 + 1 (T)
11:8	WH	**Write-enable hold-time.** The field specifies the hold time of NALE, NCLE, NCEB signals relative to the rising edge of NWEB. This field is associated with WST to expand the write cycle time, and is associated with RLT to expand the read cycle time. 00b: No wait state 01b: 1T wait state 10b: 2T wait state 11b: 3T wait state
7:4	WST	**Write Wait State** The field specifies the wait states to be inserted to meet the requirement of the pulse width of the NWEB signal. 00b: No wait state 01b: 1T wait state 10b: 2T wait state

Bit(s)	Name	Description
		11b: 3T wait state
3:0	RLT	**Read Latency Time** The field specifies how many wait states to be inserted to meet the requirement of the read access time(tREA) for the device. 00b: No wait state 01b: 1T wait state 10b: 2T wait state 11b: 3T wait state

11005010 NFI_INTR_EN NFI Interrupt Enable Register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_IRQ_INTR_EN															
Type	RW															
Reset	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ALL_READ_INTR_EN	EARLY_READ_INTR_EN	AUTO_BLKER_INTR_EN	AUTO_READ_INTR_EN	AUTO_PROGRAM_INTR_EN	CUSTOM_READ_INTR_EN	CUSTOM_PROGRAM_INTR_EN	AHB_DONE_EN	ACCESS_LOCK_EN	BUSY_RETURN_EN	ERASE_DONE_EN	RESET_DONE_EN	WR_DONE_EN	RD_DONE_EN
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	NFI_IRQ_INTR_EN	**If this bit is enabled, an event can trigger CPU IRQ process; if this bit is 0, you can only get NFI IRQ status by reading register NFI_INTR.**
13	ALL_READ_INTR_EN	**Enables all read interrupts**
12	EARLY_READ_INTR_EN	**Enables early read interrupts**
11	AUTO_BLKER_INTR_EN	**Enables the done interrupt for SPI auto block erase**
10	AUTO_READ_INTR_EN	**Enables the done interrupt for SPI auto read**
9	AUTO_PROGRAM_INTR_EN	**Enables the done interrupt for SPI auto program**
8	CUSTOM_READ_INTR_EN	**Enables the done interrupt for SPI custom read**
7	CUSTOM_PROGRAM_INTR_EN	**Enables the done interrupt for SPI custom program**
6	AHB_DONE_EN	**Enables the done interrupt for DMA mode**
5	ACCESS_LOCK_EN	**Enables the NFI access locked interrupt.**
4	BUSY_RETURN_EN	**Enables the busy return interrupt**
3	ERASE_DONE_EN	**Enables the erase completion interrupt**
2	RESET_DONE_EN	**Enables the reset completion interrupt**
1	WR_DONE_EN	**Enables the single page write completion interrupt**
0	RD_DONE_EN	**Enables the single page read completion interrupt**

11005014 NFI_INTR NFI Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ALL_READ_INTR	EARLY_READ_INTR	AUTO_BLKER_INTR	AUTO_READ_INTR	AUTO_PROGRAM_INTR	CUSTOM_READ_INTR	CUSTOM_PROGRAM_INTR	AHB_DONE	ACCESS_LOCK	BUSY_RETURN	ERASE_DONE	RESET_DONE	WR_DONE	RD_DONE
Type			RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	ALL_READ_INTR	**Indicates that all reading is completed.**
12	EARLY_READ_INTR	**Indicates that the early reading is completed.**
11	AUTO_BLKER_INTR	**Indicates that the SPI auto erasing is completed.**
10	AUTO_READ_INTR	**Indicates that the SPI auto reading is completed.**
9	AUTO_PROGRAM_INTR	**Indicates that the SPI auto programming is completed.**
8	CUSTOM_READ_INTR	**Indicates that the SPI custom reading is completed.**
7	CUSTOM_PROGRAM_INTR	**Indicates that the SPI custom programming is completed.**
6	AHB_DONE	**Indicates that the AHB operation is completed.**
5	ACCESS_LOCK	**Indicates that the NFI access locked operation is completed.**
4	BUSY_RETURN	**Indicates that the device state returns from busy by inspecting the R/B# pin.**
3	ERASE_DONE	**Indicates that the erase operation is completed.**
2	RESET_DONE	**Indicates that the reset operation is completed.**
1	WR_DONE	**Indicates that the write operation is completed.**
0	RD_DONE	**Indicates that the single page read operation is completed.**

11005020 NFI_CMD NFI Command Register 00004545

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PROG_CMD2								CMD							
Type	RW								RW							
Reset	0	1	0	0	0	1	0	1	0	1	0	0	0	1	0	1

Bit(s)	Name	Description
15:8	PROG_CMD2	**Programmed command word (Only used in program IRQ improvement)**
7:0	CMD	**Command word**

11005030 NFI_ADDRNOB NFI Address Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										ROW_ADDR_NOB				COL_ADDR_NOB		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	ROW_ADDR_NOB	**Number of bytes for the row address**
2:0	COL_ADDR_NOB	**Number of bytes for the column address**

11005034 NFI_COLADDR NFI Column Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COL_ADDR3								COL_ADDR2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_ADDR1								COL_ADDR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	COL_ADDR3	**The 3rd column address byte**
23:16	COL_ADDR2	**The 2nd column address byte**
15:8	COL_ADDR1	**The 1st column address byte**
7:0	COL_ADDR0	**The 0th column address byte**

11005038 NFI_ROWADDR NFI Row Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ROW_ADDR3								ROW_ADDR2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROW_ADDR1								ROW_ADDR0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ROW_ADDR3	**The 3rd row address byte**
23:16	ROW_ADDR2	**The 2nd row address byte**
15:8	ROW_ADDR1	**The 1st row address byte**
7:0	ROW_ADDR0	**The 0th row address byte**

11005040 NFI_STRDATA NFI Data Transfer Start Trigger Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**STR_DATA**
Type																WO
Reset																0

Bit(s)	Name	Description
0	STR_DATA	**This signal triggers the data transfer for read or write. It only takes effect as custom operation mode.**

11005044 NFI_CNRNB NFI Check NAND Ready/Busy Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**CB2R_TIME**							**STR_CNRNB**
Type									RW							WO
Reset									0	0	0	0				0

Bit(s)	Name	Description
7:4	CB2R_TIME	**These time-out registers are for polling the NAND busy/ready signal. The unit is 16T clock cycles. The clock rate is 61.44 MHz in normal mode. It will be slowed down after enabling HW DCM mode.**
0	STR_CNRNB	**This signal triggers NFI to poll the status of the NAND busy/ready signal after CB2R_TIME*16 cycles. This function is used to avoid the fail function of "BUSY2READY" status or "BUSY_RETURN" interrupt when NAND is operating at very low frequency (< 7 MHz). If NAND is operating at a lower frequency, the sampling for the event, NAND busy/ready signal from low to high, may fail and NFI will hang in the busy state. This signal is a timeout register to check the NAND status. The results will be reported to "BUSY2READY" status and "BUSY_RETURN" interrupt.**

11005050 NFI_DATAW NFI Write Data Buffer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DW3								DW2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DW1								DW0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DW3	**Write data byte 3**
23:16	DW2	**Write data byte 2**
15:8	DW1	**Write data byte 1**
7:0	DW0	**Write data byte 0**

11005054 NFI_DATAR NFI Read Data Buffer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DR3								DR2							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DR1								DR0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DR3	**Read data byte 3**
23:16	DR2	**Read data byte 2**
15:8	DR1	**Read data byte 1**
7:0	DR0	**Read data byte 0**

11005058 NFI_PIO_DIRDY PIO_mode Data Ready Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PIO_DI_RDY
Type																RO
Reset																1

Bit(s)	Name	Description
0	PIO_DI_RDY	**Indicates the PIO mode is ready for reading data in read mode and ready for writing data in write mode.** 0: NFI_DATAR and NFI_DATAW should not be read or written (not ready). 1: NFI is ready for reading data in read mode and writing data in write mode.

11005060 NFI_STA NFI State 00001020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NAND_FSM_TYPE		NAND_FSM										NFI_FSM			
Type	RO		RO										RO			
Reset	0	0	0	0	0	0	0	0	0				0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				READ_EMPTY			BUSY2READY	BUSY			FLASH_MACRO_IDLE	ACCESS_LOCK	DATAW	DATAR	ADDR	CMD
Type				RO			RO	RO			RO	RO	RO	RO	RO	RO
Reset				1			0	0			1	0	0	0	0	0

Bit(s)	Name	Description
31:30	NAND_FSM_TYPE	**The field represents the state of NAND interface FSM type: Async state, Sync state Toggle state (eif_state[8:7]).** 00b: Async_FSM 01b: Toggle_FSM 10b: Sync_FSM 11b: Reserved
29:23	NAND_FSM	**The field represents the state of NAND interface FSM (eif_state[6:0]).** 000000b: IDLE. Idle state. 111000b: PRE_CS. Pre-CS state 001001b: CMD_WRST. Command write set-up 001010b: CMD_WR. Command write enable 001011b: CMD_WRHD. Command write hold 001000b: CMD_WRRDY 010001b: ADDR_WRST. Address write set-up 0100010b: ADDR_WR. Address write enable 0100011b: ADDR_WRHD. Address write hold 0101111b: ADDR_WRRDY 0111111b: CA2DEXT. Command address write extension 1001100b: DATA_RDST. Data read set-up 1000010b: DATA_RD. Data read enable 1000011b: DATA_RDHD. Data read hold 1101100b: DATA_WRST. Data write set-up 1100010b: DATA_WR. Data write enable

Bit(s)	Name	Description
		1100011b: DATA_WRHD. Data write hold Others: Reserved
19:16	NFI_FSM	**This field represents the state of NFI internal FSM (nfi_state[3:0]).** 0000b: Idle 0001b: Reset. Reset command to ready 0010b: Read busy 0011b: Read data 0100b: Program busy 0101b: Program data. Input data command to program command 1000b: Erase busy. Erase command to ready 1001b: Erase data. Erase command 1 to erase command 2 1111b: Custom mode 1110b: Custom mode for data access Others: Reserved
12	READ_EMPTY	**Empty page indication during read operation, including all data, FDM and parity for all sectors**
9	BUSY2READY	**It is read-only. This signal indicates NAND from busy to ready state and it will be reset after nfi_reset or write command/address.**
8	BUSY	**~lat_nrb, which synchronizes busy signal from the NAND flash device. It is read-only. This signal is sampled from device.**
5	FLASH_MACRO_IDLE	**This signal indicates flash macro is idle.** Note: Only flash macro is idle; SW reset or NAND interface change can be issued. 1: Idle 0: Non idle
4	ACCESS_LOCK	**The access range is locked for erase or program.**
3	DATAW	**The NFI core is in data write mode (program state[3:0], which is based on eif_state[6:4]).**
2	DATAR	**The NFI core is in data read mode (program state[3:0], which is based on eif_state[6:4]).**
1	ADDR	**The NFI core is in address mode (program state[3:0], which is based on eif_state[6:4]).**
0	CMD	**The NFI core is in command mode (program state[3:0], which is based on eif_state[6:4]).**

11005064 NFI_FIFOSTA NFI FIFO Status 00004040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WR_FULL	WR_EMPTY	WR_REMAIN						RD_FULL	RD_EMPTY	RD_REMAIN					
Type	RO	RO	RO						RO	RO	RO					
Reset	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
15	WR_FULL	**Data FIFO full in burst write mode**
14	WR_EMPTY	**Data FIFO empty in burst write mode**
13:8	WR_REMAIN	**Data FIFO remaining byte number in burst write mode**
7	RD_FULL	**Data FIFO full in burst read mode**
6	RD_EMPTY	**Data FIFO empty in burst read mode**
5:0	RD_REMAIN	**Data FIFO remaining byte number in burst read mode**

11005070 NFI_ADDRCNTR NFI Page Address Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SEC_CNTR
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CNTR				SEC_ADDR											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:12	SEC_CNTR	**The sector count**
11:0	SEC_ADDR	**The address count of 512 main data and spare data for each sector**

11005080 NFI_STRADDR NFI AHB Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	STR_ADDR	**The start address of EMI for both read or write in DMA mode** If start address of any sector data is not 4-byte aligned, the transfer will be automatically split into byte and word transaction by NFI DMA. Non-4-byte aligned data will be transferred in single-byte transaction. Non-16-byte aligned data will be transferred in single-word transaction. 16-byte aligned data will be transferred by 4 word incrementing burst if the NFI_CNFG->DMA_BURST_EN is enabled.

11005084 NFI_BYTELEN NFI DMA Byte Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																BUS_SEC_CNTR
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUS_SEC_CNTR				BUS_SEC_ADDR											
Type	RO				RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:12	BUS_SEC_CNTR	**The sector count**
11:0	BUS_SEC_ADDR	**The address count of 512 main data and spare data for each sector**

11005090 NFI_CSEL NFI Device Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CSEL**
Type																RW
Reset																0

Bit(s)	Name	Description
0	CSEL	**Chip selection. The default value is 0.** 0: Device 1 is selected. 1: Device 2 is selected.

11005094 NFI_IOCON NFI IO Control register 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**BRSTN**					**L2NW**	**L2NR**	**NLD_PD**
Type									RW					RW	RW	RW
Reset									0	0	0	0		1	1	0

Bit(s)	Name	Description
7:4	BRSTN	**Maximum burst number for NAND read and write. The unit is number of byte (8-bit I/O) or double byte (16-bit I/O)**
2	L2NW	**Enable 1T latency for the arbitration from LCD to NAND write operation. This is used to prevent bus contention between the chip, NAND flash and LCD device.**
1	L2NR	**Enable 1T latency for the arbitration from LCD to NAND read operation. This is used to prevent bus contention between the chip, NAND flash and LCD device.**
0	NLD_PD	**Data bus pull down when this bit is not used** 0: Disable 1: Enable

110050A0 **NFI_FDM0L** **NFI Least FDM Data for Sector 0 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_3								FDM0_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_1								FDM0_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_3	**The 3rd FDM byte data for sector 0**
23:16	FDM0_2	**The 2nd FDM byte data for sector 0**
15:8	FDM0_1	**The 1st FDM byte data for sector 0**
7:0	FDM0_0	**The 0th FDM byte data for sector 0**

110050A4 NFI_FDM0M NFI Most FDM Data for Sector 0 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM0_7								FDM0_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM0_5								FDM0_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM0_7	**The 3rd FDM byte data for sector 0**
23:16	FDM0_6	**The 2nd FDM byte data for sector 0**
15:8	FDM0_5	**The 1st FDM byte data for sector 0**
7:0	FDM0_4	**The 0th FDM byte data for sector 0**

110050A8 **NFI_FDM1L** **NFI Least FDM Data for Sector 1 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM1_3								FDM1_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM1_1								FDM1_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM1_3	**The 3rd FDM byte data for sector 1**
23:16	FDM1_2	**The 2nd FDM byte data for sector 1**
15:8	FDM1_1	**The 1st FDM byte data for sector 1**
7:0	FDM1_0	**The 0th FDM byte data for sector 1**

110050AC **NFI_FDM1M** **NFI Most FDM Data for Sector 1 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM1_7								FDM1_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM1_5								FDM1_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM1_7	**The 7th FDM byte data for sector 1**
23:16	FDM1_6	**The 6th FDM byte data for sector 1**
15:8	FDM1_5	**The 5th FDM byte data for sector 1**
7:0	FDM1_4	**The 4th FDM byte data for sector 1**

110050B0 **NFI_FDM2L** **NFI Least FDM Data for Sector 2 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM2_3								FDM2_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM2_1								FDM2_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM2_3	**The 3rd FDM byte data for sector 2**
23:16	FDM2_2	**The 2nd FDM byte data for sector 2**
15:8	FDM2_1	**The 1st FDM byte data for sector 2**
7:0	FDM2_0	**The 0th FDM byte data for sector 2**

110050B4 NFI_FDM2M NFI Most FDM Data for Sector 2 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM2_7								FDM2_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM2_5								FDM2_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM2_7	**The 7th FDM byte data for sector 2**
23:16	FDM2_6	**The 6th FDM byte data for sector 2**
15:8	FDM2_5	**The 5th FDM byte data for sector 2**
7:0	FDM2_4	**The 4th FDM byte data for sector 2**

110050B8 **NFI_FDM3L** **NFI Least FDM Data for Sector 3 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM3_3								FDM3_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM3_1								FDM3_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM3_3	**The 3rd FDM byte data for sector 3**
23:16	FDM3_2	**The 2nd FDM byte data for sector 3**
15:8	FDM3_1	**The 1st FDM byte data for sector 3**
7:0	FDM3_0	**The 0th FDM byte data for sector 3**

110050BC NFI_FDM3M NFI Most FDM Data for Sector 3 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM3_7								FDM3_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM3_5								FDM3_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM3_7	**The 7th FDM byte data for sector 3**
23:16	FDM3_6	**The 6th FDM byte data for sector 3**
15:8	FDM3_5	**The 5th FDM byte data for sector 3**
7:0	FDM3_4	**The 4th FDM byte data for sector 3**

110050C0 **NFI_FDM4L** **NFI Least FDM Data for Sector 4 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM4_3								FDM4_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM4_1								FDM4_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM4_3	**The 3rd FDM byte data for sector 4**
23:16	FDM4_2	**The 2nd FDM byte data for sector 4**
15:8	FDM4_1	**The 1st FDM byte data for sector 4**
7:0	FDM4_0	**The 0th FDM byte data for sector 4**

110050C4 **NFI_FDM4M** **NFI Most FDM Data for Sector 4 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM4_7								FDM4_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM4_5								FDM4_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM4_7	**The 7th FDM byte data for sector 4**
23:16	FDM4_6	**The 6th FDM byte data for sector 4**
15:8	FDM4_5	**The 5th FDM byte data for sector 4**
7:0	FDM4_4	**The 4th FDM byte data for sector 4**

110050C8 **NFI_FDM5L** **NFI Least FDM Data for Sector 5 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM5_3								FDM5_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM5_1								FDM5_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM5_3	**The 3rd FDM byte data for sector 5**
23:16	FDM5_2	**The 2nd FDM byte data for sector 5**
15:8	FDM5_1	**The 1st FDM byte data for sector 5**
7:0	FDM5_0	**The 0th FDM byte data for sector 5**

110050CC NFI_FDM5M NFI Most FDM Data for Sector 5 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM5_7								FDM5_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM5_5								FDM5_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM5_7	**The 7th FDM byte data for sector 5**
23:16	FDM5_6	**The 6th FDM byte data for sector 5**
15:8	FDM5_5	**The 5th FDM byte data for sector 5**
7:0	FDM5_4	**The 4th FDM byte data for sector 5**

110050D0 NFI_FDM6L NFI Least FDM Data for Sector 6 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM6_3								FDM6_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM6_1								FDM6_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM6_3	**The 3rd FDM byte data for sector 6**
23:16	FDM6_2	**The 2nd FDM byte data for sector 6**
15:8	FDM6_1	**The 1st FDM byte data for sector 6**
7:0	FDM6_0	**The 0th FDM byte data for sector 6**

110050D4 NFI_FDM6M NFI Most FDM Data for Sector 6 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM6_7								FDM6_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM6_5								FDM6_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM6_7	**The 7th FDM byte data for sector 6**
23:16	FDM6_6	**The 6th FDM byte data for sector 6**
15:8	FDM6_5	**The 5th FDM byte data for sector 6**
7:0	FDM6_4	**The 4th FDM byte data for sector 6**

110050D8 NFI_FDM7L NFI Least FDM Data for Sector 7 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM7_3								FDM7_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM7_1								FDM7_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM7_3	**The 3rd FDM byte data for sector 7**
23:16	FDM7_2	**The 2nd FDM byte data for sector 7**
15:8	FDM7_1	**The 1st FDM byte data for sector 7**
7:0	FDM7_0	**The 0th FDM byte data for sector 7**

110050DC NFI_FDM7M NFI Most FDM Data for Sector 7 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM7_7								FDM7_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM7_5								FDM7_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM7_7	**The 7th FDM byte data for sector 7**
23:16	FDM7_6	**The 6th FDM byte data for sector 7**
15:8	FDM7_5	**The 5th FDM byte data for sector 7**
7:0	FDM7_4	**The 4th FDM byte data for sector 7**

110050E0 NFI_FDM8L NFI Least FDM Data for Sector 8 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM8_3								FDM8_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM8_1								FDM8_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM8_3	**The 3rd FDM byte data for sector 8**
23:16	FDM8_2	**The 2nd FDM byte data for sector 8**
15:8	FDM8_1	**The 1st FDM byte data for sector 8**
7:0	FDM8_0	**The 0th FDM byte data for sector 8**

110050E4 NFI_FDM8M NFI Most FDM Data for Sector 8 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM8_7								FDM8_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM8_5								FDM8_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM8_7	**The 7th FDM byte data for sector 8**
23:16	FDM8_6	**The 6th FDM byte data for sector 8**
15:8	FDM8_5	**The 5th FDM byte data for sector 8**
7:0	FDM8_4	**The 4th FDM byte data for sector 8**

110050E8 **NFI_FDM9L** **NFI Least FDM Data for Sector 9 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM9_3								FDM9_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM9_1								FDM9_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM9_3	**The 3rd FDM byte data for sector 9**
23:16	FDM9_2	**The 2nd FDM byte data for sector 9**
15:8	FDM9_1	**The 1st FDM byte data for sector 9**
7:0	FDM9_0	**The 0th FDM byte data for sector 9**

110050EC NFI_FDM9M NFI Most FDM Data for Sector 9 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDM9_7								FDM9_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDM9_5								FDM9_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDM9_7	**The 7th FDM byte data for sector 9**
23:16	FDM9_6	**The 6th FDM byte data for sector 9**
15:8	FDM9_5	**The 5th FDM byte data for sector 9**
7:0	FDM9_4	**The 4th FDM byte data for sector 9**

110050F0 NFI_FDMAL NFI Least FDM Data for Sector A Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMA_3								FDMA_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMA_1								FDMA_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMA_3	**The 3rd FDM byte data for sector A**
23:16	FDMA_2	**The 2nd FDM byte data for sector A**
15:8	FDMA_1	**The 1st FDM byte data for sector A**
7:0	FDMA_0	**The 0th FDM byte data for sector A**

110050F4 **NFI_FDMAM** **NFI Most FDM Data for Sector A Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMA_7								FDMA_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMA_5								FDMA_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMA_7	**The 7th FDM byte data for sector A**
23:16	FDMA_6	**The 6th FDM byte data for sector A**
15:8	FDMA_5	**The 5th FDM byte data for sector A**
7:0	FDMA_4	**The 4th FDM byte data for sector A**

110050F8 **NFI_FDMBL** **NFI Least FDM Data for Sector B Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMB_3								FDMB_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMB_1								FDMB_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMB_3	**The 3rd FDM byte data for sector B**
23:16	FDMB_2	**The 2nd FDM byte data for sector B**
15:8	FDMB_1	**The 1st FDM byte data for sector B**
7:0	FDMB_0	**The 0th FDM byte data for sector B**

110050FC NFI_FDMBM NFI Most FDM Data for Sector B Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMB_7								FDMB_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMB_5								FDMB_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMB_7	**The 7th FDM byte data for sector B**
23:16	FDMB_6	**The 6th FDM byte data for sector B**
15:8	FDMB_5	**The 5th FDM byte data for sector B**
7:0	FDMB_4	**The 4th FDM byte data for sector B**

11005100 NFI_FDMCL NFI Least FDM Data for Sector C Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMC_3								FDMC_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMC_1								FDMC_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMC_3	**The 3rd FDM byte data for sector C**
23:16	FDMC_2	**The 2nd FDM byte data for sector C**
15:8	FDMC_1	**The 1st FDM byte data for sector C**
7:0	FDMC_0	**The 0th FDM byte data for sector C**

11005104 NFI_FDMCM NFI Most FDM Data for Sector C Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMC_7								FDMC_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMC_5								FDMC_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMC_7	**The 7th FDM byte data for sector C**
23:16	FDMC_6	**The 6th FDM byte data for sector C**
15:8	FDMC_5	**The 5th FDM byte data for sector C**
7:0	FDMC_4	**The 4th FDM byte data for sector C**

11005108 NFI_FDMDL NFI Least FDM Data for Sector D Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMD_3								FDMD_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMD_1								FDMD_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMD_3	**The 3rd FDM byte data for sector D**
23:16	FDMD_2	**The 2nd FDM byte data for sector D**
15:8	FDMD_1	**The 1st FDM byte data for sector D**
7:0	FDMD_0	**The 0th FDM byte data for sector D**

1100510C **NFI_FDMDM** **NFI Most FDM Data for Sector D Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMD_7								FDMD_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMD_5								FDMD_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMD_7	**The 7th FDM byte data for sector D**
23:16	FDMD_6	**The 6th FDM byte data for sector D**
15:8	FDMD_5	**The 5th FDM byte data for sector D**
7:0	FDMD_4	**The 4th FDM byte data for sector D**

11005110 NFI_FDMEL NFI Least FDM Data for Sector E Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDME_3								FDME_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDME_1								FDME_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDME_3	**The 3rd FDM byte data for sector E**
23:16	FDME_2	**The 2nd FDM byte data for sector E**
15:8	FDME_1	**The 1st FDM byte data for sector E**
7:0	FDME_0	**The 0th FDM byte data for sector E**

11005114 NFI_FDMEM NFI Most FDM Data for Sector E Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDME_7								FDME_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDME_5								FDME_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDME_7	**The 7th FDM byte data for sector E**
23:16	FDME_6	**The 6th FDM byte data for sector E**
15:8	FDME_5	**The 5th FDM byte data for sector E**
7:0	FDME_4	**The 4th FDM byte data for sector E**

11005118 NFI_FDMFL NFI Least FDM Data for Sector F Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMF_3								FDMF_2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMF_1								FDMF_0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMF_3	**The 3rd FDM byte data for sector F**
23:16	FDMF_2	**The 2nd FDM byte data for sector F**
15:8	FDMF_1	**The 1st FDM byte data for sector F**
7:0	FDMF_0	**The 0th FDM byte data for sector F**

1100511C **NFI_FDMFM** **NFI Most FDM Data for Sector F Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FDMF_7								FDMF_6							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDMF_5								FDMF_4							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	FDMF_7	**The 7th FDM byte data for sector F**
23:16	FDMF_6	**The 6th FDM byte data for sector F**
15:8	FDMF_5	**The 5th FDM byte data for sector F**
7:0	FDMF_4	**The 4th FDM byte data for sector F**

11005120 NFI_CRC01 NFI CRC Data for Sectors 0 and 1 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC1_M								CRC1_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC0_M								CRC0_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC1_M	**The most CRC byte for sector 1**
23:16	CRC1_L	**The least CRC byte for sector 1**
15:8	CRC0_M	**The most CRC byte for sector 0**
7:0	CRC0_L	**The least CRC byte for sector 0**

11005124 NFI_CRC23 NFI CRC Data for Sectors 2 and 3 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC3_M								CRC3_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC2_M								CRC2_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC3_M	**The most CRC byte for sector 1**
23:16	CRC3_L	**The least CRC byte for sector 1**
15:8	CRC2_M	**The most CRC byte for sector 0**
7:0	CRC2_L	**The least CRC byte for sector 0**

11005128 NFI_CRC45 NFI CRC Data for Sectors 4 and 5 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC5_M								CRC5_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC4_M								CRC4_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC5_M	**The most CRC byte for sector 1**
23:16	CRC5_L	**The least CRC byte for sector 1**
15:8	CRC4_M	**The most CRC byte for sector 0**
7:0	CRC4_L	**The least CRC byte for sector 0**

1100512C **NFI_CRC67** **NFI CRC Data for Sectors 6 and 7 Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC7_M								CRC7_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC6_M								CRC6_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC7_M	**The most CRC byte for sector 1**
23:16	CRC7_L	**The least CRC byte for sector 1**
15:8	CRC6_M	**The most CRC byte for sector 0**
7:0	CRC6_L	**The least CRC byte for sector 0**

11005130 NFI_CRC89 NFI CRC Data for Sectors 8 and 9 Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRC9_M								CRC9_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRC8_M								CRC8_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRC9_M	**The most CRC byte for sector 1**
23:16	CRC9_L	**The least CRC byte for sector 1**
15:8	CRC8_M	**The most CRC byte for sector 0**
7:0	CRC8_L	**The least CRC byte for sector 0**

11005134 NFI_CRCAB NFI CRC Data for Sectors A and B Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCB_M								CRCB_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRCA_M								CRCA_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRCB_M	**The most CRC byte for sector 1**
23:16	CRCB_L	**The least CRC byte for sector 1**
15:8	CRCA_M	**The most CRC byte for sector 0**
7:0	CRCA_L	**The least CRC byte for sector 0**

11005138 NFI_CRCCD NFI CRC Data for Sectors C and D Register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCD_M								CRCD_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRCC_M								CRCC_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRCD_M	**The most CRC byte for sector 1**
23:16	CRCD_L	**The least CRC byte for sector 1**
15:8	CRCC_M	**The most CRC byte for sector 0**
7:0	CRCC_L	**The least CRC byte for sector 0**

1100513C **NFI_CRCEF** **NFI CRC Data for Sectors E and F Register** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CRCF_M								CRCF_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CRCE_M								CRCE_L							
Type	RO								RO							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	CRCF_M	**The most CRC byte for sector 1**
23:16	CRCF_L	**The least CRC byte for sector 1**
15:8	CRCE_M	**The most CRC byte for sector 0**
7:0	CRCE_L	**The least CRC byte for sector 0**

11005190 NFI_FIFODATA0 NFI FIFO Content Data 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA0	**NFI Data FIFO Content Data 0**

11005194 NFI_FIFODATA1 NFI FIFO Content Data 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA1	**NFI DATA FIFO Content Data 1**

11005198 NFI_FIFODATA2 NFI FIFO Content Data 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA2	**NFI DATA FIFO Content Data 2**

1100519C NFI_FIFODATA3 NFI FIFO Content Data 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO_DATA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIFO_DATA3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FIFO_DATA3	**NFI DATA FIFO Content Data 3**

11005200 NFI_MCON NFI LCD Monitor Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BMCLR	BMSTR
Type															WO	RW
Reset															0	0

Bit(s)	Name	Description
1	BMCLR	**Clear NFI-LCD bandwidth monitor register counter**
0	BMSTR	**Enable NFI-LCD bandwidth monitor** 0: Disable 1: Enable

11005204 NFI_TOTALCNT NFI LCD Monitor Total Cycle Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_TOTALCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_TOTALCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_TOTALCNT	**The total clock cycle count during enabling NFI-LCD bandwidth monitor**

11005208 NFI_RQCNT NFI LCD Monitor Request Cycle Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_RQCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_RQCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_RQCNT	**The request clock cycle count during enabling NFI-LCD bandwidth monitor**

1100520C NFI_ACCNT NFI LCD Monitor Access Cycle Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NFI_ACCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NFI_ACCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NFI_ACCNT	**The access clock cycle count during enabling NFI-LCD bandwidth monitor**

11005220 NFI_DEBUG_CON1 NFI Debug Register 00000085

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					rg_custom_mode_irq_imp	rg_early_read_sec_num					rg_prog_irq_imp	rg_nre_b_low_dly_en				
Type					RW	RW					RW	RW				
Reset					0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYPASS_MASTER_EN	REG_CE_HOLD	CLK_HOLD					AUTOC_HPROT_EN	HWDCM_SWCON_EN_VAL		STROBE_SEL			WBUF_EN	HWDCM_SWCON_ON	HWDCM_SWCON_EN
Type	RW	RW	RW					RW	RW		RW			RW	RW	RW
Reset	0	0	0					0	1		0	0	0	1	0	1

Bit(s)	Name	Description
27	rg_custom_mode_irq_imp	**Enable custom mode IRQ improvement; default: disable.**
26:22	rg_early_read_sec_num	**This signal indicates that when the controller sends early read IRQ, how many sectors are left in one page.**
21	rg_prog_irq_imp	**Enable program IRQ improvement; default: disable.**
20	rg_nre_b_low_dly_en	**To pull nre_b low after pulling nce_b low in read mode.**
15	BYPASS_MASTER_EN	**To improve performance, bypass master async circuit** Note: Just for SLC NAND, and clock @ 133 MHz or 26 MHz; otherwise, this bit cannot be set to 1. 1'b1: Bypass master async circuit 1'b0: Not bypass master async circuit
14	REG_CE_HOLD	**This bit is used for keeping ce low if there is no data driven out during data programming.** 1'b1: When programming data, ce will keep low. 1'b0: When programming data, ce may release low if no data is driven out.
13	CLK_HOLD	**This bit is used for keeping ONFI clock active.** 1'b1: Non-stop ONFI NAND clock during idle state 1'b0: Stop ONFI clock during idle state
8	AUTOC_HPROT_EN	**This register is used for enabling ECC autoc bufferable, which is an option for DMA operation of NFI mode.** 0: autoc not bufferable 1: autoc bufferable
7	HWDCM_SWCON_EN_VAL	**When HWDCM_SWCON_EN is enabled, this bit is used for selecting swcon enable value.** 0: NFI will be busy.

Bit(s)	Name	Description
		1: NFI will be idle.
5:3	STROBE_SEL	**Strobe select** 3'b000: Sampling at the rising edge of NREB 3'b001: Sampling at 1-cycle delay of the rising edge of NREB 3'b010: Sampling at 2-cycle delay of the rising edge of NREB 3'b011: Sampling at 3-cycle delay of the rising edge of NREB 3'b100: Sampling at 4-cycle delay of the rising edge of NREB 3'b101: Sampling at 5-cycle delay of the rising edge of NREB 3'b110: Sampling at 6-cycle delay of the rising edge of NREB 3'b111: Sampling at 7-cycle delay of the rising edge of NREB
2	WBUF_EN	**Used for enabling AHB hprot[2] for bufferable.** 1: Enable hprot control 0: Disable hprot control
1	HWDCM_SWCON_ON	**ECC clock gating control while NFIECC is idle and NAND is busy** 1'b0: Disable ECC clock gating; ECC clock will not be closed while NFI is working. 1'b1: Enable ECC clock gating; ECC clock will be closed while ECC is idle and NAND is busy.
0	HWDCM_SWCON_EN	**Enable hardware DCM control** 0: HW auto control 1: SW control by HWDCM_SWCON_EN_VAL

11005224 **NFI_MASTER_STA** **NFI Master Status** **00018044**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														grant_state		
Type														RO		
Reset														0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					hburst_cnt										ahb_bus_busy	bus_busy
Type					RO										RO	RO
Reset					0	0	0	0							0	0

Bit(s)	Name	Description
18:16	grant_state	**grant_state means current AHB arb_master states.** 3'b001: NFI access 3'b010: autoc access 3'b100: ecc_r access
11:8	hburst_cnt	**hburst_cnt means current burst cnt for AHB operation**
1	ahb_bus_busy	**ahb_bus_busy means each AHB burst access is busy or not.**
0	bus_busy	**bus_busy means NFI internal related req bus is busy or not.**

11005228 NFI_MASTER_RST NFI Master Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															macro_sw_rst	dma_master_sw_rst
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	macro_sw_rst	**For SW reset pad_macro, whose circuit is close to external device**
0	dma_master_sw_rst	**For SW reset DMA master interface status such as AHB**

1100522C NFI_SECCUS_SIZE Customized Size for the Last Sector 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CUS_LAST_SEC_SIZE													CUS_LAST_SEC_SIZE_EN	SECCUS_SIZE_EN	
Type	RW													RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0		0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CUS_SEC_SIZE												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	CUS_LAST_SEC_SIZE	**The last sector size can be programmed independently when bit 18 is asserted.**
18	CUS_LAST_SEC_SIZE_EN	**Enable customization of the size of the last sector. Note: The spare_size will be ignored if this feature is enabled.**
17	SECCUS_SIZE_EN	**Enable customization of the sector size. Note: The spare_size will be ignored if this feature is enabled.**
12:0	CUS_SEC_SIZE	**The sector size is programmable when bit 17 is asserted.**

11005230 NFI_SPIADDRCNTR NFI AHB Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												NF_TSF_SEC				
Type												RO				
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				NF_TSF_ADDR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20:16	NF_TSF_SEC	**This register represents the start address for DMA to access EMI. These memory from the start address is used to put read data from NAND or write data to NAND in DMA mode.**
12:0	NF_TSF_ADDR	**NF_TSF address**

11005234 NFI_SPIBYTELEN NFI DMA Byte Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUS_TSF_SEC			
Type													RO			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				BUS_TSF_ADDR												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:16	BUS_TSF_SEC	**This register represents the current transfer length for DMA to access EMI.**
12:0	BUS_TSF_ADDR	**BUS_TSF address**

11005238 NFI_RANDOM_CNFG Randomizer Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DECODED_SEED															DECODED_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENCODED_SEED															ENCODED_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	DECODED_SEED	**Randomize decoded seed (for Samsung)**
16	DECODED_EN	**Randomize decoded enable (for Samsung and Toshiba)**
15:1	ENCODED_SEED	**Randomize encoded seed (for Samsung)**
0	ENCODED_EN	**Randomize encoded enable (for Samsung and Toshiba)**

1100523C NFI_ENMPTY_THRESH Empty Threshold Setting 0000000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ZERO_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EMPTY_THRESH							
Type									RW							
Reset									0	0	0	0	1	0	1	0

Bit(s)	Name	Description
31:16	ZERO_CNT	**Zero counter of read data in each read operation (sector/page)**
7:0	EMPTY_THRESH	**Empty threshold**

11005240 NFI_NAND_TYPE_CNFG Toggle/Synchronous/Asynchronous Interface and Timing Mode Setting 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**SLC_TYPE**	**INTERFACE_TYPE**	
Type														RO	RW	
Reset														1	0	0

Bit(s)	Name	Description
2	SLC_TYPE	**When INTERFACE_TYPE = 2'b00 or 2'b11, then slc_type is 1, and this signal is used for selecting DQS output.** 1'b0: MLC 1'b1: SLC
1:0	INTERFACE_TYPE	**Interface type configuration** 2'b00: Async 2'b01: Toggle 2'b10: Sync 2'b11: Reserved

11005244 NFI_ACCCON1 NFI Access Timing Setting1 3F3F3F3F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RDPRE_LATENCY								WRPRE_LATENCY					
Type			RW								RW					
Reset			1	1	1	1	1	1			1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RDPST_LATENCY								WRPST_LATENCY					
Type			RW								RW					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
29:24	RDPRE_LATENCY	**This field represents RDPRE state latency: RDPRE_LATENCY+1, used for toggling NAND.**
21:16	WRPRE_LATENCY	**This field represents WRPRE state latency: WRPRE_LATENCY+1, used for toggling NAND.**
13:8	RDPST_LATENCY	**This field represents RDPST state latency: RDPST_LATENCY+1**
5:0	WRPST_LATENCY	**This field represents WRPST state latency: WRPST_LATENCY+1**

11005248 NFI_DELAY_CTRL DQS and DQ Delay Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		DQS_DLY_SEL														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RD_DQS_DDR_TIMING										DQS_DLY_MUX			DQS_MODE		
Type	RW										RW			RW		
Reset	0	0	0	0							0	0		0	0	0

Bit(s)	Name	Description
30:16	DQS_DLY_SEL	**This field represents delay control of DQS, there are 32 levels of delay control which vary from 0 ns to 7.2 ns.** [20:16]-->dly0_sel[4:0] [25:21]-->dly1_sel[4:0] [30:26]-->dly2_sel[4:0]
15:12	RD_DQS_DDR_TIMING	**This field represents strobe of latch read data since rd_dqs_vld is valid. There are 16 types, from 0T to 15T. T means period of operation clock.**
5:4	DQS_DLY_MUX	**Dly_mux[1:0]; work with DQS_DLY_SEL for control delay of DQS signal** 2'b00: No delay 2'b01: dly0 and dly1 2'b10: dly0 2'b11: dly0 and dly1 and dly2
2:0	DQS_MODE	**This field represents delay control of DQS. There are 8 levels of delay control, which can be from 0T to 3.5T. 1T means period of DQS/4. (Used for FPGA mode only)**

1100524C RANDOM_TSB_SEED0 TOSHIBA seed0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED0	**TOSHIBA randomizer seed0**

11005250 RANDOM_TSB_SEED1 TOSHIBA seed1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED1	**TOSHIBA randomizer seed1**

11005254 RANDOM_TSB_SEED2 TOSHIBA seed2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED2	**TOSHIBA randomizer seed2**

11005258 RANDOM_TSB_SEED3 TOSHIBA seed3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED3	**TOSHIBA randomizer seed3**

1100525C RANDOM_TSB_SEED4 TOSHIBA seed4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED4	**TOSHIBA randomizer seed4**

11005260 RANDOM_TSB_SEED5 TOSHIBA seed5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED5	**TOSHIBA randomizer seed5**

11005264 RANDOM_TSB_SEED6 TOSHIBA seed6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED6	**TOSHIBA randomizer seed6**

11005268 RANDOM_TSB_SEED7 TOSHIBA seed7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED7	**TOSHIBA randomizer seed7**

1100526C RANDOM_TSB_SEED8 TOSHIBA seed8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED8															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED8	**TOSHIBA randomizer seed8**

11005270 RANDOM_TSB_SEED9 TOSHIBA seed9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED9															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED9	**TOSHIBA randomizer seed9**

11005274 RANDOM_TSB_SEED10 TOSHIBA seed10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED10															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED10	**TOSHIBA randomizer seed10**

11005278 RANDOM_TSB_SEED11 TOSHIBA seed11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED11															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED11	**TOSHIBA randomizer seed11**

1100527C RANDOM_TSB_SEED12 TOSHIBA seed12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED12															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED12	**TOSHIBA randomizer seed12**

11005280 RANDOM_TSB_SEED13 TOSHIBA seed13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED13															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED13	**TOSHIBA randomizer seed13**

11005284 RANDOM_TSB_SEED14 TOSHIBA seed14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED14															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED14	**TOSHIBA randomizer seed14**

11005288 RANDOM_TSB_SEED15 TOSHIBA seed15 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_SEED15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SEED15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EN_SEED15	**TOSHIBA randomizer seed15**

11005490 NFI_FLUSH NFI Software Reset Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FLASH_RESET_ACT
Type																RO
Reset																0

Bit(s)	Name	Description
0	FLASH_RESET_ACT	**Controlled by flush_fifo or nfi_reset; reset AHB related status**

11005500 SNF_MAC_CTL Serial NAND Flash MAC Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**MAC_XIO_SEL**	**SF_MAC_EN**	**SF_TRIG**	**WIP_READY**	**WIP**
Type												RW	RW	RW	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	MAC_XIO_SEL	**MAC mode for QPI/SPI setting** 0: SPI 1: QPI
3	SF_MAC_EN	**Switches the serial flash control to update the macro. Please set up this bit before triggering the update macro (It is suggested to run MAC mode in internal sysram code because DIRECT/MAC cannot run at the same time. Another way is to switch to hardware auto switch mode by setting up MAC_MASK_OP)** 0: Disable MAC_MODE 1: Enable MAC MODE (Direct read is forbidden when SF_MAC_EN = 1)
2	SF_TRIG	**Serial flash write macro trigger** 0: Disable 1: Enable (Fill command sequence I/O length before SF_TRIG)
1	WIP_READY	**WIP register status ready for access. WIP_READY exits due to asynchronous latency delay before flash responds to WIP** 0: WIP not ready for read 1: WIP ready for read (Check if WIP_READY = 1 before the next command sequence)
0	WIP	**Serial flash command write in process** 0: Flash update finished (Check if WIP = 0 before the next command sequence) 1: Not finished

11005504 SNF_MAC_OUTL Serial NAND Flash MAC Mode Output Data Length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SNF_MAC_OUT_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SNF_MAC_OUT_LENGTH	**Serial flash write data length (unit: byte)**

11005508 SNF_MAC_INL Serial NAND Flash MAC Mode Input Data Length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SNF_MAC_IN_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SNF_MAC_IN_LENGTH	**Serial flash read data length (unit: byte)**

1100550C **SNF_RD_CTL1** **Serial NAND Flash Read Control 1** **13000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAGE_READ_CMD								PAGE_READ_ADDRESS							
Type	RW								RW							
Reset	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PAGE_READ_ADDRESS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	PAGE_READ_CMD	**Page read command setting**
23:0	PAGE_READ_ADDRESS	**Page read address**

11005510 SNF_RD_CTL2 Serial NAND Flash Read Control 2 0000080B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DATA_READ_DUMMY				DATA_READ_CMD							
Type					RW				RW							
Reset					1	0	0	0	0	0	0	0	1	0	1	1

Bit(s)	Name	Description
11:8	DATA_READ_DUMMY	**Dummy cycle** When reading from cache, set the dummy cycles according to read command of datasheet.
7:0	DATA_READ_CMD	**Data read command**

11005514 SNF_RD_CTL3 Serial NAND Flash Read Control 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA_READ_CMD_DUMMY_OUT				DATA_READ_ADDRESS											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	DATA_READ_CMD_DUMMY_OUT	**Data read command output in dummy cycle [3:0]**
11:0	DATA_READ_ADDRESS	**Data read address setting [11:0]**

11005518 SNF_GF_CTL1 Serial NAND Flash Get Feature Control 1 0FC00101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GF_CMD								GF_ADDR							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GF_BUSY_MASK								GF_STATUS							
Type	RW								RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GF_CMD	**Get feature command setting**
23:16	GF_ADDR	**Get feature address setting**

15:8	GF_BUSY_MASK	**Get feature status busy mask bits setting**
		E.g.
		flag[7:0] = get_feature_status[7:0] & get_feature_busy [7:0];
		If (flag[7:0] == 0) done;
		Else, continue
		0: Mask this bit. Do not check it
		1: Check this bit

7:0	GF_STATUS	**Get feature status result [7:0]**

11005520 SNF_GF_CTL3 Serial NAND Flash Get Feature Control3 000F0320

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													LOOP_LIMIT			
Type													RW			
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POOLING_CYCLE															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
19:16	LOOP_LIMIT	**Get Feature loop setting for status read and compare** Note: 4'b1111 for no limit setting
15:0	POOLING_CYCLE	**Polling cycle setting for standby period between issuing Get Feature commands** Standby period = polling_cycle x base_time_slot Base_time_slot = spi-nand clock cycle x 128. E.g. spi-nand clock = 100M, 1T = 10 ns, then base_time_slot = 1.28 µs. And the polling cycle value should be set to meet the Standby_period ~= spec time.

11005524 SNF_PG_CTL1 Serial NAND Flash Program Control1 00100206

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PG_EXE_CMD							
Type									RW							
Reset									0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_LOAD_CMD								WRITE_EN_CMD							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0

Bit(s)	Name	Description
23:16	PG_EXE_CMD	**Program execute command [7:0]**
15:8	PG_LOAD_CMD	**Program load command [7:0]**
7:0	WRITE_EN_CMD	**Write enable command [7:0]**

11005528 SNF_PG_CTL2 Serial NAND Flash Program Control2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_LOAD_CMD_DUMMY_OUT								PG_LOAD_ADDR							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	PG_LOAD_CMD_DUMMY_OUT	**Program load command output in dummy cycle [3:0]**
7:0	PG_LOAD_ADDR	**Program load address [7:0]**

1100552C SNF_PG_CTL3 Serial NAND Flash Program Control3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									PG_EXE_ADDR							
Type									RW							
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PG_EXE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23:0	PG_EXE_ADDR	**Program execute address [23:0]**

11005530 SNF_ER_CTL Serial NAND Flash Erase Control 0000D800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_CMD															AUTO_ERASE_TRIGGER
Type	RW															RW
Reset	1	1	0	1	1	0	0	0								0

Bit(s)	Name	Description
15:8	ERASE_CMD	**Erase command setting [7:0]**
0	AUTO_ERASE_TRIGGER	**Auto ease trigger bit**

11005534 SNF_ER_CTL2 Serial NAND Flash Erase Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ERASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ERASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ERASE_ADDR	**Erase address setting [23:0]**

11005538 SNF_MISC_CTL Serial NAND Flash MISC Control 0400000A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MACRO_RST_EN	SW_RST	SFIO_EN_SEL	FIFO_RD_LTC		_4FIFO_EN	FBCLK_SEL	SMPCK_INV	CLK_INV	PG_LOAD_X4_EN		DATA_READ_MODE		
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW		RW		
Reset			0	0	0	1	0	0	0	0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SF2CS_DUAL_EN	SF2CS_SEL	SF2CS_EN			LATCH_LAT		PG_LOAD_CUSTOM_EN	DATARD_CUSTOM_EN		CS_DESELECT_CYC				
Type		RW	RW	RW			RW		RW	RW		RW				
Reset		0	0	0			0	0	0	0		0	1	0	1	0

Bit(s)	Name	Description
29	MACRO_RST_EN	**Macro reset FIFO enable**
28	SW_RST	**SW reset controller: 1 for reset on, 0 for reset off.**
27	SFIO_EN_SEL	**IO PAD enable signal alignment with clock positive edge selection**
26:25	FIFO_RD_LTC	**FIFO read latency**
24	_4FIFO_EN	**Enable 4Tap FIFO read**
23	FBCLK_SEL	**Feedback clock selection**
22	SMPCK_INV	**Inner sample clock inverter selection**
21	CLK_INV	**Output serial clock inverter selection**
20	PG_LOAD_X4_EN	**Enable program load data x4 mode**
18:16	DATA_READ_MODE	**Data read mode select. Bit[1:0] for data mode, Bit[2] for IO mode.** 000: X1 data mode 001: X2 data mode 010: X4 data mode 011: Reserved 100: Reserved 101: Dual IO mode 110: Quad IO mode 111: Reserved
14	SF2CS_DUAL_EN	**Both CS1/CS2 enable/select for first/second SPI-NAND device**
13	SF2CS_SEL	**SF 2CS select for first/second SPI NAND device**
12	SF2CS_EN	**SF 2CS enable for second SPI NAND device**
9:8	LATCH_LAT	**Data read latch latency for auto mode**
7	PG_LOAD_CUSTOM_EN	**Enable program load custom mode**

Bit(s)	Name	Description
6	DATARD_CUSTOM_EN	**Enable data read custom mode**
4:0	CS_DESELECT_CYC	**CS deselect cycle setting**

1100553C SNF_MISC_CTL2 Serial NAND Flash MISC Control 2 02100210

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					PROGRAM_LOAD_BYTE_NUM											
Type					RW											
Reset					0	0	1	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					READ_DATA_BYTE_NUM											
Type					RW											
Reset					0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description

27:16	PROGRAM_LOAD_BYTE_NUM	**Note: Setting value should sync with NFI Read/Write byte length.**
		if (NFI_SECCUS_SIZE.CUS_SEC_SIZE.SECCUS_SIZE_EN==0) {
		(512 + PAGEFMT.spare_size) * NFI_CON.sec_num
		== Transfer Data Length
		== SNF_MISC_CTL2.PROGRAM_LOAD_BYTE_NUM
		== SNF_MISC_CTL2.READ_DATA_BYTE_NUM
		} else {
		(NFI_SECCUS_SIZE.CUS_SEC_SIZE) * NFI_CON.sec_num
		== Transfer Data Length
		== SNF_MISC_CTL2.PROGRAM_LOAD_BYTE_NUM
		== SNF_MISC_CTL2.READ_DATA_BYTE_NUM

11:0	READ_DATA_BYTE_NUM	**Note: Setting value should sync with NFI Read byte length.**
		if (NFI_SECCUS_SIZE.CUS_SEC_SIZE.SECCUS_SIZE_EN==0) {
		(512 + PAGEFMT.spare_size) * NFI_CON.sec_num
		== Transfer Data Length
		== SNF_MISC_CTL2.READ_DATA_BYTE_NUM
		} else {
		(NFI_SECCUS_SIZE.CUS_SEC_SIZE) * NFI_CON.sec_num
		== Transfer Data Length
		== SNF_MISC_CTL2.READ_DATA_BYTE_NUM

11005540 SNF_DLY_CTL1 Serial NAND Flash Delay Control Setting 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIO3_OUT_DLY								SFIO2_OUT_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SFIO1_OUT_DLY										SFIO0_OUT_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
29:24	SFIO3_OUT_DLY	**Serial flash SFIO3 pin IO output delay setting**
21:16	SFIO2_OUT_DLY	**Serial flash SFIO2 pin IO output delay setting**
13:8	SFIO1_OUT_DLY	**Serial flash SFIO1 pin IO output delay setting**
3:0	SFIO0_OUT_DLY	**Serial flash SFIO0 pin IO output delay setting**

11005544 SNF_DLY_CTL2 Serial NAND Flash Delay Control Setting 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIO3_IN_DLY								SFIO2_IN_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SFIO1_IN_DLY								SFIO0_IN_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	SFIO3_IN_DLY	**Serial flash SFIO3 pin IO input delay setting**
21:16	SFIO2_IN_DLY	**Serial flash SFIO2 pin IO input delay setting**
13:8	SFIO1_IN_DLY	**Serial flash SFIO1 pin IO input delay setting**
5:0	SFIO0_IN_DLY	**Serial flash SFIO0 pin IO input delay setting**

11005548 SNF_DLY_CTL3 Serial NAND Flash Control Setting 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SFIFO_WR_EN_DLY_SEL										SFCS_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SFCK_OUT_DLY						SFCK_SAM_DLY					
Type					RW						RW					
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	SFIFO_WR_EN_DLY_SEL	**Serial flash FIFO write enable delay select setting**
19:16	SFCS_DLY	**Serial flash SFCS pin IO output delay setting**
11:8	SFCK_OUT_DLY	**Serial flash CK pin IO output delay setting**
5:0	SFCK_SAM_DLY	**Serial flash sample clock delay setting**

1100554C SNF_DLY_CTL4 Serial NAND Flash Delay Control Setting 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SFCS2_DLY			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SFCS2_DLY	**Serial flash SFCS2 pin IO output delay setting**

11005550 SNF_STA_CTL1 Serial NAND Flash Status1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			GF_LOOP_TIMEOUT	CUS_PG_DONE	CUS_READ_DONE	AUTO_PG_DONE	AUTO_READ_DONE	AUTO_BLRER_DONE		DATARD_STATE			PGREAD_STATE			PGEXE_STATE
Type			RO	W1C	W1C	W1C	W1C	W1C		RO			RO			RO
Reset			0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGEXE_STATE		PGLOAD_STATE			GF_STATE			BLKER_STATE			WREN_STATE	SPI_STATE			
Type	RO		RO			RO			RO			RO	RO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	GF_LOOP_TIMEOUT	**Get Feature read status timeout flag**
28	CUS_PG_DONE	**Custom program mode clear setting and status** Status read (R): Custom program mode done flag Clear (W): Set 1 then set 0 to clear this flag
27	CUS_READ_DONE	**Custom read mode clear setting and status** Status read (R): Custom read mode done flag Clear (W): Set 1 then set 0 to clear this flag
26	AUTO_PG_DONE	**Auto program mode clear setting and status** Status read (R): Auto program mode done flag Clear (W): Set 1 then set 0 to clear this flag
25	AUTO_READ_DONE	**Auto read mode clear setting and status** Status read (R): Auto read mode done flag Clear (W): Set 1 then set 0 to clear this flag
24	AUTO_BLRER_DONE	**Auto block erase mode clear setting and status** Status read (R): Auto block erase mode done flag Clear (W): Set 1 then set 0 to clear this flag
22:20	DATARD_STATE	**State machine of custom read** 0: IDLE 1: CMD 2: ADDR1 3: ADDR2 4: DUMMY 5: DATA 6: BUFOUT

Bit(s)	Name	Description
		7: WAIT
19:17	PGREAD_STATE	**State machine of auto read**
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2
		4: ADDR3
16:14	PGEXE_STATE	**State machine of program execution**
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2
		4: ADDR3
13:11	PGLOAD_STATE	**State machine of program load**
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2
		4: BUFIN
		5: DATA
10:8	GF_STATE	**State machine of get feature**
		0: IDLE
		1: GF_CMD
		2: GF_ADDR
		3: GF_DATA
		4: GF_CMP
		5: GF_WAIT
7:5	BLKER_STATE	**State machine of auto block erase**
		0: IDLE
		1: CMD
		2: ADDR1
		3: ADDR2

Bit(s)	Name	Description
		4: ADDR3
4	WREN_STATE	**Enable state machine of write** 0: IDLE 1: CMD
3:0	SPI_STATE	**State machine SPI main controller** 0: IDLE 1: Write Enable 2: Block Erase 3: Get Feature 4: Program Load 5: Program Execution 6: Page Read 7: Custom Data Read

11005554 SNF_STA_CTL2 Serial NAND Flash Status2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DATARD_BYTE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PGLOAD_BTTE_CNT												
Type				RO												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:16	DATARD_BYTE_CNT	**Data read transfer byte count**
12:0	PGLOAD_BTTE_CNT	**Program load transfer byte count**

11005558 SNF_STA_CTL3 Serial NAND Flash Status3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										GF_BASE_CNT						
Type										RO						
Reset										0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GF_WAIT_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
22:16	GF_BASE_CNT	**Get feature base counter**
15:0	GF_WAIT_CNT	**Get feature wait counter** When GF_BASE_CNT==8'hff, GF_WAIT_CNT plus 1; when GF_WAIT_CNT = Polling_Cycle, issue get feature command.

1100555C **SNF_SNF_CNFG** **SPI/Parallel NAND Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SPI_MODE**
Type																RW
Reset																0

Bit(s)	Name	Description
0	SPI_MODE	**Switch for Parallel NAND or Serial NAND** 0: NFI 1: SPI NAND

11005560 SNF_DEBUG_SEL DEBUG MUX Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DEBUG_SEL	**Debug monitor select**

11005800 SPI_GPRAM_ADDR GPRAM Start Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPRAM_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPRAM_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPRAM_SEL	**When using MAC mode, put data into SRAM**

4.3 Inter-Integrated Circuit (I2C)

4.3.1 Register Definition

Module name: imp_iic_wrap Base address: (+0x11000000)

Address	Name	Width	Register Function
11008000	I2C_INTB	16	I2C Interrupt
11008004	LATCH_ADDR	16	Latch Address
11008008	RST_EN	16	Reset Enable
1100800C	ABORT_STATUS	16	Abort Status
11008010	SEC_EN	16	Secure Enable
11008014	GLOBAL_SEC_EN	16	Global Secure Enable
11008018	ASYNC_CTRL	16	ASYNC Control
11008E00	AP_CLOCK_CG_RO	16	AP CLOCK CG Register
11008E04	AP_CLOCK_CG_W1C	16	AP CLOCK CG Clear Register
11008E08	AP_CLOCK_CG_W1S	16	AP CLOCK CG Set Register
11008E10	CCU_CLOCK_CG_RO	16	CCU CLOCK CG Read-only Register
11008E14	CCU_CLOCK_CG_W1C	16	CCU CLOCK CG Write-1-to-Clear Register
11008E18	CCU_CLOCK_CG_W1S	16	CCU CLOCK CG Write-1-to-Set Register
11008E20	SSPM_CLOCK_CG_RO	16	SSPM CLOCK CG Read-only Register
11008E24	SSPM_CLOCK_CG_W1C	16	SSPM CLOCK CG Write-1-to-Clear Register
11008E28	SSPM_CLOCK_CG_W1S	16	SSPM CLOCK CG Write-1-to-Set Register
11008E30	CLOCK_SEL_RO	16	CLOCK Select Read-only Register
11008E34	CLOCK_SEL_W1C	16	CLOCK Select Write-1-to-Clear Register
11008E38	CLOCK_SEL_W1S	16	CLOCK Select Write-1-to-Set Register
11008EF4	CCU_INT_EN	16	CCU Interrupt Enable Register
11008EF8	CCU_INT_INV	16	CCU Interrupt Inverter Enable Register
11008F10	SEMAPHORE_0_RO	16	SEMAPHORE_0 Read-only Register
11008F14	SEMAPHORE_0_W1C	16	SEMAPHORE_0 Write-1-to-Clear Register
11008F18	SEMAPHORE_0_W1S	16	SEMAPHORE_0 Write-1-to-Set Register
11008F20	SEMAPHORE_1_RO	16	SEMAPHORE_1 Read-only Register
11008F24	SEMAPHORE_1_W1C	16	SEMAPHORE_1 Write-1-to-Clear Register
11008F28	SEMAPHORE_1_W1S	16	SEMAPHORE_1 Write-1-to-Set Register
11008F30	SEMAPHORE_2_RO	16	SEMAPHORE_2 Read-only Register
11008F34	SEMAPHORE_2_W1C	16	SEMAPHORE_2 Write-1-to-Clear Register
11008F38	SEMAPHORE_2_W1S	16	SEMAPHORE_2 Write-1-to-Set Register
11008F00	SEC_SLV_0	16	Secure slave_0 Register
11008F04	SEC_SLV_1	16	Secure slave_1 Register
11008F08	SEC_CCC_0	16	Secure CCC_0 Register
11008F0C	SEC_CCC_1	16	Secure CCC_1 Register
11008100	I2C0_SEC_SLV_EN	16	I2C0 Secure Slave Enable
11007000	I2C0_CHN_DATA_PORT	16	Data Port Register
11007094	I2C0_CHN_SLAVE_ADDR	16	Slave Address Register
11007008	I2C0_CHN_INTR_MASK	16	Interrupt Mask Register
1100700C	I2C0_CHN_INTR_STAT	16	Interrupt Status Register
11007010	I2C0_CHN_CONTROL	16	Control Register
11007014	I2C0_CHN_TRANSFER_LEN	16	Transfer Length Register
11007018	I2C0_CHN_TRANSAC_LEN	16	Transaction Length Register (Number of Transfers per Transaction)
1100701C	I2C0_CHN_DELAY_LEN	16	Inter Delay Length Register
11007020	I2C0_CHN_HTIMING	16	SCL High Timing Control Register
11007024	I2C0_CHN_START	16	Start Register
11007028	I2C0_CHN_EXT_CONF	16	Extension Configuration Register
1100702C	I2C0_CHN_LTIMING	16	SCL Low Timing Control Register
11007030	I2C0_CHN_HS	16	High Speed Mode Register

Address	Name	Width	Register Function
11007034	I2C0_CHN_IO_CONFIG	16	IO Config Register
11007038	I2C0_CHN_FIFO_ADDR_CLR	16	FIFO Address Clear Register
1100703C	I2C0_CHN_DATA_TIMING	16	DATA Receive Time Adjust
11007040	I2C0_CHN_MCU_INTR	16	MCU Interrupt
11007044	I2C0_CHN_TRANSFER_LEN_AUX	16	Transfer Length Register (Number of Bytes per Transfer)
11007048	I2C0_CHN_CLOCK_DIV	16	Clock Divider
1100704C	I2C0_CHN_TIMEOUT_DIV	16	Hardware Timeout Target
11007050	I2C0_CHN_SOFTRESET	16	Soft Reset Register
110070D4	I2C0_CHN_DELAY_STEP	16	For Timestamp (I3C_EN==1)
110070D8	I2C0_CHN_DELAY_SAMPLE	16	For Timestamp (I3C_EN==1)
110070E4	I2C0_CHN_DEBUGSTAT	16	Debug Status Register
110070E8	I2C0_CHN_DEBUGCTRL	16	Debug Control Register
110070EC	I2C0_CHN_DMA_FSM_DEBUG	16	Multi-DMA Channel Debug
110070F0	I2C0_CHN_MULTIMAS	16	Multi-master Control Register
110070F4	I2C0_CHN_FIFO_STAT	16	FIFO Status Register
110070F8	I2C0_CHN_FIFO_THRESH	16	FIFO Threshold Register
11007F00	I2C0_CHN_SEC_CONTROL	16	Security Control
11007F80	I2C0_CHN_CHANNEL_LOCK	16	Channel Lock
11007F84	I2C0_CHN_CHANNEL_SEC	16	Channel Security Enable
11007F88	I2C0_CHN_HW_CG_EN	16	HW DCM Enable
11007F8C	I2C0_CHN_MULTI_DMA	16	Multi-DMA Channel Mode
11007F90	I2C0_CHN_DMA_REQ	16	Multi-DMA Channel Request
11007F94	I2C0_CHN_DMA_NREQ	16	Multi-DMA Channel Request Cancel

11008000 **I2C_INTB** **I2C Interrupt** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IIC_INTB
Type																RO
Reset																0

Bit(s)	Name	Description
0	IIC_INTB	**I2C interrupt.** 0: interrupt 1: Normal

11008004 LATCH_ADDR Latch Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					LATCH_ADDR											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	LATCH_ADDR	**Abort APB offset address.**

11008008 **RST_EN** **Reset Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RST_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RST_EN	**SW reset I2C. Need to be toggled by SW.** 0: Normal 1: Reset

1100800C ABORT_STATUS Abort Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**ABORT_STATUS**								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	ABORT_STATUS	**Abort status.** 0: Normal 1: Abort

11008010 **SEC_EN** **Secure Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SEC_EN	**Secure the whole 4KB address.** 0: Normal 1: Secured

11008014 GLOBAL_SEC_EN Global Secure Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GLOCK	LOCK	DLOCK									SEC_CCC_EN				GSEC_EN
Type	RW	RW	RW									RW				RW
Reset	0	0	0									0	0	0	0	0

Bit(s)	Name	Description
15	GLOCK	0: Unlock 1: Lock
14	LOCK	**Locks the secure bit** 0: Unlock channel secure bit write 1: Lock channel secure bit
13	DLOCK	**Locks the domain registers** 0: Unlock channel domain register write 1: Lock channel domain register write
4:1	SEC_CCC_EN	0: Disable 1: Smaller than 2: Larger than 3: Between
0	GSEC_EN	**Controls global security enabling** When this bit is set to 0, the overall channel will be treated as non-security channel. When this bit is set to 1, the security property will depend on each channel's sec_en. 0: Disable 1: Enable

11008018 ASYNC_CTRL ASYNC Control 00000029

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**ASYNC_CTRL**					
Type											RW					
Reset											1	0	1	0	0	1

Bit(s)	Name	Description
5:0	ASYNC_CTRL	**ASYNC control**

11008E00 AP_CLOCK_CG_RO AP CLOCK CG Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AP_CLOCK_I2C0_CG_RO
Type																RW
Reset																0

Bit(s)	Name	Description
0	AP_CLOCK_I2C0_CG_RO	0: Normal 1: No clock

11008E04 AP_CLOCK_CG_W1C AP CLOCK CG Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**AP_CLOCK_CG_W1C**
Type																W1C
Reset																0

Bit(s)	Name	Description
0	AP_CLOCK_CG_W1C	0: Normal 1: No clock

11008E08 AP_CLOCK_CG_W1S AP CLOCK CG Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**AP_CLOCK_CG_W1S**
Type																W1S
Reset																0

Bit(s)	Name	Description
0	AP_CLOCK_CG_W1S	0: Normal 1: No clock

11008E10 CCU_CLOCK_CG_RO CCU CLOCK CG Read-only Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CCU_CLOCK_CG_RO**
Type																RO
Reset																1

Bit(s)	Name	Description
0	CCU_CLOCK_CG_RO	0: Normal 1: No clock

11008E14 CCU_CLOCK_CG_W1C CCU CLOCK CG Write-1-to-Clear Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CCU_CLOCK_CG_W1C
Type																W1C
Reset																1

Bit(s)	Name	Description
0	CCU_CLOCK_CG_W1C	0: Normal 1: No clock

11008E18 CCU_CLOCK_CG_W1S CCU CLOCK CG Write-1-to-Set Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CCU_CLOCK_CG_W1S**
Type																W1S
Reset																1

Bit(s)	Name	Description
0	CCU_CLOCK_CG_W1S	0: Normal 1: No clock

11008E20 SSPM_CLOCK_CG_RO SSPM CLOCK CG Read-only Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SSPM_CLOCK_CG_RO**
Type																RO
Reset																1

Bit(s)	Name	Description
0	SSPM_CLOCK_CG_RO	0: Normal 1: No clock

11008E24 SSPM_CLOCK_CG_W1C SSPM CLOCK CG Write-1-to-Clear Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SSPM_CLOCK_CG_W1C**
Type																W1C
Reset																1

Bit(s)	Name	Description
0	SSPM_CLOCK_CG_W1C	0: Normal 1: No clock

11008E28 SSPM_CLOCK_CG_W1S SSPM CLOCK CG Write-1-to-Set Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SSPM_CLOCK_CG_W1S**
Type																W1S
Reset																1

Bit(s)	Name	Description
0	SSPM_CLOCK_CG_W1S	0: Normal 1: No clock

11008E30 CLOCK_SEL_RO CLOCK Select Read-only Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLOCK_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	CLOCK_SEL	0: Normal 1: No clock

11008E34 CLOCK_SEL_W1C CLOCK Select Write-1-to-Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CLOCK_SEL_W1C**
Type																W1C
Reset																0

Bit(s)	Name	Description
0	CLOCK_SEL_W1C	0: Normal 1: No clock

11008E38 CLOCK_SEL_W1S CLOCK Select Write-1-to-Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CLOCK_SEL_W1S**
Type																W1S
Reset																0

Bit(s)	Name	Description
0	CLOCK_SEL_W1S	0: Normal 1: No clock

11008EF4 CCU_INT_EN CCU Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CCU_INT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	CCU_INT_EN	0: Off 1: On

11008EF8 CCU_INT_INV CCU Interrupt Inverter Enable Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CCU_INV_EN**
Type																RW
Reset																1

Bit(s)	Name	Description
0	CCU_INV_EN	0: Off 1: On

11008F10 SEMAPHORE_0_RO SEMAPHORE_0 Read-only Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEMAPHORE_0_RO**
Type																RO
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_0_RO	0: Normal 1: NO Clock

11008F14 SEMAPHORE_0_W1C SEMAPHORE_0 Write-1-to-Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEMAPHORE_0_W1C
Type																W1C
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_0_W1C	0: Normal 1: No clock

11008F18 SEMAPHORE_0_W1S SEMAPHORE_0 Write-1-to-Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEMAPHORE_0_W1S
Type																W1C
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_0_W1S	0: Normal 1: No clock

11008F20 SEMAPHORE_1_RO SEMAPHORE_1 Read-only Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEMAPHORE_1_RO**
Type																RO
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_1_RO	0: Normal 1: No clock

11008F24 SEMAPHORE_1_W1C SEMAPHORE_1 Write-1-to-Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEMAPHORE_1_W1C**
Type																W1C
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_1_W1C	0: Normal 1: No clock

11008F28 SEMAPHORE_1_W1S SEMAPHORE_1 Write-1-to-Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEMAPHORE_1_W1S**
Type																W1C
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_1_W1S	0: Normal 1: No clock

11008F30 SEMAPHORE_2_RO SEMAPHORE_2 Read-only Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEMAPHORE_2_RO**
Type																RO
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_2_RO	0: Normal 1: No clock

11008F34 SEMAPHORE_2_W1C SEMAPHORE_2 Write-1-to-Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SEMAPHORE_2_W1C**
Type																W1C
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_2_W1C	0: Normal 1: No clock

11008F38 SEMAPHORE_2_W1S SEMAPHORE_2 Write-1-to-Set Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SEMAPHORE_2_W1S
Type																W1C
Reset																0

Bit(s)	Name	Description
0	SEMAPHORE_2_W1S	0: Normal 1: No clock

11008F00 SEC_SLV_0 Secure slave_0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_SLV_ADDR_1							SEC_SLV_ADDR_EN_1	SEC_SLV_ADDR_0							SEC_SLV_ADDR_EN_0
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:9	SEC_SLV_ADDR_1	**Secure slave ADDR_1**
8	SEC_SLV_ADDR_EN_1	0: Disable
		1: Enable
7:1	SEC_SLV_ADDR_0	**Secure slave ADDR_0**
0	SEC_SLV_ADDR_EN_0	0: Disable
		1: Enable

11008F04 **SEC_SLV_1** **Secure slave_1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_SLV_ADDR_3							SEC_SLV_ADDR_EN_3	SEC_SLV_ADDR_2							SEC_SLV_ADDR_EN_2
Type	RW							RW	RW							RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:9	SEC_SLV_ADDR_3	**Secure slave ADDR_3**
8	SEC_SLV_ADDR_EN_3	0: Disable
		1: Enable
7:1	SEC_SLV_ADDR_2	**Secure slave ADDR_2**
0	SEC_SLV_ADDR_EN_2	0: Disable
		1: Enable

11008F08 SEC_CCC_0 Secure CCC_0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CCC_ADDR_3								SEC_CCC_ADDR_2							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SEC_CCC_ADDR_3	**Use for range.**
7:0	SEC_CCC_ADDR_2	**Use for range.**

11008F0C **SEC_CCC_1** **Secure CCC_1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEC_CCC_ADDR_1								SEC_CCC_ADDR_0							
Type	WO								WO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SEC_CCC_ADDR_1	**Use for exact.**
7:0	SEC_CCC_ADDR_0	**Use for exact.**

11008100 I2C0_SEC_SLV_EN I2C0 Secure Slave Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUS_SEC_SLV_EN			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	BUS_SEC_SLV_EN	0: Disable 1: Enable

11007000 I2C0_CHN_DATA_PORT Data Port Register 0000FF00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CONFIG_LEN								DATA_PORT							
Type	RO								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	DMA_CONFIG_LEN	**DMA config length. Setting this for DMA_CONFIG_LEN*4 length.**
7:0	DATA_PORT	**This is the FIFO access port. During master write sequences (slave_addr[0] = 0), this port can be written by APB, and during master read sequences (slave_addr[0] = 1), this port can be read by APB.** (NOTE) Slave_addr must be set correctly before accessing the FIFO. (DEBUG ONLY) If the fifo_APB_debug bit is set, then the FIFO can be read and write by the APB

11007094 I2C0_CHN_SLAVE_ADDR Slave Address Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SLAVE_ADDR**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	**This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol as a bit that indicates the direction of transfer. 1 = master read, 0 = master write.**

11007008 I2C0_CHN_INTR_MASK interrupt Mask Register 000001FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MAS_ERR	MAS_IBI	MAS_DMA_ERR	MAS_TIMEOUT	MAS_RS_MULTIPLE	MAS_ARB_LOST	MAS_HS_NACKER	MAS_ACKERR	MAS_TRANSAC_COMP
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	MAS_ERR	**Setting this value to 0 will mask bus error interrupt signal.**
7	MAS_IBI	**Setting this value to 0 will mask IN-BAND interrupt signal.**
6	MAS_DMA_ERR	**Setting this value to 0 will mask DMA hand-shake error interrupt signal.**
5	MAS_TIMEOUT	**Setting this value to 0 will mask TIMEOUT interrupt signal.**
4	MAS_RS_MULTIPLE	**Setting this value to 0 will mask RS_MULTIPLE interrupt signal.**
3	MAS_ARB_LOST	**Setting this value to 0 will mask ARB_LOST interrupt signal.**
2	MAS_HS_NACKER	**Setting this value to 0 will mask HS_NACKERR interrupt signal.**
1	MAS_ACKERR	**Setting this value to 0 will mask ACK_ERR interrupt signal.**
0	MAS_TRANSAC_COMP	**Setting this value to 0 will mask TRANSAC_COMP interrupt signal.**

1100700C I2C0_CHN_INTR_STAT Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ERR	IBI	DMA_ERR	TIMEOUT	RS_MULTIPLE	ARB_LOST	HS_NACKERR	ACKERR	TRANSAC_COMP
Type								W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	ERR	**This status is asserted if the I2C bus error has occurred.**
7	IBI	**This status is asserted if the I2C bus in-band interrupt has occurred.**
6	DMA_ERR	**This status is asserted if the DMA hand-shake error has occurred.**
5	TIMEOUT	**This status is asserted if the I2C bus timeout occurred.**
4	RS_MULTIPLE	**This status is asserted if the I2C controller user trigger done occurred.**
3	ARB_LOST	**This status is asserted if the I2C controller loses arbitration.**
2	HS_NACKERR	**This status is asserted if hs master code nack error detection is enabled. If enabled, hs master code nack err will cause transaction to end and stop will be issued.**
1	ACKERR	**This status is asserted if ACK error detection is enabled. If enabled, ackerr will cause transaction to end and stop will be issued.**
0	TRANSAC_COMP	**This status is asserted when a transaction has completed successfully.**

11007010 I2C0_CHN_CONTROL Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									irq_sel	TRANSFER_LEN_CHANGE	ACKERR_DET_EN	DIR_CHANGE	CLK_EXT_EN	DMA_EN	RS_STOP	forc_hs
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	irq_sel	**This option controls when nack error or ack error occurs.** 0: Disable 1: Enable
6	TRANSFER_LEN_CHANGE	**This option specifies whether or not to change the transfer length after the first transfer completes. If enabled, the transfers after the first transfer will use the transfer_len_aux parameter.**
5	ACKERR_DET_EN	**This option enables slave ack error detection. When enabled, if slave ack error is detected, the master shall terminate the transaction by issuing a STOP condition and then asserts ackerr interrupt. MCU shall handle this case appropriately and then reset the FIFO address before reissuing transaction. If this option is disabled, the controller will ignore slave ack error and keep on scheduled transaction.** 0: Disable 1: Enable
4	DIR_CHANGE	**This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the transfer_len_aux parameter.** 0: Disable 1: Enable
3	CLK_EXT_EN	**I2C spec allows slaves to hold the SCL line low if it is not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line.**
2	DMA_EN	**By default, this is disabled, and FIFO data shall be manually prepared by MCU. This default setting should be used for transfer sizes of less than 8 data bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data should be prepared in memory.**
1	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether or not REPEATED-START condition is used between transfers. The last ending transfer always ends with a STOP.**

Bit(s)	Name	Description
		In HS mode, this bit must be set to 1. 0: Use STOP 1: Use REPEATED-START
0	forc_hs	**Force using high-speed timing.** 0: Disable 1: Enable

11007014 I2C0_CHN_TRANSFER_LEN Transfer Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN	**This indicates the number of DATA BYTES to be transferred in 1 transfer unit (excluding slave address byte)** (NOTE) The value must be set to greater than 1, otherwise no transfer will take place.

11007018 I2C0_CHN_TRANSAC_LEN Transaction Length Register (Number of Transfers per Transaction) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TRANSAC_LEN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TRANSAC_LEN	**This indicates the number of TRANSFERS to be transferred in 1 transaction** (NOTE) The value must be set to greater than 1; otherwise, no transfer will take place.

1100701C **I2C0_CHN_DELAY_LEN** **Inter Delay Length Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DELAY_LEN**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DELAY_LEN	**This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0.** Time unit: SCL_H_TIME

11007020 I2C0_CHN_HTIMING SCL High Timing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TIMEOUT_EN	HSAMPLE_CNT_DIV			DELAY_TIME_DET		HSTEP_CNT_DIV					
Type					RW	RW			RW		RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	TIMEOUT_EN	**Enable hardware timeout.**
10:8	HSAMPLE_CNT_DIV	**Used for scl high LS/FS only. This adjusts the width of each sample. SCL_H_SAMPLE_RATE = SAMPLE_CLK/ (HSAMPLE_CNT_DIV+1).**
7:6	DELAY_TIME_DET	**Used for round-trip delay detection.** 0: Disable 3: Enable
5:0	HSTEP_CNT_DIV	**This specifies the number of samples scl high pulse width** SCL_H_TIME = (HSTEP_CNT_DIV + 1) /SCL_H_SAMPLE_RATE.

11007024 I2C0_CHN_START Start Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RS_STOP_MULTIPLE_CONFIG	RS_STOP_MULTIPLE_TRIG	RS_STOP_MULTIPLE_TRIG_CLR												KICK_OFF	START
Type	RW	RW	RO												WO	RW
Reset	0	0	0												0	0

Bit(s)	Name	Description
15	RS_STOP_MULTIPLE_CONFIG	**Enable multiple r/w, length and slave address with rs_stop transfer**
14	RS_STOP_MULTIPLE_TRIG	**Trigger next transfer when enabling multiple r/w, length and slave address with rs_stop transfer**
13	RS_STOP_MULTIPLE_TRIG_CLR	**Clear the rs_stop_mul_trig for the next transfer**
1	KICK_OFF	**Arbitration kick-off.**
0	START	**This register starts the transaction on the bus. It is auto deasserted at the end of the transaction.**

11007028 I2C0_CHN_EXT_CONF Extension Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TIME															EXT_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0								0

Bit(s)	Name	Description
15:8	EXT_TIME	**Used for tSU;STA, tHD;STA and tSU;STO.** Configurable extension time of start condition. Time unit: bclk/ (CLOCK_DIV+1)
0	EXT_EN	**Used for tSU;STA, tHD;STA and tSU;STO.** This option decides to perform the extension of start/stop condition. If enabled, perform the extension; otherwise, do not perform. 0: Disable 1: Enable

1100702C I2C0_CHN_LTIMING SCL Low Timing Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_SEL	LHS_SAMPLE_CNT_DIV			LHS_STEP_CNT_DIV			LSAMPLE_CNT_DIV			LSTEP_CNT_DIV					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_SEL	**High-Speed hold time control selection.** 0: Disable 1: Enable
14:12	LHS_SAMPLE_CNT_DIV	**Used for scl low HS only. This adjusts the width of each sample. SCL_L_SAMPLE_RATE = HS_SAMPLE_CLK/ (LHS_SAMPLE_CNT_DIV+1).**
11:9	LHS_STEP_CNT_DIV	**This specifies the number of samples for scl low width and for HS only.** SCL_L_TIME = (LHS_STEP_CNT_DIV + 1) /HS_SCL_L_SAMPLE_RATE.
8:6	LSAMPLE_CNT_DIV	**Used for scl low LS/FS only. This adjusts the width of each sample. SCL_L_SAMPLE_RATE = SAMPLE_CLK/ (LSAMPLE_CNT_DIV+1).**
5:0	LSTEP_CNT_DIV	**This specifies the number of samples for scl low width** SCL_L_TIME = (LSTEP_CNT_DIV + 1) /SCL_L_SAMPLE_RATE.

11007030 I2C0_CHN_HS High Speed Mode Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HS_HOLD_EN	HHS_SAMPLE_CNT_DIV			HS_NO_HOLD	HHS_STEP_CNT_DIV			HS_SPEED	HS_FC_STEP			HS_HOLD_TIME		HS_NACKERR_DET_EN	HS_EN
Type	RW	RW			RW	RW			RW	RW			RW		RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	HS_HOLD_EN	**Used for high speed mode tHD;DAT only.** Can be off by default. 0: Enable 1: Disable
14:12	HHS_SAMPLE_CNT_DIV	**Used for scl low HS only. This adjusts the width of each sample. SCL_H_SAMPLE_RATE = HS_SAMPLE_CLK/ (HHS_SAMPLE_CNT_DIV+1) .**
11	HS_NO_HOLD	**High-Speed zero hold at ACK bit.**
10:8	HHS_STEP_CNT_DIV	**This specifies the number of samples for scl low width and for HS only.** SCL_H_TIME = (HHS_STEP_CNT_DIV + 1) /HHS_SCL_L_SAMPLE_RATE.
7	HS_SPEED	**Use high speed after common command code.** 0: Disable 1: Enable
6:4	HS_FC_STEP	**This register is for pad control in high speed mode.**
3:2	HS_HOLD_TIME	**This register is for when sampling data in high speed mode.**
1	HS_NACKERR_DET_EN	**This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will be terminated with a STOP condition.**
0	HS_EN	**This enables the high speed transaction. (note: rs_stop must be set to 1 as well)**

11007034 I2C0_CHN_IO_CONFIG IO Config Register 00000093

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**IDLE_OE_EN**	**IO_SYNC_EN**	**SDA_IO_CONFIG**	**SCL_IO_CONFIG**
Type													RW	RW	RW	RW
Reset													0	0	1	1

Bit(s)	Name	Description
3	IDLE_OE_EN	0: Do not drive bus in idle state 1: Drive bus in idle state
2	IO_SYNC_EN	**DEBUG ONLY: When set to 1, scl and sda inputs will be first dual synced by bclk_ck. This should not be needed. Only reserved for debugging.**
1	SDA_IO_CONFIG	**0: Normal tristate io mode** 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode
0	SCL_IO_CONFIG	**0: Normal tristate io mode** 1: Open-drain mode 0: Normal tristate io mode 1: Open-drain mode

11007038 I2C0_CHN_FIFO_ADDR_CLR FIFO Address Clear Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**HFIFO_ADDR_CLR**	**FIFO_ADDR_CLR**
Type															WO	WO
Reset															0	0

Bit(s)	Name	Description
1	HFIFO_ADDR_CLR	**When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.**
0	FIFO_ADDR_CLR	**When written with a 1, a 1 pulse fifo_addr_clr is generated to clear the FIFO address to back to 0.**

1100703C I2C0_CHN_DATA_TIMING DATA Receive Time Adjust 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**DATA_READ_ADJ_EN**	**DATA_READ_ADJ**					
Type										RW	RW					
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	DATA_READ_ADJ_EN	**Enable data read timing adjustment.** 0: Disable 1: Enable
5:0	DATA_READ_ADJ	**Adjust data read timing.**

11007040 I2C0_CHN_MCU_INTR MCU Interrupt 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MCU_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	MCU_EN	0: Disable 1: Enable

11007044 **I2C0_CHN_TRANSFER_LEN_AUX** **Transfer Length Register (Number of Bytes per Transfer)** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	**This field is valid only when dir_change or transfer_len_change is set to 1.** Indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte) for the transfers following the direction change. That is, if dir_change = 1, then the first write transfer length will depend on transfer_len, while the second read transfer length depend on transfer_len_aux. Dir change is always after the first transfer. Note: The value must be set to be bigger than 1; otherwise, no transfer will take place.

11007048 I2C0_CHN_CLOCK_DIV Clock Divider 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CLOCK_DIV**				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	CLOCK_DIV	**Clock divider. It will create SAMPLE_CLK, which equals (I2C module clock/(CLOCK_DIV+1)).** Default: All 1 for low-power.

1100704C **I2C0_CHN_TIMEOUT_DIV** **Hardware Timeout Target** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_TIMEOUT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HW_TIMEOUT	**Timeout target. Hardware will timeout when it reaches this number.** Time unit: SCL_L_TIME

11007050 I2C0_CHN_SOFTRESET Soft Reset Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**ERROR_RESET**	**GRANT_RESET**	**FSM_RESET**	**SOFT_RESET**
Type													WO	WO	WO	WO
Reset													0	0	0	0

Bit(s)	Name	Description
3	ERROR_RESET	**Reset error flag.**
2	GRANT_RESET	**Reset authority.**
1	FSM_RESET	**Reset state machine only.**
0	SOFT_RESET	**When written with 1, 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.** This reset will cause bus charge.

110070D4 I2C0_CHN_DELAY_STEP For Timestamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DELAY_STEP															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DELAY_STEP	**Total delay time = DELAY_STEP/SCL_H_STEP_RATE + Sample delay time**

110070D8 I2C0_CHN_DELAY_SAMPLE For Timestamp (I3C_EN==1) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DELAY_SAMPLE					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	DELAY_SAMPLE	**Sample delay time = (DELAY_SAMPLE+1)/SCL_H_SAMPLE_RATE**

110070E4 I2C0_CHN_DEBUGSTAT Debug Status Register 00006800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SDA_IN_SYNC	SCL_IN_SYNC	WR_FULL	RD_EMPTY	BUS_BUSY	MASTER_WRITE	MASTER_READ	MASTER_STATE							
Type		RO	RO	RO	RO	RO	RO	RO	RO							
Reset		1	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	SDA_IN_SYNC	**BUS SDA status.**
13	SCL_IN_SYNC	**BUS SCL status.**
12	WR_FULL	**This indicates that the FIFO is full.**
11	RD_EMPTY	**This indicates that the FIFO is empty.**
10	BUS_BUSY	**DEBUG ONLY: valid when bus_detect_en is 1. bus_busy = 1 indicates a start transaction has been detected and no stop condition has been detected yet.**
9	MASTER_WRITE	**DEBUG ONLY: 1 = current transfer is in the master write dir**
8	MASTER_READ	**DEBUG ONLY: 1 = current transfer is in the master read dir**
7:0	MASTER_STATE	**DEBUG ONLY: reads back the current master_state.** 0: Idle state; 1: I2C master is preparing sending out the start bit, SCL=1, SDA=1; 2: I2C master is sending out the start bit, SCL=1, SDA=0; 3: I2C master/slave is preparing transmitting data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: I2C master/slave is preparing transmitting ack bit, SCL=0, SDA=ack (ack bit can be changed when SCL=0); 6: I2C master/slave is transmitting ack bit, SCL=1, SDA=0 (ack bit is stable when SCL=1); 7: I2C master is preparing sending out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: I2C master is sending out stop bit or repeated-start bit, SCL=1, SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: I2C master is in delay start between two transfers, SCL=1, SDA=1; 10: I2C master is in FIFO wait state; For writing transaction, it means FIFO is empty and I2C master is waiting for DMA controller writing data into FIFO; For reading transaction, it means FIFO is full and I2C master is

Bit(s)	Name	Description
		waiting for DMA controller reading data from FIFO, SCL=0, SDA=do not care; 12: I2C master is preparing sending out data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (data bit of master code can be changed when SCL=0); 13: I2C master is sending out data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (data bit of master code is stable when SCL=1); 14: I2C master/slave is preparing transmitting nack bit, SCL=0, SDA=nack bit (nack bit can be changed when SCL=0); This state is used only in high-speed transaction; 15: I2C master/slave is transmitting nack bit, SCL=1, SDA=1; This state is used only in high-speed transaction.

110070E8 I2C0_CHN_DEBUGCTRL Debug Control Register 0000001C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RELIABILITY**	**DMAACK_ENABLE**		**OLT_MODE**	**FIFO_APB_DEBUG**
Type												RW	RW		RW	RW
Reset												1	1		0	0

Bit(s)	Name	Description
4	RELIABILITY	0: Disable 1: Enable
3	DMAACK_ENABLE	**Snoop DMA ack for early terminate DMA request.** 0: Disable 1: Enable
1	OLT_MODE	**Use for OLT only.** 0: Disable 1: Enable
0	FIFO_APB_DEBUG	**This is used for trace32 debug purposes. When using trace32, and the memory map is shown, turning this bit on will block the normal APB read access. APB read access to the FIFO is then enabled by writing to APB_debug_rd.** 0: Disable 1: Enable

110070EC **I2C0_CHN_DMA_FSM_DEBUG** **Multi-DMA Channel Debug** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	I3C_EN	APB_ID											FSM_STAT			
Type	RO	RO											RO			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	I3C_EN	**0: I2C** 1: I3C
14:8	APB_ID	**If (APB_ID<32)** This design is in perisys Else, This design is in other HW domain.
3:0	FSM_STAT	**FSM status.** 0x7: Wait for IRQ clean 0xc: Wait for kick-off

110070F0 I2C0_CHN_MULTIMAS Multi-master Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**BUS_DETECT_EN**	**CLK_SYNC_EN**	**ARB_EN**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	BUS_DETECT_EN	**When enabled, the bus status is monitored. If bus is currently busy, no new transaction can proceed.** 0: Disable 1: Enable
1	CLK_SYNC_EN	**When enabled clk sync will be performed.** 0: Disable 1: Enable
0	ARB_EN	**When enabled, multi-master arbitration will be performed.** 0: Disable 1: Enable

110070F4 I2C0_CHN_FIFO_STAT FIFO Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RD_ADDR					WR_ADDR					FIFO_OFFSET				
Type		RO					RO					RO				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RD_ADDR	**The current rd address pointer. (only bit [2:0] has physical meaning)**
9:5	WR_ADDR	**The current wr address pointer. (only bit [2:0] has physical meaning)**
4:0	FIFO_OFFSET	**wr_addr[3:0] - rd_addr[3:0]**

110070F8 I2C0_CHN_FIFO_THRESH FIFO Threshold Register 00000F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TX_TRIG_THRESH								RX_TRIG_THRESH			
Type					RW								RW			
Reset					1	1	1	1					0	0	0	0

Bit(s)	Name	Description
11:8	TX_TRIG_THRESH	**When TX FIFO level is below this value, TX DMA request is asserted.**
3:0	RX_TRIG_THRESH	**When RX FIFO level is above this value, RX DMA request is asserted.**

11007F00 I2C0_CHN_SEC_CONTROL Security Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SKIP_SLAVE_ADDR_OFF	DAA_EN_OFF
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	SKIP_SLAVE_ADDR_OFF	**Force skip slave address off.**
0	DAA_EN_OFF	**Force DAA enable off.**

11007F80 I2C0_CHN_CHANNEL_LOCK Channel Lock 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CHANNEL_LOCK**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_LOCK	**Channel has been locked since security issue.** 0: Disable 1: Enable

11007F84 I2C0_CHN_CHANNEL_SEC Channel Security Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CHANNEL_SEC**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CHANNEL_SEC	**Channel which should be protected.** 0: Disable 1: Enable

11007F88 **I2C0_CHN_HW_CG_EN** **HW DCM Enable** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**DCM_ULPOWER**	**DCM_13M_EN**	**DCM_INTF_EN**	**DCM_EN**
Type													RW	RW	RW	RW
Reset													1	1	1	1

Bit(s)	Name	Description
3	DCM_ULPOWER	**When enabled, most register clocks will be set to 4 * scl.** 0: Disable 1: Enable
2	DCM_13M_EN	**When enabled, it's aligned with DCM_EN.** 0: Disable 1: Enable
1	DCM_INTF_EN	**DCM for DMA interface.** 0: Disable 1: Enable
0	DCM_EN	**Enable HW DCM function.** Default is disable. 0: Disable 1: Enable

11007F8C I2C0_CHN_MULTI_DMA Multi-DMA Channel Mode 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	APB_SET				SIDE_SET				IRQ_SET_EN					DMA_CONFIG_MODE	SHADOW_REG_MODE	TRIGGER_ENABLE
Type	RO				RO				RO					RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0					0	0	0

Bit(s)	Name	Description
15:12	APB_SET	**APB setting register**
11:8	SIDE_SET	**SIDE setting register**
7	IRQ_SET_EN	**Interrupt setting enable register**
2	DMA_CONFIG_MODE	**Enable multi-DMA channel mode.** 0: Disable 1: Enable
1	SHADOW_REG_MODE	**Enable shadow register configuration mode.** 0: Disable 1: Enable
0	TRIGGER_ENABLE	**Enable side-band trigger I2C.** 0: Disable 1: Enable

11007F90 I2C0_CHN_DMA_REQ Multi-DMA Channel Request 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_REQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_REQ	**Request for relative DMA channel.**

11007F94 I2C0_CHN_DMA_NREQ Multi-DMA Channel Request Cancel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DMA_NREQ			
Type													RO			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	DMA_NREQ	**Cancel request for relative DMA channel.**

4.4 Universal Asynchronous Receiver/Transmitter (UART)

4.4.1 Register Definition

Module name: uart0 Base address: (+0x11002000)

Module name: uart1 Base address: (+0x11003000)

Module name: uart2 Base address: (+0x11004000)

Address	Name	Width	Register Function
11002000	RBR	8	RX Buffer Register
11002000	THR	8	TX Holding Register
11002004	IER	8	Interrupt Enable Register
11002008	IIR	8	Interrupt Identification Register
11002008	FCR	8	FIFO Control Register
1100200C	LCR	8	Line Control Register
11002010	MCR	8	Modem Control Register
11002014	LSR	8	Line Status Register
11002018	MSR	8	Modem Status Register
1100201C	SCR	8	Scratch Register
11002020	AUTOBAUD_EN	8	Auto Baud Detect Enable Register
11002024	HIGHSPEED	8	High Speed Mode Register
11002028	SAMPLE_COUNT	8	Sample Counter Register
1100202C	SAMPLE_POINT	8	Sample Point Register
11002030	AUTOBAUD_REG	8	Auto Baud Monitor Register
11002034	RATEFIX_AD	8	Clock Rate Fix Register
11002038	AUTOBAUDSAMPLE	8	Auto Baud Sample Register
1100203C	GUARD	8	Guard Time Added Register
11002040	ESCAPE_DAT	8	Escape Character Register
11002044	ESCAPE_EN	8	Escape Enable Register
11002048	SLEEP_EN	8	Sleep Enable Register
1100204C	DMA_EN	8	DMA Enable Register
11002050	RXTRI_AD	8	Rx Trigger Address
11002054	FRACDIV_L	8	Fractional Divider LSB Address
11002058	FRACDIV_M	8	Fractional Divider MSB Address
1100205C	FCR_RD	8	FIFO Control Register
11002088	RTO_CFG	8	Rx Time Out Configuration Register
11002090	DLL	8	Divisor Latch (LS)
11002094	DLM	8	Divisor Latch (MS)
11002098	EFR	8	Enhanced Feature Register
1100209C	FEATURE_SEL	8	UART Feature Select Register
110020A0	XON1	8	XON1 Char Register
110020A4	XON2	8	XON2 Char Register
110020A8	XOFF1	8	XOFF1 Char Register
110020AC	XOFF2	8	XOFF2 Char Register
110020B0	USB_RX_SEL	8	UART USB RX Pin Selection Register
110020B4	SLEEP_REQ	8	UART Sleep Request Register
110020B8	SLEEP_ACK	8	UART Idle Register

11002000 RBR RX Buffer Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RBR							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR	**Read-only** The received data can be read by accessing this register.

11002000 THR TX Holding Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**THR**							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	THR	**Tx holding register** Write-only. The data to be transmitted are written to this register then sent to PC via serial communication.

11002004 IER Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CTSI	RTSI	XOFFI		EDSSI	ELSI	ETBEI	ERBFI
Type									RW	RW	RW		RW	RW	RW	RW
Reset									0	0	0		0	0	0	0

Bit(s)	Name	Description
7	CTSI	**Masks an interrupt that is generated when a rising edge is detected on the CTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt generated when a rising edge is detected on the CTS modem control line. 1: Unmask an interrupt generated when a rising edge is detected on the CTS modem control line.
6	RTSI	**Masks an interrupt that is generated when a rising edge is detected on the RTS modem control line.** Note: This interrupt is only enabled when hardware flow control is enabled. 0: Mask an interrupt generated when a rising edge is detected on the RTS modem control line. 1: Unmask an interrupt generated when a rising edge is detected on the RTS modem control line.
5	XOFFI	**Masks an interrupt that is generated when an XOFF character is received.** Note: This interrupt is only enabled when software flow control is enabled. 0: Mask an interrupt generated when an XOFF character is received. 1: Unmask an interrupt generated when an XOFF character is received.
3	EDSSI	**When this bit is set to 1, an interrupt will be generated if DCTS (MSR[0]) becomes set.** 0: No interrupt is generated if DCTS (MSR[0]) becomes set. 1: An interrupt is generated if DCTS (MSR[0]) becomes set.
2	ELSI	**When this bit is set to 1, an interrupt will be generated if BI, FE, PE or OE (LSR[4:1]) becomes set.** 0: No interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set. 1: An interrupt is generated if BI, FE, PE or OE (LSR[4:1]) becomes set.

Bit(s)	Name	Description
1	ETBEI	**When this bit is set to 1, an interrupt will be generated if the Tx holding register is empty or the contents of Tx FIFO are reduced to their trigger level.** 0: No interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. 1: An interrupt is generated if the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level
0	ERBFI	**When this bit is set to 1, an interrupt will be generated if Rx data are placed in the Rx buffer register or the Rx trigger level is reached.** 0: No interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. 1: An interrupt is generated if RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached.

11002008 IIR Interrupt Identification Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFOE**		**ID**					
Type									RO		RU					
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:6	FIFOE	**FIFO enable status** 00: FIFO is enabled 11: FIFO is disabled
5:0	ID	**IIR[5:0] Priority Level Interrupt Source** 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE or OE set in LSR. (Under IER[2]=1) 001100 2 RX Data Timeout: Timeout on character in RX FIFO. (Under IER[0]=1) 000100 3 RX Data Received: RX Data received or RX Trigger Level reached. (Under IER[0]=1) 000010 4 TX Holding Register Empty: TX Holding Register empty or TX FIFO Trigger Level reached. (Under IER[1]=1) 000000 5 Modem Status change: DDCD, TERI, DDSR or DCTS set in MSR. (Under IER[3]=1) 010000 6 Software Flow Control: XOFF Character received. (Under IER[5]=1) 100000 7 Hardware Flow Control: CTS or RTS Rising Edge. (Under IER[7]=1 or IER[6]=1) Line Status Interrupt: An RX Line Status Interrupt (IIR[5:0] == 000110b) is generated if ELSI (IER[2]) is set and any of BI, FE, PE or OE (LSR[4:1]) becomes set. The interrupt is cleared by reading the Line Status Register. RX Data Timeout Interrupt: When virtual FIFO mode is disabled, RX Data Timeout Interrupt is generated if all of the following apply:

Bit(s)	Name	Description
		1. FIFO contains at least one character. 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits). 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register, or on a CPU read from the RX FIFO. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading RX FIFO. When virtual FIFO mode is enabled, RX Data Timeout Interrupt is generated if all of the following apply: 1. FIFO is empty. 2. The most recent character was received longer than four character periods ago (including all start, parity and stop bits). 3. The most recent CPU read of the FIFO was longer than four character periods ago. The timeout timer is restarted on receipt of a new byte from the RX Shift Register or reading DMA_EN register. The RX Data Timeout Interrupt is enabled by setting EFRBI (IER[0]) to 1, and is cleared by reading DMA_EN register. RX Data Received Interrupt: An RX Received interrupt (IER[5:0] == 000100b) is generated if EFRBI (IER[0]) is set and either RX Data is placed in the RX Buffer Register or the RX Trigger Level is reached. The interrupt is cleared by reading the RX Buffer Register or the RX FIFO (if enabled). TX Holding Register Empty Interrupt: A TX Holding Register Empty Interrupt (IIR[5:0] = 000010b) is generated if ETRBI (IER[1]) is set and either the TX Holding Register is empty or the contents of the TX FIFO have been reduced to its Trigger Level. The interrupt is cleared by writing to the TX Holding Register or TX FIFO if FIFO enabled. Modem Status Change Interrupt: A Modem Status Change Interrupt (IIR[5:0] = 000000b) is generated if EDSSI (IER[3]) is set and either DDCD, TERI, DDSR or DCTS (MSR[3:0]) becomes set. The interrupt is cleared by reading the Modem Status Register. Software Flow Control Interrupt: A Software Flow Control Interrupt (IIR[5:0] = 010000b) is generated if Software Flow Control is enabled and XOFFI (IER[5]) becomes set, indicating that an XOFF character has been received. The interrupt is cleared by reading the Interrupt Identification Register.

Bit(s)	Name	Description
		Hardware Flow Control Interrupt: A Hardware Flow Control Interrupt (IER[5:0] = 100000b) is generated if Hardware Flow Control is enabled and either RTSI (IER[6]) or CTSI (IER[7]) becomes set, indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. The interrupt is cleared by reading the Interrupt Identification Register.

11002008 FCR FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RFTL1_RFTL0**		**TFTL1_TFTL0**			**CLRT**	**CLRR**	**FIFOE**
Type									WO		WO			WO	WO	WO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**Rx FIFO trigger threshold** Rx FIFO contains a total of 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**Tx FIFO trigger threshold** Tx FIFO contains a total of 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	**Control bit to clear Tx FIFO** 0: No effect 1: Clear Tx FIFO
1	CLRR	**Control bit to clear Rx FIFO** 0: No effect 1: Clear Rx FIFO
0	FIFOE	**Enables FIFO** This bit must be set to 1 for any of other bits in the registers to take effect. 0: Disable both Rx and Tx FIFO 1: Enable both Rx and Tx FIFO

1100200C LCR Line Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLAB	SB	SP	EPS	PEN	STB	WLS1_WLS0	
Type									RW	RW	RW	RW	RW	RW	RW	
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	DLAB	**Divisor latch access bit** 0: Rx and Tx registers are read/written at Address 0 and IER register is read/written at Address 4. 1: Divisor Latch LS is read/written at Address 0 and the Divisor Latch MS is read/written at Address 4.
6	SB	**Sets up break** 0: No effect 1: SOUT signal is forced to "0" state.
5	SP	**Stick parity** 0: No effect. 1: The Parity bit is forced to a defined state, depending on the states of EPS and PEN: If EPS = 1 & PEN = 1, the Parity bit will be set and checked = 0. If EPS = 0 & PEN = 1, the Parity bit will be set and checked = 1.
4	EPS	**Selects even parity** 0: When EPS = 0, an odd number of ones is sent and checked. 1: When EPS = 1, an even number of ones is sent and checked.
3	PEN	**Enables parity** 0: The Parity is neither transmitted nor checked. 1: The Parity is transmitted and checked.
2	STB	**Number of STOP bits** 0: One STOP bit is always added. 1: Two STOP bits are added after each character is sent; unless the character length is 5 when 1 STOP bit is added.
1:0	WLS1_WLS0	**Selects word length.** 0: 5 bits 1: 6 bits 2: 7 bits

Bit(s)	Name	Description
		3: 8 bits

11002010 MCR Modem Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**XOFF_STATUS**			**Loop**			**RTS**	
Type									RU			RW			RW	
Reset									0			0			0	

Bit(s)	Name	Description
7	XOFF_STATUS	**Read-only** 0: When an XON character is received. 1: When an XOFF character is received.
4	Loop	**Loopback control bit** 0: No loopback is enabled. 1: Loopback mode is enabled.
1	RTS	**Controls the state of the output NRTS, even in loop mode.** 0: RTS always outputs 1. 1: RTS output is controlled by flow control condition.

11002014 LSR Line Status Register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFOERR	TEMT	THRE	BI	FE	PE	OE	DR
Type									RU	RU	RU	RU	RU	RU	RU	RU
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7	FIFOERR	**Rx FIFO error indicator** 0: No PE, FE and BI is in Rx FIFO. 1: Set to 1 when there is at least one PE, FE or BI in Rx FIFO.
6	TEMT	**Tx holding register (or Tx FIFO) and Tx shift register are empty.** 0: Empty conditions below are not met. 1: If FIFOs are enabled, the bit will be set whenever Tx FIFO and the Tx shift register are empty. If FIFOs are disabled, the bit will be set whenever Tx holding register and Tx shift register are empty.
5	THRE	**Indicates if there is room for Tx holding register or Tx FIFO is reduced to its trigger level.** 0: Reset whenever the contents of Tx FIFO are more than its trigger level (FIFOs are enabled), or whenever Tx holding register is not empty (FIFOs are disabled). 1: Set whenever the contents of Tx FIFO are reduced to its trigger level (FIFOs are enabled), or whenever Tx holding register is empty and ready to accept new data (FIFOs are disabled).
4	BI	**Break interrupt** 0: Reset by CPU reading this register 1: If FIFOs are disabled, this bit will be set whenever SIN is held in 0 state for more than one transmission time (START bit + DATA bits + PARITY + STOP bits). If FIFOs are enabled, this error will be associated with a corresponding character in FIFO and is flagged when this byte is at top of FIFO. When a break occurs, only one zero character will be loaded to the FIFO: The next character transfer will be enabled when SIN enters the marking state and receives the next valid start bit.
3	FE	**Framing error** 0: Reset by CPU reading this register 1: If the FIFOs are disabled, this bit will be set if the received data do not have a valid STOP bit. If FIFOs are enabled, the state of this bit will be revealed when the byte it refers to is the next to be read.
2	PE	**Parity error**

Bit(s)	Name	Description
		0: Reset by CPU reading this register 1: If FIFOs are disabled, this bit will be set if the received data do not have a valid parity bit. If FIFOs are enabled, the state of this bit will be revealed when the referred byte is the next to be read.
1	OE	**Overrun error** 0: Reset by CPU reading this register. 1: If FIFOs are disabled, this bit will be set if Rx buffer is not read by CPU before new data from Rx shift register overwrites the previous contents. If FIFOs are enabled, an overrun error will occur when Rx FIFO is full and Rx shift register becomes full. OE is set as soon as this happens. The character in the shift register will then be overwritten but not transferred to the FIFO.
0	DR	**Data ready** 0: Cleared by CPU reading Rx buffer or by reading all FIFO bytes. 1: Set by Rx buffer becoming full or by FIFO becoming not empty.

11002018 MSR Modem Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CTS**				**DCTS**
Type												RU				RW
Reset												0				0

Bit(s)	Name	Description
4	CTS	**Clear to send** When Loop = "0", this value is the complement of the NCTS input signal. When Loop = "1", this value is equal to the RTS bit in the modem control register.
0	DCTS	**Delta clear to send** 0: Cleared if the state of CTS has not changed since this register is last read. 1: Set if the state of CTS has changed since this register is last read.

1100201C SCR Scratch Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**General purpose read/write register.** After reset, its value will be undefined.

11002020 AUTOBAUD_EN Auto Baud Detect Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															AUTOBAUD_SEL	AUTOBAUD_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	AUTOBAUD_SEL	**Selects auto-baud** 0: Support standard baud rate detection 1: Support non_standard baud rate detection (only baud from 300 to 115,200; using 52 MHz to auto fix is recommended)
0	AUTOBAUD_EN	**Auto-baud enabling signal** 0: Disable auto-baud function 1: Enable auto-baud function (UARTn+0024h SPEED should be set to 0) Note: When AUTOBAUD_EN is active, there should not be A*/a* char before auto baud char AT/at. If A*/a* is inevitable, autobaud will fail and please disable AUTOBAUD_EN to reset autobaud feature and autobaud_en.

11002024 HIGHSPEED High Speed Mode Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**SPEED**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**UART sample counter base** 0: Based on 16*baud_pulse, baud_rate = System clock frequency/16/{DLH, DLL} 1: Based on 8*baud_pulse, baud_rate = System clock frequency/8/{DLH, DLL} 2: Based on 4*baud_pulse, baud_rate = System clock frequency/4/{DLH, DLL} 3: Based on sample_count*baud_pulse, baud_rate = System clock frequency/(sample_count+1)/{DLM, DLL}

11002028 SAMPLE_COUNT Sample Counter Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLECOUNT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SAMPLECOUNT	**Only useful when HIGHSPEED mode = 3**

1100202C SAMPLE_POINT Sample Point Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SAMPLEPOINT							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SAMPLEPOINT	**SAMPLE_POINT is usually (SAMPLE_COUNT-1)/2 without decimal.** Sample point is effective only when HIGHSPEED = 3.

11002030 AUTOBAUD_REG Auto Baud Monitor Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									BAUD_STAT				BAUD_RATE			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	BAUD_STAT	**Autobaud format** 0: Autobaud is detecting. 1: AT_7N1 2: AT_7O1 3: AT_7E1 4: AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1 12: at_8O1 13: Autobaud detection fails.
3:0	BAUD_RATE	**Autobaud baud rate** 0: 115,200 1: 57,600 2: 38,400 3: 19,200 4: 9,600 5: 4,800 6: 2,400 7: 1,200

Bit(s)	Name	Description
		8: 300 9: 110

11002034 RATEFIX_AD Clock Rate Fix Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**FREQ_SEL**	**AUTOBAUD_RATE_FIX**	**RATE_FIX**
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	FREQ_SEL	**0: System clock = UART_CLK_SRC/2** 1: System clock = UART_CLK_SRC/4
1	AUTOBAUD_RATE_FIX	**0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52MHz or 26MHz)** 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depending on FREQ_SEL)
0	RATE_FIX	**0: System clock = UART_CLK_SRC/1 (UART_CLK_SRC = 52 MHz or 26 MHz)** 1: System clock = UART_CLK_SRC/2 or UART_CLK_SRC/4 (depending on FREQ_SEL)

11002038 AUTOBAUDSAMPLE Auto Baud Sample Register 0000000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**AUTOBAUDSAMPLE**					
Type											RW					
Reset											0	0	1	1	0	1

Bit(s)	Name	Description
5:0	AUTOBAUDSAMPLE	**CLK division for autobaud rate detection** For standard baud rate detection. System clk 52m: 'd 27 System clk 26m: 'd 13 System clk 13m: 'd 6 For non-standard baud rate detection: 15

1100203C GUARD Guard Time Added Register 0000000F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**GUARD_EN**	**GUARD_CNT**			
Type												RW	RW			
Reset												0	1	1	1	1

Bit(s)	Name	Description
4	GUARD_EN	**Guard interval add enabling signal** 0: No guard interval added 1: Add guard interval after stop bit
3:0	GUARD_CNT	**Guard interval count value** Guard interval = [1/(system clock/div_step/div)]*GUARD_CNT

11002040 ESCAPE_DAT Escape Character Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**ESCAPE_DAT**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	ESCAPE_DAT	**Escape character added before software flow control data and escape character** If Tx data are xon (31h) with esc_en = 1, UART transmits data as esc + CEh (~xon).

11002044 ESCAPE_EN Escape Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**ESC_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	ESC_EN	**Adds escape character in transmitter and removes escape character in receiver by UART** 0: Does not deal with escape character 1: Add escape character in transmitter and remove escape character in receiver

11002048 SLEEP_EN Sleep Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLEEP_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_EN	**For sleep mode issue** 0: Does not deal with sleep mode indicate signal 1: Activate hardware flow control or software control according to software initial setting when chip enters sleep mode. Release hardware flow when chip wakes up. For software control, UART sends xon when the system is awakened and when FIFO does not reach threshold level.

1100204C DMA_EN DMA Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**FIFO_lsr_sel**	**TO_CNT_AUTORST**	**TX_DMA_EN**	**RX_DMA_EN**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	FIFO_lsr_sel	**Selects FIFO LSR mode** 0: LSR updates automatically with read data from Rx FIFO. 1: LSR holds the first line status error state until you read the LSR register.
2	TO_CNT_AUTORST	**Timeout counter auto reset register** 0: After Rx timeout happens, SW shall reset the interrupt by reading UART 0x4C. 1: The timeout counter will be auto reset. Set this register when Rain's new DMA is used.
1	TX_DMA_EN	**TX_DMA mechanism enabling signal** 0: Does not use DMA in Tx 1: Use DMA in Tx. When this register is enabled, the flow control is based on the DMA threshold and generates a timeout interrupt for DMA.
0	RX_DMA_EN	**RX_DMA mechanism enabling signal** 0: Does not use DMA in Rx 1: Use DMA in Rx. When this register is enabled, the flow control is based on the DMA threshold and generates a timeout interrupt.

11002050 RXTRI_AD Rx Trigger Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RXTRIG**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RXTRIG	**When {rtm,rtl}=2'b11, Rx FIFO threshold will be Rxtrig.** The value is suggested to be less than half of Rx FIFO size, which is 32 bytes.

11002054 FRACDIV_L Fractional Divider LSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FRACDIV_L							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FRACDIV_L	**Adds sampling count (+1) from state data7 to data0 in order to contribute fractional divisor. Only when high_speed==3.**

11002058 FRACDIV_M Fractional Divider MSB Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**FRACDIV_M**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	FRACDIV_M	**Adds sampling count when in state stop to parity in order to contribute fractional divisor. Only when high_speed==3.**

1100205C FCR_RD FIFO Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RFTL1_RFTL0		TFTL1_TFTL0			CLRT	CLRR	FIFOE
Type									RO		RO			RO	RO	RO
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:6	RFTL1_RFTL0	**Rx FIFO trigger threshold** Rx FIFO contains a total of 32 bytes. 0: 1 1: 6 2: 12 3: RXTRIG
5:4	TFTL1_TFTL0	**Tx FIFO trigger threshold** Tx FIFO contains a total of 32 bytes. 0: 1 1: 4 2: 8 3: 14
2	CLRT	0: Tx FIFO is not cleared. 1: Tx FIFO is cleared.
1	CLRR	0: Rx FIFO is not cleared. 1: Rx FIFO is cleared.
0	FIFOE	**Enables FIFO** This bit must be set to 1 for any other bits in the registers to take effect. 0: Rx and Tx FIFOs are not enabled. 1: Rx and Tx FIFOs are enabled.

11002088 RTO_CFG Rx Time Out Configuration Register 00000024

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**RTO_SEL**	**RTO_LENGTH**					
Type										RW	RW					
Reset										0	1	0	0	1	0	0

Bit(s)	Name	Description
6	RTO_SEL	**Select the trigger method of Rx Timeout** 0: Timeout value set to old method 1: Timeout value set to FW programmed value
5:0	RTO_LENGTH	**Timeout value programmed by FW** Unit: bit numbers based on current UART baud rate

11002090 DLL Divisor Latch (LS) 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DLL							
Type									RW							
Reset									0	0	0	0	0	0	0	1

Bit(s)	Name	Description
7:0	DLL	**Divisor latch low 8-bit data**

11002094 DLM Divisor Latch (MS) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DLM**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DLM	**Divisor latch high 8-bit data** Note: Division by 1 generates a BAUD signal that is constantly high. DLL & DLM setting formula is {DLH, DLL}=(system clock frequency/baud_pulse/baud_rate). When RATE_FIX(RATEFIX_AD[0]) = 0, system clock frequency = 52 MHz. When RATE_FIX(RATEFIX_AD[0]) = 1 and RATE_FIX(RATEFIX_AD[2]) = 0, system clock frequency = 26 MHz. When RATE_FIX(RATEFIX_AD[0]) = 1 and RATE_FIX(RATEFIX_AD[2]) = 1, system clock frequency = 13 MHz. For baud_pulse value, refer to HIGH_SPEED(offset=24H) register, e.g. when the source clock is 52 MHz, default speed mode is used and 115200 baud rate need to be configured, {DLH, DLL} = 52 MHz/16/115200 = 28.

11002098 EFR Enhanced Feature Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**AUTO_CTS**	**AUTO_RTS**		**ENABLE_E**	**SW_FLOW_CONT**			
Type									RW	RW		RW	RW			
Reset									0	0		0	0	0	0	0

Bit(s)	Name	Description
7	AUTO_CTS	**Enables hardware transmission flow control** 0: Disable 1: Enable
6	AUTO_RTS	**Enables hardware reception flow control** 0: Disable 1: Enable
4	ENABLE_E	**Enables enhancement feature** 0: Disable 1: Enable
3:0	SW_FLOW_CONT	**Software flow control bits** 00xx: No Tx flow control 10xx: Transmit XON1/XOFF1 as flow control bytes 01xx: Transmit XON2/XOFF2 as flow control bytes xx00: No Rx flow control xx10: Receive XON1/XOFF1 as flow control bytes xx01: Receive XON2/XOFF2 as flow control bytes

1100209C FEATURE_SEL UART Feature Select Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FEATURE_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	FEATURE_SEL	**For AP MCU side UART, if new UART register map is used, feature_sel should be kept at 1.** 0: Disable new register map 1: Enable new register map

110020A0 XON1 XON1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XON1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON1	**XON1 character for software flow control**

110020A4 XON2 XON2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**XON2**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XON2	**XON2 character for software flow control**

110020A8 XOFF1 XOFF1 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF1							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF1	**XOFF1 character for software flow control**

110020AC XOFF2 XOFF2 Char Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									XOFF2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	XOFF2	**XOFF2 character for software flow control**

110020B0 USB_RX_SEL UART USB RX Pin Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																USB_RX_SEL
Type																RW
Reset																0

Bit(s)	Name	Description
0	USB_RX_SEL	0: Select UART Rx pin 1: Select USB Rx pin

110020B4 SLEEP_REQ UART Sleep Request Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLEEP_REQ**
Type																RW
Reset																0

Bit(s)	Name	Description
0	SLEEP_REQ	0: Cancel sleep request to UART (after wake-up sent by CPU) 1: Send sleep request to UART (before sleep sent by CPU)

110020B8 SLEEP_ACK UART Idle Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SLEEP_ACK
Type																RU
Reset																1

Bit(s)	Name	Description
0	SLEEP_ACK	0: UART is not in idle state. (CPU can poll this register to get the UART state.) 1: UART is in idle state. (CPU can poll this register to get the UART state.)

4.5 Pulse Width Modulators (PWMs)

4.5.1 Register Definition

Module name: PWM Base address: (+0x10048000)

Address	Name	Width	Register Function
10048100	PWM2_CON	32	PWM Control Register
10048104	PWM2_HIGH_DURATION	32	PWM High Duration Register
10048108	PWM2_LOW_DURATION	32	PWM Low Duration Register
1004810C	PWM2_DG_DURATION	32	PWM Delay/Guard Duration Register
10048110	PWM2_BUF0_BASE_ADDR	32	PWM Buffer 0 Base Address register
10048114	PWM2_BUF0_SIZE	32	PWM Buffer Size Register
10048118	PWM2_BUF1_BASE_ADDR	32	PWM Buffer 1 Base Address register
1004811C	PWM2_BUF1_SIZE	32	PWM Buffer Size Register
10048120	PWM2_SEND_DATA0	32	PWM Send Data 0 Register
10048124	PWM2_SEND_DATA1	32	PWM Send Data 1 Register
10048128	PWM2_WAVE_NUM	32	PWM Wave Number Register
1004812C	PWM2_DATA_WIDTH	32	PWM Data Width Register
10048130	PWM2_THRESH	32	PWM Threshold Width Register
10048134	PWM2_SEND_WAVENUM	32	PWM Wave Number Register
10048138	PWM2_VALID	32	PWM Wave Number Register
1004813C	PWM2_BUF_BASE_ADDR2	32	PWM Buffer Base Address 2 register
100480C0	PWM1_CON	32	PWM Control Register
100480C4	PWM1_HIGH_DURATION	32	PWM High Duration Register
100480C8	PWM1_LOW_DURATION	32	PWM Low Duration Register
100480CC	PWM1_DG_DURATION	32	PWM Delay/Guard Duration Register
100480D0	PWM1_BUF0_BASE_ADDR	32	PWM Buffer 0 Base Address register
100480D4	PWM1_BUF0_SIZE	32	PWM Buffer Size Register
100480D8	PWM1_BUF1_BASE_ADDR	32	PWM Buffer 1 Base Address register
100480DC	PWM1_BUF1_SIZE	32	PWM Buffer Size Register
100480E0	PWM1_SEND_DATA0	32	PWM Send Data 0 Register
100480E4	PWM1_SEND_DATA1	32	PWM Send Data 1 Register
100480E8	PWM1_WAVE_NUM	32	PWM Wave Number Register
100480EC	PWM1_DATA_WIDTH	32	PWM Data Width Register
100480F0	PWM1_THRESH	32	PWM Threshold Width Register
100480F4	PWM1_SEND_WAVENUM	32	PWM Wave Number Register
100480F8	PWM1_VALID	32	PWM Wave Number Register
100480FC	PWM1_BUF_BASE_ADDR2	32	PWM Buffer Base Address 2 register
10048080	PWM0_CON	32	PWM Control Register
10048084	PWM0_HIGH_DURATION	32	PWM High Duration Register
10048088	PWM0_LOW_DURATION	32	PWM Low Duration Register
1004808C	PWM0_DG_DURATION	32	PWM Delay/Guard Duration Register
10048090	PWM0_BUF0_BASE_ADDR	32	PWM Buffer 0 Base Address register
10048094	PWM0_BUF0_SIZE	32	PWM Buffer Size Register
10048098	PWM0_BUF1_BASE_ADDR	32	PWM Buffer 1 Base Address register
1004809C	PWM0_BUF1_SIZE	32	PWM Buffer Size Register
100480A0	PWM0_SEND_DATA0	32	PWM Send Data 0 Register
100480A4	PWM0_SEND_DATA1	32	PWM Send Data 1 Register
100480A8	PWM0_WAVE_NUM	32	PWM Wave Number Register
100480AC	PWM0_DATA_WIDTH	32	PWM Data Width Register
100480B0	PWM0_THRESH	32	PWM Threshold Width Register
100480B4	PWM0_SEND_WAVENUM	32	PWM Wave Number Register
100480B8	PWM0_VALID	32	PWM Wave Number Register
100480BC	PWM0_BUF_BASE_ADDR2	32	PWM Buffer Base Address 2 register
10048000	PWM_ENABLE	32	PWM Enable Register

Address	Name	Width	Register Function
10048004	PWM_INT_ENABLE_FIN	32	PWM Finish Interrupt Enable Register
10048008	PWM_INT_ENABLE_UDF	32	PWM Underflow Interrupt Enable Register
1004800C	PWM_INT_STATUS_FIN	32	PWM Finish Interrupt Status Register
10048010	PWM_INT_STATUS_UDF	32	PWM Underflow Interrupt Status Register
10048014	PWM_INT_ACK_FIN	32	PWM Finish Interrupt Acknowledge Register
10048018	PWM_INT_ACK_UDF	32	PWM Underflow Interrupt Acknowledge Register
1004801C	PWM_EN_STATUS_UDF	32	PWM Enable Status Register
10048020	PWM_LOOP_BACK_TEST	32	PWM Loopback Test

10048100 PWM2_CON PWM Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_FIN	PWM_INT_STA_UDF	PWM_INT_EN_FIN	PWM_INT_EN_UDF							DELAY_EN	DELAY_CKSRC	PWM2_3DLCM	PWM2_3DLCM_BASE	PWM2_3DLCM_INV	PWM2_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_FIN	**PWM interrupt presents for finish; write 1 to clear.**
30	PWM_INT_STA_UDF	**PWM interrupt presents for underflow; write 1 to clear.**
29	PWM_INT_EN_FIN	**PWM interrupt enable presents for finish.** 1: Enable 0: Disable
28	PWM_INT_EN_UDF	**PWM interrupt enable presents for underflow.** 1: Enable 0: Disable
21	DELAY_EN	**Enable sequential mode**
20	DELAY_CKSRC	**Sequential mode clock source divisor: 1625**
19	PWM2_3DLCM	**This channel inverts or not in 3dlcm mode**
18	PWM2_3DLCM_BASE	**This channel is as 3dlcm base channel**
17	PWM2_3DLCM_INV	**This channel enables 3dlcm mode or not**
16	PWM2_EN_CHN	**PWM2_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.** 1: Enable 0: Disable
15	OLD_PWM_MODE	0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in the total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM2 output value during guard time**
7	IDLE_VALUE	**PWM2 output value in idle state**
6	MODE	0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK = 32K; CLK is not used. 1: CLK = 32K; CLK can be used.
3	CLKSEL	0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

Bit(s)	Name	Description

10048104 PWM2_HIGH_DURATION PWM High Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	**PWM2 pulse duration based on the current clock when PWM2 output is high** If duration = N, program N-1 in this register. Note: The duration of PWM2 must not be 0.

10048108 PWM2_LOW_DURATION PWM Low Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	**PWM2 pulse duration based on the current clock when PWM2 output is low** If duration = N, program N-1 in this register. Note: The duration of PWM2 must not be 0.

1004810C PWM2_DG_DURATION PWM Delay/Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE**

10048110 PWM2_BUF0_BASE_ADDR PWM Buffer 0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM2's waveform data**

10048114 PWM2_BUF0_SIZE PWM Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM2 should generate** If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048118 PWM2_BUF1_BASE_ADDR PWM Buffer 1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM2's waveform data** Note: The memory buffer1 is useless in periodical mode.

1004811C PWM2_BUF1_SIZE PWM Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM2 should generate** If it equals N, program N-1 in this register.

10048120 PWM2_SEND_DATA0 PWM Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM2 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodical FIFO mode. In other modes, this buffer is for internal memory access.

10048124 PWM2_SEND_DATA1 PWM Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM2 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodical FIFO mode. In other modes, this buffer is for internal memory access.

10048128 PWM2_WAVE_NUM PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM0 will generate from pulse data repeatedly** Note: If WAVE_NUM = 0, the waveform generation will not stop until it is disabled.

1004812C PWM2_DATA_WIDTH PWM Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DATA_WIDTH	**PWM2 pulse data width in Standard PWM mode**

10048130 PWM2_THRESH PWM Threshold Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM2 pulse data high/low switching threshold in Standard PWM mode**

10048134 PWM2_SEND_WAVENUM PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	**Memory mode, random mode security usage**
15:0	SEND_WAVENUM	**Number by which PWM2 has already generated from specified data source in periodical mode**

10048138 PWM2_VALID PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31	PSEC_USAGE	PSEC Usage
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

1004813C PWM2_BUF_BASE_ADDR2 PWM Buffer Base Address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	**Base address over 32 bits of memory buffer1 for PWM2's waveform data** Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	**Base address over 32 bits of memory buffer0 for PWM2's waveform data** Note: The memory buffer1 is useless in periodical mode.

100480C0 PWM1_CON PWM Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_FIN	PWM_INT_STA_UDF	PWM_INT_EN_FIN	PWM_INT_EN_UDF							DELAY_EN	DELAY_CKSRC	PWM1_3DLCM	PWM1_3DLCM_BASE	PWM1_3DLCM_INV	PWM1_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_FIN	**PWM interrupt presents for finish; write 1 to clear.**
30	PWM_INT_STA_UDF	**PWM interrupt presents for underflow; write 1 to clear.**
29	PWM_INT_EN_FIN	**PWM interrupt enable presents for finish.** 1: Enable 0: Disable
28	PWM_INT_EN_UDF	**PWM interrupt enable presents for underflow.** 1: Enable 0: Disable
21	DELAY_EN	**Sequential mode enable**
20	DELAY_CKSRC	**Sequential mode clock source divisor: 1625**
19	PWM1_3DLCM	**This channel inverts or not in 3dlcm mode**
18	PWM1_3DLCM_BASE	**This channel is as 3dlcm base channel**
17	PWM1_3DLCM_INV	**This channel enables 3dlcm mode or not**
16	PWM1_EN_CHN	**PWM1_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.**
15	OLD_PWM_MODE	0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in the total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM1 output value during guard time**
7	IDLE_VALUE	**PWM1 output value in idle state**
6	MODE	0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK = 32K; CLK is not used. 1: CLK = 32K; CLK can be used.
3	CLKSEL	0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	000b: CLK Hz 001b: CLK/2 Hz 010b: CLK/4 Hz 011b: CLK/8 Hz 100b: CLK/16 Hz 101b: CLK/32 Hz 110b: CLK/64 Hz 111b: CLK/128 Hz

100480C4 PWM1_HIGH_DURATION PWM High Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	**PWM1 pulse duration based on the current clock when PWM1 output is high** If duration = N, program N-1 in this register. Note: The duration of PWM1 must not be 0.

100480C8 PWM1_LOW_DURATION PWM Low Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	**PWM1 pulse duration based on the current clock when PWM1 output is low** If duration = N, program N-1 in this register. Note: The duration of PWM1 must not be 0.

100480CC PWM1_DG_DURATION PWM Delay/Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE**

100480D0 PWM1_BUF0_BASE_ADDR PWM Buffer 0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM1's waveform data**

100480D4 PWM1_BUF0_SIZE PWM Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM1 should generate** If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

100480D8 PWM1_BUF1_BASE_ADDR PWM Buffer 1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM1's waveform data** Note: The memory buffer1 is useless in periodical mode.

100480DC PWM1_BUF1_SIZE PWM Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM1 should generate** If it equals N, program N-1 in this register.

100480E0 PWM1_SEND_DATA0 PWM Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM1 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodical FIFO mode. In other modes, this buffer is for internal memory access.

100480E4 **PWM1_SEND_DATA1** **PWM Send Data 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM1 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodical FIFO mode. In other modes, this buffer is for internal memory access.

100480E8 PWM1_WAVE_NUM PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM0 will generate from pulse data repeatedly** Note: If WAVE_NUM = 0, the waveform generation will not stop until it is disabled.

100480EC PWM1_DATA_WIDTH PWM Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM1 pulse data width in Standard PWM mode**

100480F0 PWM1_THRESH PWM Threshold Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM1 pulse data high/low switching threshold in Standard PWM mode**

100480F4 PWM1_SEND_WAVENUM PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	**Memory mode, random mode security usage**
15:0	SEND_WAVENUM	**Number by which PWM1 has already generated from specified data source in periodical mode**

100480F8 PWM1_VALID PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31	PSEC_USAGE	PWM security usage
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

100480FC PWM1_BUF_BASE_ADDR2 PWM Buffer Base Address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	**Base address over 32 bits of memory buffer1 for PWM1's waveform data** Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	**Base address over 32 bits of memory buffer0 for PWM1's waveform data** Note: The memory buffer1 is useless in periodical mode.

10048080 PWM0_CON PWM Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PWM_INT_STA_FIN	PWM_INT_STA_UDF	PWM_INT_EN_FIN	PWM_INT_EN_UDF							DELAY_EN	DELAY_CKSRC	PWM0_3DLCM	PWM0_3DLCM_BASE	PWM0_3DLCM_INV	PWM0_EN_CHN
Type	RO	RO	RW	RW							RW	RW	RW	RW	RW	RW
Reset	0	0	0	0							0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OLD_PWM_MODE	STOP_BITPOS						GUARD_VALUE	IDLE_VALUE	MODE	SRCSEL	CLKSEL_OLD	CLKSEL	CLKDIV		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PWM_INT_STA_FIN	**PWM interrupt presents for finish; write 1 to clear.**
30	PWM_INT_STA_UDF	**PWM interrupt presents for underflow; write 1 to clear.**
29	PWM_INT_EN_FIN	**PWM interrupt enable presents for finish.** 1: Enable 0: Disable
28	PWM_INT_EN_UDF	**PWM interrupt enable presents for underflow.** 1: Enable 0: Disable
21	DELAY_EN	**Enable sequential mode** 1: Enable 0: Disable
20	DELAY_CKSRC	**Sequential mode clock source divisor: 1625** 0: CLK = CLKSRC 1: CLK = CLKSRC/1625
19	PWM0_3DLCM	**This channel inverts or not in 3dlcm mode**
18	PWM0_3DLCM_BASE	**This channel is as 3dlcm base channel**
17	PWM0_3DLCM_INV	**This channel enables 3dlcm mode or not**
16	PWM0_EN_CHN	**PWM0_EN at channel side. This bit will work if and only if CHANNEL_LOCK of this channel is enabled.**
15	OLD_PWM_MODE	0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	**Stop bit position for source data in periodical mode** In FIFO mode, it is used to indicate the stop bit position in total 64 bits. In memory mode, it is for the stop bit position of the last 32 bits.
8	GUARD_VALUE	**PWM0 output value during guard time**
7	IDLE_VALUE	**PWM0 output value in idle state**
6	MODE	0: Periodical PWM mode. 1: Random PWM mode
5	SRCSEL	0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK = 32K; CLK is not used. 1: CLK = 32K; CLK can be used.
3	CLKSEL	0: CLK = CLKSRC 1: CLK = CLKSRC/1625
2:0	CLKDIV	000b: CLK Hz 001b: CLK/2 Hz

Bit(s)	Name	Description
		010b: CLK/4 Hz
		011b: CLK/8 Hz
		100b: CLK/16 Hz
		101b: CLK/32 Hz
		110b: CLK/64 Hz
		111b: CLK/128 Hz

10048084 PWM0_HIGH_DURATION PWM High Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	HDURATION	**PWM0 pulse duration based on the current clock when PWM0 output is high** If duration = N, program N-1 in this register. Note: The duration of PWM0 must not be 0.

10048088 PWM0_LOW_DURATION PWM Low Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	LDURATION	**PWM0 pulse duration based on the current clock when PWM0 output is low** If duration = N, program N-1 in this register. Note: The duration of PWM2 must not be 0.

1004808C PWM0_DG_DURATION PWM Delay/Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DELAY_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DELAY_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE** If it equals N, program N-1 in this register. Note: 1. If this duration is 0, it means there is no guarding interval. 2: The guard duration of standard mode is set by PWM_DATA_WIDTH.
15:0	GUARD_DURATION	**Guarding interval between individual waveforms and the output is decided by GUARD_VALUE**

10048090 PWM0_BUF0_BASE_ADDR PWM Buffer 0 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	**Base address of memory buffer0 for PWM0's waveform data**

10048094 PWM0_BUF0_SIZE PWM Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	**Length of waveform data in memory buffer0 PWM0 should generate** If it equals N, program N-1 in this register. Note: The size is in unit of 32-bit data.

10048098 PWM0_BUF1_BASE_ADDR PWM Buffer 1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	**Base address of memory buffer1 for PWM0's waveform data** Note: The memory buffer1 is useless in periodical mode.

1004809C PWM0_BUF1_SIZE PWM Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	**Length of waveform data in memory buffer1 PWM0 should generate** If it equals N, program N-1 in this register.

100480A0 PWM0_SEND_DATA0 PWM Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	**PWM0 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodical FIFO mode. In other modes, this buffer is for internal memory access.

100480A4 PWM0_SEND_DATA1 PWM Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	**PWM0 local buffer0 of pulse sequence data to be generated** Note: This value should be written only in periodical FIFO mode. In other modes, this buffer is for internal memory access.

100480A8 PWM0_WAVE_NUM PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	**Number by which PWM0 will generate from pulse data repeatedly** Note: If WAVE_NUM = 0, the waveform generation will not stop until it is disabled.

100480AC PWM0_DATA_WIDTH PWM Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	**PWM0 pulse data width in Standard PWM mode**

100480B0 PWM0_THRESH PWM Threshold Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	**PWM0 pulse data high/low switching threshold in Standard PWM mode**

100480B4 PWM0_SEND_WAVENUM PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HSEC_USAGE	**Memory mode, random mode security usage**
15:0	SEND_WAVENUM	**Number by which PWM0 has already generated from specified data source in periodical mode**

100480B8 PWM0_VALID PWM Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSEC_USAGE															
Type	WO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31	PSEC_USAGE	PWM security usage
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

100480BC PWM0_BUF_BASE_ADDR2 PWM Buffer Base Address 2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													BUF1_BS_ADDR2			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													BUF0_BS_ADDR2			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
19:16	BUF1_BS_ADDR2	**Base address over 32 bits of memory buffer1 for PWM0's waveform data** Note: The memory buffer1 is useless in periodical mode.
3:0	BUF0_BS_ADDR2	**Base address over 32 bits of memory buffer0 for PWM0's waveform data** Note: The memory buffer1 is useless in periodical mode.

10048000 PWM_ENABLE PWM Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_EN		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_EN	**PWM enable at global side if CHANNEL_LOCK of that channel is disabled** PWM_EN[0] points to PWM0 enable PWM_EN[1] points to PWM1 enable PWM_EN[2] points to PWM2 enable

10048004 PWM_INT_ENABLE_FIN PWM Finish Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_INT_EN_FIN		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_INT_EN_FIN	**PWM interrupt enable presents for finish.** 1: Enable 0: Disable

10048008 PWM_INT_ENABLE_UDF PWM Underflow Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_INT_EN_UDF		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_INT_EN_UDF	**PWM interrupt enable presents for underflow.** 1: Enable 0: Disable

1004800C PWM_INT_STATUS_FIN PWM Finish Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_INT_STA_FIN		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_INT_STA_FIN	**PWM interrupt presents for finish.**

10048010 PWM_INT_STATUS_UDF PWM Underflow Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_INT_STA_UDF		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_INT_STA_UDF	**PWM interrupt presents for underflow.**

10048014 PWM_INT_ACK_FIN PWM Finish Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_INT_ACK_FIN		
Type														WO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_INT_ACK_FIN	**PWM interrupt clear for finish.**

10048018 PWM_INT_ACK_UDF PWM Underflow Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_INT_ACK_UDF		
Type														WO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_INT_ACK_UDF	**PWM interrupt clear for underflow.**

1004801C PWM_EN_STATUS_UDF PWM Enable Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_EN_STA		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_EN_STA	**PWM enable status**

10048020 PWM_LOOP_BACK_TEST PWM Loopback Test 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM_OUT		
Type														RO		
Reset														0	0	0

Bit(s)	Name	Description
2:0	PWM_OUT	**PWM_OUT monitor by APB**

4.6 GPIO (General-Purpose Input/Output)

4.6.1 Register Definition

Module name: GPIO Base address: (+0x11D0_0000)

Address	Name	Width	Register Function
11D00000	GPIO_DIR0	32	GPIO_DIRECTION Register for GPIO0~GPIO31
11D00010	GPIO_DIR1	32	GPIO_DIRECTION Register for GPIO32~GPIO56
11D00004	GPIO_DIR0_SET	32	GPIO_DIRECTION Register for GPIO0~GPIO31
11D00014	GPIO_DIR1_SET	32	GPIO_DIRECTION Register for GPIO32~GPIO56
11D00008	GPIO_DIR0_CLR	32	GPIO_DIRECTION Register for GPIO0~GPIO31
11D00018	GPIO_DIR1_CLR	32	GPIO_DIRECTION Register for GPIO32~GPIO56
11D00100	GPIO_DOUT0	32	GPIO_DOUT Register for GPIO0~GPIO31
11D00110	GPIO_DOUT1	32	GPIO_DOUT Register for GPIO32~GPIO56
11D00104	GPIO_DOUT0_SET	32	GPIO_DOUT Register for GPIO0~GPIO31
11D00114	GPIO_DOUT1_SET	32	GPIO_DOUT Register for GPIO32~GPIO56
11D00108	GPIO_DOUT0_CLR	32	GPIO_DOUT Register for GPIO0~GPIO31
11D00118	GPIO_DOUT1_CLR	32	GPIO_DOUT Register for GPIO32~GPIO56
11D00200	GPIO_DIN0	32	GPIO_DIN Register for GPIO0~GPIO31
11D00210	GPIO_DIN1	32	GPIO_DIN Register for GPIO32~GPIO56
11D00300	GPIO_MODE0	32	Aux Mode of GPIO_MODE0
11D00310	GPIO_MODE1	32	Aux Mode of GPIO_MODE1
11D00320	GPIO_MODE2	32	Aux Mode of GPIO_MODE2
11D00330	GPIO_MODE3	32	Aux Mode of GPIO_MODE3
11D00340	GPIO_MODE4	32	Aux Mode of GPIO_MODE4
11D00350	GPIO_MODE5	32	Aux Mode of GPIO_MODE5
11D00360	GPIO_MODE6	32	Aux Mode of GPIO_MODE6
11D00370	GPIO_MODE7	32	Aux Mode of GPIO_MODE7
11D00304	GPIO_MODE0_SET	32	Bitwise Set of Aux mode of GPIO_MODE0
11D00314	GPIO_MODE1_SET	32	Bitwise Set of Aux mode of GPIO_MODE1
11D00324	GPIO_MODE2_SET	32	Bitwise Set of Aux mode of GPIO_MODE2
11D00334	GPIO_MODE3_SET	32	Bitwise Set of Aux mode of GPIO_MODE3
11D00344	GPIO_MODE4_SET	32	Bitwise Set of Aux Mode of GPIO_MODE4
11D00354	GPIO_MODE5_SET	32	Bitwise Set of Aux Mode of GPIO_MODE5
11D00364	GPIO_MODE6_SET	32	Bitwise Set of Aux Mode of GPIO_MODE6
11D00374	GPIO_MODE7_SET	32	Bitwise Set of Aux Mode of GPIO_MODE7
11D00308	GPIO_MODE0_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE0
11D00318	GPIO_MODE1_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE1
11D00328	GPIO_MODE2_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE2
11D00338	GPIO_MODE3_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE3
11D00348	GPIO_MODE4_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE4
11D00358	GPIO_MODE5_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE5
11D00368	GPIO_MODE6_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE6
11D00378	GPIO_MODE7_CLR	32	Bitwise Clear of Aux Mode of GPIO_MODE7
11D0030C	GPIO_MODE0_MOD	32	Alternative way to set Aux Mode of GPIO_MODE0
11D0031C	GPIO_MODE1_MOD	32	Alternative way to set Aux Mode of GPIO_MODE1
11D0032C	GPIO_MODE2_MOD	32	Alternative way to set Aux Mode of GPIO_MODE2
11D0033C	GPIO_MODE3_MOD	32	Alternative way to set Aux Mode of GPIO_MODE3
11D0034C	GPIO_MODE4_MOD	32	Alternative way to set Aux Mode of GPIO_MODE4
11D0035C	GPIO_MODE5_MOD	32	Alternative way to set Aux Mode of GPIO_MODE5
11D0036C	GPIO_MODE6_MOD	32	Alternative way to set Aux Mode of GPIO_MODE6
11D0037C	GPIO_MODE7_MOD	32	Alternative way to set Aux Mode of GPIO_MODE7
11D00600	MISC	32	Chip Related Misc Options
11D00604	MISC_SET	32	Chip Related Misc Options
11D00608	MISC_CLR	32	Chip Related Misc Options

Address	Name	Width	Register Function
11D006D0	DBG	32	dbg_mon Control Bit
11D006E0	BANK	32	GPIO Reserved Control Register [0]: test_normal_sel_bypreg
11D006F0	TPBANK0	32	Trapping Force Enable
11D00710	AP_GOOD	32	Chip related AP_GPPD Control
11D00714	AP_GOOD_SET	32	Chip related AP_GPPD Control
11D00718	AP_GOOD_CLR	32	Chip related AP_GPPD Control
11D00720	MODE_CFG_CT_REG	32	GPIO Reserved Control Register [0]: test_normal_sel_bypreg
11D00724	MODE_CFG_CT_REG_SET	32	GPIO Reserved Control Register [0]: test_normal_sel_bypreg
11D00728	MODE_CFG_CT_REG_CLR	32	GPIO Reserved Control Register [0]: test_normal_sel_bypreg

11D00000 GPIO_DIR0 GPIO_DIRECTION Register for GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SRW	**GPIO_DIRECTION register for GPIO0~GPIO31** 0: GPIO direction as input; 1: GPIO direction as output;

11D00010 GPIO_DIR1 GPIO_DIRECTION Register for GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SRW	**GPIO_DIRECTION register for GPIO32~GPIO56; GPIO57~GPIO63: reserved** 0: GPIO direction as input; 1: GPIO direction as output;

11D00004 GPIO_DIR0_SET GPIO_DIRECTION Register for GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	**GPIO_DIRECTION register for GPIO0~GPIO31** 0: Keep; 1: SET bit;

11D00014 GPIO_DIR1_SET GPIO_DIRECTION Register for GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	**GPIO_DIRECTION register for GPIO32~GPIO56; GPIO57~GPIO63: reserved** 0: Keep; 1: SET bit;

11D00008 GPIO_DIR0_CLR GPIO_DIRECTION Register for GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	**GPIO_DIRECTION register for GPIO0~GPIO31** 0: Keep; 1: CLR bit

11D00018 GPIO_DIR1_CLR GPIO_DIRECTION Register for GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	**GPIO_DIRECTION register for GPIO32~GPIO56; GPIO57~GPIO63: reserved** 0: Keep; 1: CLR bit

11D00100 GPIO_DOUT0 GPIO_DOUT register GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SRW	**GPIO_DOUT register GPIO0~GPIO31** 0: GPIO output low; 1: GPIO output high;

11D00110 GPIO_DOUT1 GPIO_DOUT register GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SRW	**GPIO_DOUT register GPIO32~GPIO56; GPIO57~GPIO63: reserved** 0: GPIO output low; 1: GPIO output high;

11D00104 GPIO_DOUT0_SET GPIO_DOUT register GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	**GPIO_DOUT register GPIO0~GPIO31** 0: Keep; 1: SET bit;

11D00114 GPIO_DOUT1_SET GPIO_DOUT register GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	**GPIO_DOUT register GPIO32~GPIO56; GPIO57~GPIO63: reserved** 0: Keep; 1: SET bit;

11D00108 GPIO_DOUT0_CLR GPIO_DOUT register GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG0															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG0	SW	**GPIO_DOUT register GPIO0~GPIO31** 0: Keep; 1: CLR bit

11D00118 GPIO_DOUT1_CLR GPIO_DOUT register GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CFG1															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	CFG1	SW	**GPIO_DOUT register GPIO32~GPIO56; GPIO57~GPIO63: reserved** 0: Keep; 1: CLR bit

11D00200 GPIO_DIN0 GPIO_DIN for GPIO0~GPIO31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DATA0	SRW	**GPIO_DIN for GPIO0~GPIO31** [31:0] value of GPIO Input

11D00210 GPIO_DIN1 GPIO_DIN for GPIO32~GPIO56 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DATA1	SRW	**GPIO_DIN for GPIO32~GPIO56; GPIO57~GPIO63: reserved** [31:0] value of GPIO Input

11D00300 GPIO_MODE0 Aux Mode of GPIO_MODE0 11111100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO7				GPIO6				GPIO5				GPIO4		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO3				GPIO2				GPIO1				GPIO0		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO7	SRW	**Aux Mode of PAD_JTAG_JTCLK** 000: B:GPIO7; 001: I1:JTAG_JTCLK; 010: I1:WM_JTAG_JTCLK; 011: O:UART2_RTS; 100:O:PWM2; 101:O:SPI1_CS; 110: B1:I2C_SDA;111:;
26:24	GPIO6	SRW	**Aux Mode of PAD_JTAG_JTMS** 000: B:GPIO6; 001: B1:JTAG_JTMS; 010:I1:WM_JTAG_JTMS; 011: I1:UART2_CTS; 100: O:PTA_EXT_WLAN_ACT; 101: I0:SPI1_MISO; 110: B1:I2C_SCL; 111:;
22:20	GPIO5	SRW	**Aux Mode of PAD_JTAG_JTDI** 000: B:GPIO5; 001: I1:JTAG_JTDI; 010: I1:WM_JTAG_JTDI; 011:O:UART2_TXD; 100:I0:PTA_EXT_PRI; 101: O:SPI1_MOSI; 110:I0:DFD_TDI; 111:;
18:16	GPIO4	SRW	**Aux Mode of PAD_JTAG_JTDO** 000: B:GPIO4; 001: O:JTAG_JTDO; 010: O:WM_JTAG_JTDO; 011:I1:UART2_RXD; 100: I0:PTA_EXT_ACT; 101: O:SPI1_CLK; 110: O:DFD_TDO; 111:;
14:12	GPIO3	SRW	**Aux Mode of PAD_PCIE_PERESET_N** 000: B:GPIO3; 001: O:PCIE_PERESET_N; 010:; 011:; 100:; 101:; 110:; 111:;
10:8	GPIO2	SRW	**Aux Mode of PAD_SYS_WATCHDOG** 000: B:GPIO2; 001: O:SYS_WATCHDOG; 010:; 011:; 100:; 101:; 110:; 111:;
6:4	GPIO1	SRW	**Aux Mode of PAD_GPIO_RESET** 000: B:GPIO1; 001:; 010: B0:WA_AICE_TMSC; 011: B0:WM_AICE_TMSC; 100:; 101: O:WA_UART_TXD; 110: I0:DFD_TCK_XI; 111: O:DBG_MON_A0;
2:0	GPIO0	SRW	**Aux Mode of PAD_GPIO_WPS** 000: B:GPIO0; 001:; 010: I0:WA_AICE_TCKC; 011: I0:WM_AICE_TCKC; 100:; 101: O:WM_UART_TXD; 110: I0:DFD_TMS; 111: O:DBG_MON_A1;

11D00310 **GPIO_MODE1** **Aux Mode of GPIO_MODE1** **11000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15				GPIO14				GPIO13				GPIO12		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO15	SRW	**Aux Mode of PAD_PWM0** 000: B:GPIO15; 001: O:PWM0; 010: O:EMMC_RSTB; 011:O:PWM1; 100: O:NET_WO0_UART_TXD; 101:; 110: O:ANT_SEL10; 111: O:DBG_MON_A12;
26:24	GPIO14	SRW	**Aux Mode of PAD_USB_VBUS** 000: B:GPIO14; 001: O:DRV_VBUS; 010: O:PWM1; 011: O:NET_WO0_UART_TXD; 100:; 101:; 110: O:ANT_SEL11; 111:;
22:20	GPIO13	SRW	**Aux Mode of PAD_WO_JTAG_JTRST_N** 000: B:GPIO13; 001: I0:WO0_JTAG_JTRST_N; 010: O:PWM0; 011: O:GBE_LED1; 100: O:PCM_MCK; 101: O:SYS_WATCHDOG; 110: I0:UDI_NTRST; 111: O:DBG_MON_A13;
18:16	GPIO12	SRW	**Aux Mode of PAD_WO_JTAG_JTCLK** 000: B:GPIO12; 001: I1:WO0_JTAG_JTCLK; 010:; 011:; 100: O:PCM_FS; 101:; 110:I0:UDI_TCK_XI; 111:O:DBG_MON_A14;
14:12	GPIO11	SRW	**Aux Mode of PAD_WO_JTAG_JTMS** 000: B:GPIO11; 001: B1:WO0_JTAG_JTMS; 010:; 011:; 100: O:PCM_CLK; 101:; 110: I0:UDI_TMS; 111:O:DBG_MON_A15;
10:8	GPIO10	SRW	**Aux Mode of PAD_WO_JTAG_JTDI** 000: B:GPIO10; 001: I1:WO0_JTAG_JTDI; 010: B0:WM_AICE_TMSC; 011:; 100: I0:PCM_DRX; 101:; 110: I0:UDI_TDI; 111:O:DBG_MON_A16;
6:4	GPIO9	SRW	**Aux Mode of PAD_WO_JTAG_JTDO** 000: B:GPIO9; 001: O:WO0_JTAG_JTDO; 010: I0:WM_AICE_TCKC; 011:; 100: O:PCM_DTX; 101:; 110: O:UDI_TDO; 111: O:DBG_MON_A17;
2:0	GPIO8	SRW	**Aux Mode of PAD_JTAG_JTRST_N** 000: B:GPIO8; 001: I0:JTAG_JTRST_N; 010: I0:WM_JTAG_JTRST_N; 011: O:GBE_LED0; 100: O:NET_WO0_UART_TXD; 101:; 110: I0:DFD_NTRST; 111:;

11D00320 **GPIO_MODE2** **Aux Mode of GPIO_MODE2** **11111111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23				GPIO22				GPIO21				GPIO20		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO23	SRW	**Aux Mode of PAD_SPI1_MOSI** 000: B:GPIO23; 001: O:SPI1_MOSI; 010: B1:EMMC_DAT7; 011: O:UART2_TXD; 100: I0:PTA_EXT_PRI; 101: I1:WM_JTAG_JTCLK; 110: O:ANT_SEL2; 111: O:DBG_MON_A4;
26:24	GPIO22	SRW	**Aux Mode of PAD_SPI1_CLK** 000: B:GPIO22; 001: O:SPI1_CLK; 010: B1:EMMC_DAT6; 011: I1:UART2_RXD; 100: I0:PTA_EXT_ACT; 101: I1:WM_JTAG_JTMS; 110: O:ANT_SEL3; 111: O:DBG_MON_A5;
22:20	GPIO21	SRW	**Aux Mode of PAD_SPI0_WP** 000: B:GPIO21; 001: B0:SPI0_WP; 010: B1:EMMC_DAT5; 011: B0:SNFI_WP; 100: O:WA_UART_TXD; 101: I1:WM_JTAG_JTDI; 110: O:ANT_SEL4; 111:O:DBG_MON_A6;
18:16	GPIO20	SRW	**Aux Mode of PAD_SPI0_HOLD** 000: B:GPIO20; 001: B0:SPI0_HOLD; 010: B1:EMMC_DAT4; 011: B0:SNFI_HOLD; 100: O:WM_UART_TXD; 101: O:WM_JTAG_JTDO; 110: O:ANT_SEL5; 111: O:DBG_MON_A7;
14:12	GPIO19	SRW	**Aux Mode of PAD_SPI0_CS** 000: B:GPIO19; 001: O:SPI0_CS; 010: B1:EMMC_DAT3; 011: O:SNFI_CS; 100: O:UART1_RTS; 101:; 110: O:ANT_SEL6; 111: O:DBG_MON_A8;
10:8	GPIO18	SRW	**Aux Mode of PAD_SPI0_MISO** 000: B:GPIO18; 001: B0:SPI0_MISO; 010: B1:EMMC_DAT2; 011: B0:SNFI_MISO; 100: I1:UART1_CTS; 101:; 110: O:ANT_SEL7; 111: O:DBG_MON_A9;
6:4	GPIO17	SRW	**Aux Mode of PAD_SPI0_MOSI** 000: B:GPIO17; 001: B0:SPI0_MOSI; 010: B1:EMMC_DAT1; 011: B0:SNFI_MOSI; 100: O:UART1_TXD; 101:; 110: O:ANT_SEL8; 111:O:DBG_MON_A10;
2:0	GPIO16	SRW	**Aux Mode of PAD_SPI0_CLK** 000: B:GPIO16; 001: O:SPI0_CLK; 010: B1:EMMC_DAT0; 011: O:SNFI_CLK; 100: I1:UART1_RXD; 101:; 110: O:ANT_SEL9; 111: O:DBG_MON_A11;

11D00330 GPIO_MODE3 Aux Mode of GPIO_MODE3 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO31				GPIO30				GPIO29				GPIO28		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO31	SRW	**Aux Mode of PAD_SPI2_WP** 000: B:GPIO31; 001: B0:SPI2_WP; 010: O:WF5G_LED; 011: O:WA_UART_TXD; 100: B1:I2C_SDA; 101: B0:WM_AICE_TMSC; 110: B1:U2_PHY_I2C_SDA; 111:;
26:24	GPIO30	SRW	**Aux Mode of PAD_SPI2_HOLD** 000: B:GPIO30; 001: B0:SPI2_HOLD; 010:O:WF2G_LED; 011: O:WM_UART_TXD; 100: B1:I2C_SCL; 101: I0:WM_AICE_TCKC; 110: B1:U2_PHY_I2C_SCL; 111:;
22:20	GPIO29	SRW	**Aux Mode of PAD_SPI2_CS** 000: B:GPIO29; 001: O:SPI2_CS; 010: O:UART1_RTS; 011: B0:WA_AICE_TMSC; 100:; 101: I0:WO0_JTAG_JTRST_N; 110:; 111:;
18:16	GPIO28	SRW	**Aux Mode of PAD_SPI2_MISO** 000: B:GPIO28; 001: B0:SPI2_MISO; 010: I1:UART1_CTS; 011: I0:WA_AICE_TCKC; 100:; 101: I1:WO0_JTAG_JTCLK; 110:; 111:;
14:12	GPIO27	SRW	**Aux Mode of PAD_SPI2_MOSI** 000: B:GPIO27; 001: B0:SPI2_MOSI; 010: O:UART1_TXD; 011:; 100:; 101: B1:WO0_JTAG_JTMS; 110:; 111:;
10:8	GPIO26	SRW	**Aux Mode of PAD_SPI2_CLK** 000: B:GPIO26; 001: O:SPI2_CLK; 010: I1:UART1_RXD; 011:; 100:; 101: I1:WO0_JTAG_JTDI; 110:; 111:;
6:4	GPIO25	SRW	**Aux Mode of PAD_SPI1_CS** 000: B:GPIO25; 001: O:SPI1_CS; 010: B1:EMMC_CLK; 011: O:UART2_RTS; 100: O:PCM_MCK; 101: O:WO0_JTAG_JTDO; 110: O:ANT_SEL0; 111:O:DBG_MON_A2;
2:0	GPIO24	SRW	**Aux Mode of PAD_SPI1_MISO** 000: B:GPIO24; 001: I0:SPI1_MISO; 010: B1:EMMC_CMD; 011: I1:UART2_CTS; 100: O:PTA_EXT_WLAN_ACT; 101: I0:WM_JTAG_JTRST_N; 110: O:ANT_SEL1; 111: O:DBG_MON_A3;

11D00340 GPIO_MODE4 Aux Mode of GPIO_MODE4 01111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO39				GPIO38				GPIO37				GPIO36		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	1		0	0	1		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35				GPIO34				GPIO33				GPIO32		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO39	SRW	**Aux Mode of PAD_GBE_RESET** 000: B:GPIO39; 001:; 010:; 011:; 100:; 101:; 110:; 111:;
26:24	GPIO38	SRW	**Aux Mode of PAD_GBE_INT** 000: B:GPIO38; 001: I0:MT7531_INT; 010:; 011:; 100:; 101:; 110:; 111:;
22:20	GPIO37	SRW	**Aux Mode of PAD_SMI_MDIO** 000: B:GPIO37; 001: B0:SMI_MDIO; 010: B1:I2C_SDA; 011: B1:GBE_EXT_MDIO; 100:; 101:; 110:; 111:;
18:16	GPIO36	SRW	**Aux Mode of PAD_SMI_MDC** 000: B:GPIO36; 001: O:SMI_MDC; 010: B1:I2C_SCL; 011: I1:GBE_EXT_MDC; 100:; 101:; 110:; 111:;
14:12	GPIO35	SRW	**Aux Mode of PAD_PCIE_WAKE_N** 000: B:GPIO35; 001: O:WF5G_LED; 010: I1:PCIE_WAKE_N; 011:; 100:; 101:; 110: O:ANT_SEL13; 111: O:DBG_MON_A18;
10:8	GPIO34	SRW	**Aux Mode of PAD_PCIE_CLK_REQ** 000: B:GPIO34; 001: O:WF2G_LED; 010: B1:PCIE_CLK_REQ; 011:; 100:; 101:; 110: O:ANT_SEL12; 111: O:DBG_MON_A19;
6:4	GPIO33	SRW	**Aux Mode of PAD_UART0_TXD** 000: B:GPIO33; 001: O:UART0_TXD; 010: B1:SGMII1_PHY_I2C_SDA; 011: B1:U3_PHY_I2C_SDA; 100:; 101: B1:SGMII0_PHY_I2C_SDA; 110:; 111:;
2:0	GPIO32	SRW	**Aux Mode of PAD_UART0_RXD** 000: B:GPIO32; 001: I1:UART0_RXD; 010: B1:SGMII1_PHY_I2C_SCL; 011: B1: U3_PHY_I2C_SCL; 100:; 101: B1:SGMII0_PHY_I2C_SCL; 110:; 111:;

11D00350 GPIO_MODE5 Aux Mode of GPIO_MODE5 22211111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO47				GPIO46				GPIO45				GPIO44		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	1	0		0	1	0		0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	1		0	0	1

Bit(s)	Name	Secure	Description
30:28	GPIO47	SRW	**Aux Mode of PAD_WF_HB3** 000: B:GPIO47; 001: B0:WF_HB3; 010: O:WF0_XTAL_SEL_0; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A22;
26:24	GPIO46	SRW	**Aux Mode of PAD_WF_HB2** 000: B:GPIO46; 001:B0:WF_HB2; 010: O:WF0_MODE_SEL_2;011:; 100:; 101:; 110:; 111: O:DBG_MON_A21;
22:20	GPIO45	SRW	**Aux Mode of PAD_WF_HB1** 000: B:GPIO45; 001: B0:WF_HB1; 010: O:WF0_MODE_SEL_1; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A20;
18:16	GPIO44	SRW	**Aux Mode of PAD_WF_TOP_DATA** 000: B:GPIO44; 001: B0:WF0_TOP_DATA; 010:; 011:; 100:; 101:; 110:; 111:;
14:12	GPIO43	SRW	**Aux Mode of PAD_WF_TOP_CLK** 000: B:GPIO43; 001: O:WF0_TOP_CLK; 010:; 011:; 100:; 101:; 110:; 111:;
10:8	GPIO42	SRW	**Aux Mode of PAD_WF_XO_REQ** 000: B:GPIO42; 001: O:WF0_XO_REQ; 010:; 011:; 100:; 101:; 110:; 111:;
6:4	GPIO41	SRW	**Aux Mode of PAD_WF_CBA_RESETB** 000: B:GPIO41; 001: O:WF0_CBA_RESETB; 010:; 011:; 100:; 101:; 110:; 111:;
2:0	GPIO40	SRW	**Aux Mode of PAD_WF_DIG_RESETB** 000: B:GPIO40; 001: O:WF0_DIG_RESETB; 010:; 011:; 100:; 101:; 110:; 111:;

11D00360 GPIO_MODE6 Aux Mode of GPIO_MODE6 00002122

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO55				GPIO54				GPIO53				GPIO52		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		RW				RW				RW				RW		
Reset		0	1	0		0	0	1		0	1	0		0	1	0

Bit(s)	Name	Secure	Description
30:28	GPIO55	SRW	**Aux Mode of PAD_WF_HB9** 000: B:GPIO55; 001: B0:WF_HB9; 010:; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A30;
26:24	GPIO54	SRW	**Aux Mode of PAD_WF_HB8** 000: B:GPIO54; 001: B0:WF_HB8; 010:; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A29;
22:20	GPIO53	SRW	**Aux Mode of PAD_WF_HB7** 000: B:GPIO53; 001: B0:WF_HB7; 010:; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A28;
18:16	GPIO52	SRW	**Aux Mode of PAD_WF_HB6** 000: B:GPIO52; 001: B0:WF_HB6; 010:; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A27;
14:12	GPIO51	SRW	**Aux Mode of PAD_WF_HB5** 000: B:GPIO51; 001: B0:WF_HB5; 010: O:WF0_XTAL_SEL_2; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A26;
10:8	GPIO50	SRW	**Aux Mode of PAD_WF_HB0_B** 000: B:GPIO50; 001: O:WF_O_HB0_B; 010:; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A25;
6:4	GPIO49	SRW	**Aux Mode of PAD_WF_HB0** 000: B:GPIO49; 001: O:WF_O_HB0; 010: O:WF0_MODE_SEL_0; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A24;
2:0	GPIO48	SRW	**Aux Mode of PAD_WF_HB4** 000: B:GPIO48; 001: B0:WF_HB4; 010: O:WF0_XTAL_SEL_1; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A23;

11D00370 GPIO_MODE7 Aux Mode of GPIO_MODE7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO63				GPIO62				GPIO61				GPIO60		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59				GPIO58				GPIO57				GPIO56		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO63	SRW	**Aux Mode of Reserved** 000: Reserved
26:24	GPIO62	SRW	**Aux Mode of Reserved** 000: Reserved
22:20	GPIO61	SRW	**Aux Mode of Reserved** 000: Reserved
18:16	GPIO60	SRW	**Aux Mode of Reserved** 000: Reserved
14:12	GPIO59	SRW	**Aux Mode of Reserved** 000: Reserved
10:8	GPIO58	SRW	**Aux Mode of Reserved** 000: Reserved
6:4	GPIO57	SRW	**Aux Mode of Reserved** 000: Reserved
2:0	GPIO56	SRW	**Aux Mode of PAD_WF_HB10** 000: B:GPIO56; 001: B0:WF_HB10; 010:; 011:; 100:; 101:; 110:; 111: O:DBG_MON_A31;

11D00304 GPIO_MODE0_SET Bitwise Set of Aux Mode of GPIO_MODE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO7				GPIO6				GPIO5				GPIO4		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO3				GPIO2				GPIO1				GPIO0		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO7	SW	**Bitwise SET of Aux Mode of PAD_JTAG_JTCLK** 0: Keep; 1: SET bit;
26:24	GPIO6	SW	**Bitwise SET of Aux Mode of PAD_JTAG_JTMS** 0: Keep; 1: SET bit;
22:20	GPIO5	SW	**Bitwise SET of Aux Mode of PAD_JTAG_JTDI** 0: Keep; 1: SET bit;
18:16	GPIO4	SW	**Bitwise SET of Aux Mode of PAD_JTAG_JTDO** 0: Keep; 1: SET bit;
14:12	GPIO3	SW	**Bitwise SET of Aux Mode of PAD_PCIE_PERESET_N** 0: Keep; 1: SET bit;
10:8	GPIO2	SW	**Bitwise SET of Aux Mode of PAD_SYS_WATCHDOG** 0: Keep; 1: SET bit;
6:4	GPIO1	SW	**Bitwise SET of Aux Mode of PAD_GPIO_RESET** 0: Keep; 1: SET bit;
2:0	GPIO0	SW	**Bitwise SET of Aux Mode of PAD_GPIO_WPS** 0: Keep; 1: SET bit;

11D00314 GPIO_MODE1_SET Bitwise Set of Aux Mode of GPIO_MODE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15				GPIO14				GPIO13				GPIO12		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO15	SW	**Bitwise SET of Aux Mode of PAD_PWM0** 0: Keep; 1: SET bit;
26:24	GPIO14	SW	**Bitwise SET of Aux Mode of PAD_USB_VBUS** 0: Keep; 1: SET bit;
22:20	GPIO13	SW	**Bitwise SET of Aux Mode of PAD_WO_JTAG_JTRST_N** 0: Keep; 1: SET bit;
18:16	GPIO12	SW	**Bitwise SET of Aux Mode of PAD_WO_JTAG_JTCLK** 0: Keep; 1: SET bit;
14:12	GPIO11	SW	**Bitwise SET of Aux Mode of PAD_WO_JTAG_JTMS** 0: Keep; 1: SET bit;
10:8	GPIO10	SW	**Bitwise SET of Aux Mode of PAD_WO_JTAG_JTDI** 0: Keep; 1: SET bit;
6:4	GPIO9	SW	**Bitwise SET of Aux Mode of PAD_WO_JTAG_JTDO** 0: Keep; 1: SET bit;
2:0	GPIO8	SW	**Bitwise SET of Aux Mode of PAD_JTAG_JTRST_N** 0: Keep; 1: SET bit;

11D00324 **GPIO_MODE2_SET** **Bitwise Set of Aux Mode of GPIO_MODE2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23				GPIO22				GPIO21				GPIO20		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO23	SW	**Bitwise SET of Aux Mode of PAD_SPI1_MOSI** 0: Keep; 1: SET bit;
26:24	GPIO22	SW	**Bitwise SET of Aux Mode of PAD_SPI1_CLK** 0: Keep; 1: SET bit;
22:20	GPIO21	SW	**Bitwise SET of Aux Mode of PAD_SPI0_WP** 0: Keep; 1: SET bit;
18:16	GPIO20	SW	**Bitwise SET of Aux Mode of PAD_SPI0_HOLD** 0: Keep; 1: SET bit;
14:12	GPIO19	SW	**Bitwise SET of Aux Mode of PAD_SPI0_CS** 0: Keep; 1: SET bit;
10:8	GPIO18	SW	**Bitwise SET of Aux Mode of PAD_SPI0_MISO** 0: Keep; 1: SET bit;
6:4	GPIO17	SW	**Bitwise SET of Aux Mode of PAD_SPI0_MOSI** 0: Keep; 1: SET bit;
2:0	GPIO16	SW	**Bitwise SET of Aux Mode of PAD_SPI0_CLK** 0: Keep; 1: SET bit;

11D00334 **GPIO_MODE3_SET** **Bitwise Set of Aux Mode of GPIO_MODE3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO31				GPIO30				GPIO29				GPIO28		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO31	SW	**Bitwise SET of Aux Mode of PAD_SPI2_WP** 0: Keep; 1: SET bit;
26:24	GPIO30	SW	**Bitwise SET of Aux Mode of PAD_SPI2_HOLD** 0: Keep; 1: SET bit;
22:20	GPIO29	SW	**Bitwise SET of Aux Mode of PAD_SPI2_CS** 0: Keep; 1: SET bit;
18:16	GPIO28	SW	**Bitwise SET of Aux Mode of PAD_SPI2_MISO** 0: Keep; 1: SET bit;
14:12	GPIO27	SW	**Bitwise SET of Aux Mode of PAD_SPI2_MOSI** 0: Keep; 1: SET bit;
10:8	GPIO26	SW	**Bitwise SET of Aux Mode of PAD_SPI2_CLK** 0: Keep; 1: SET bit;
6:4	GPIO25	SW	**Bitwise SET of Aux Mode of PAD_SPI1_CS** 0: Keep; 1: SET bit;
2:0	GPIO24	SW	**Bitwise SET of Aux Mode of PAD_SPI1_MISO** 0: Keep; 1: SET bit;

11D00344 GPIO_MODE4_SET Bitwise Set of Aux Mode of GPIO_MODE4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO39				GPIO38				GPIO37				GPIO36		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35				GPIO34				GPIO33				GPIO32		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO39	SW	**Bitwise SET of Aux Mode of PAD_GBE_RESET** 0: Keep; 1: SET bit;
26:24	GPIO38	SW	**Bitwise SET of Aux Mode of PAD_GBE_INT** 0: Keep; 1: SET bit;
22:20	GPIO37	SW	**Bitwise SET of Aux Mode of PAD_SMI_MDIO** 0: Keep; 1: SET bit;
18:16	GPIO36	SW	**Bitwise SET of Aux Mode of PAD_SMI_MDC** 0: Keep; 1: SET bit;
14:12	GPIO35	SW	**Bitwise SET of Aux Mode of PAD_PCIE_WAKE_N** 0: Keep; 1: SET bit;
10:8	GPIO34	SW	**Bitwise SET of Aux Mode of PAD_PCIE_CLK_REQ** 0: Keep; 1: SET bit;
6:4	GPIO33	SW	**Bitwise SET of Aux Mode of PAD_UART0_TXD** 0: Keep; 1: SET bit;
2:0	GPIO32	SW	**Bitwise SET of Aux Mode of PAD_UART0_RXD** 0: Keep; 1: SET bit;

11D00354 GPIO_MODE5_SET Bitwise Set of Aux Mode of GPIO_MODE5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO47				GPIO46				GPIO45				GPIO44		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO47	SW	**Bitwise SET of Aux Mode of PAD_WF_HB3** 0: Keep; 1: SET bit;
26:24	GPIO46	SW	**Bitwise SET of Aux Mode of PAD_WF_HB2** 0: Keep; 1: SET bit;
22:20	GPIO45	SW	**Bitwise SET of Aux Mode of PAD_WF_HB1** 0: Keep; 1: SET bit;
18:16	GPIO44	SW	**Bitwise SET of Aux Mode of PAD_WF_TOP_DATA** 0: Keep; 1: SET bit;
14:12	GPIO43	SW	**Bitwise SET of Aux Mode of PAD_WF_TOP_CLK** 0: Keep; 1: SET bit;
10:8	GPIO42	SW	**Bitwise SET of Aux Mode of PAD_WF_XO_REQ** 0: Keep; 1: SET bit;
6:4	GPIO41	SW	**Bitwise SET of Aux Mode of PAD_WF_CBA_RESETB** 0: Keep; 1: SET bit;
2:0	GPIO40	SW	**Bitwise SET of Aux Mode of PAD_WF_DIG_RESETB** 0: Keep; 1: SET bit;

11D00364 **GPIO_MODE6_SET** **Bitwise Set of Aux Mode of GPIO_MODE6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO55				GPIO54				GPIO53				GPIO52		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO55	SW	**Bitwise SET of Aux Mode of PAD_WF_HB9** 0: Keep; 1: SET bit;
26:24	GPIO54	SW	**Bitwise SET of Aux Mode of PAD_WF_HB8** 0: Keep; 1: SET bit;
22:20	GPIO53	SW	**Bitwise SET of Aux Mode of PAD_WF_HB7** 0: Keep; 1: SET bit;
18:16	GPIO52	SW	**Bitwise SET of Aux Mode of PAD_WF_HB6** 0: Keep; 1: SET bit;
14:12	GPIO51	SW	**Bitwise SET of Aux Mode of PAD_WF_HB5** 0: Keep; 1: SET bit;
10:8	GPIO50	SW	**Bitwise SET of Aux Mode of PAD_WF_HB0_B** 0: Keep; 1: SET bit;
6:4	GPIO49	SW	**Bitwise SET of Aux Mode of PAD_WF_HB0** 0: Keep; 1: SET bit;
2:0	GPIO48	SW	**Bitwise SET of Aux Mode of PAD_WF_HB4** 0: Keep; 1: SET bit;

11D00374 GPIO_MODE7_SET Bitwise Set of Aux Mode of GPIO_MODE7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO63				GPIO62				GPIO61				GPIO60		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59				GPIO58				GPIO57				GPIO56		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO63	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
26:24	GPIO62	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
22:20	GPIO61	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
18:16	GPIO60	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
14:12	GPIO59	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
10:8	GPIO58	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
6:4	GPIO57	SW	**Bitwise SET of Aux Mode of Reserved** 0: Keep; 1: SET bit;
2:0	GPIO56	SW	**Bitwise SET of Aux Mode of PAD_WF_HB10** 0: Keep; 1: SET bit;

11D00308 GPIO_MODE0_CLR Bitwise Clear of Aux Mode of GPIO_MODE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO7				GPIO6				GPIO5				GPIO4		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO3				GPIO2				GPIO1				GPIO0		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO7	SW	**Bitwise CLR of Aux Mode of PAD_JTAG_JTCLK** 0: Keep; 1: CLR bit
26:24	GPIO6	SW	**Bitwise CLR of Aux Mode of PAD_JTAG_JTMS** 0: Keep; 1: CLR bit
22:20	GPIO5	SW	**Bitwise CLR of Aux Mode of PAD_JTAG_JTDI** 0: Keep; 1: CLR bit
18:16	GPIO4	SW	**Bitwise CLR of Aux Mode of PAD_JTAG_JTDO** 0: Keep; 1: CLR bit
14:12	GPIO3	SW	**Bitwise CLR of Aux Mode of PAD_PCIE_PERESET_N** 0: Keep; 1: CLR bit
10:8	GPIO2	SW	**Bitwise CLR of Aux Mode of PAD_SYS_WATCHDOG** 0: Keep; 1: CLR bit
6:4	GPIO1	SW	**Bitwise CLR of Aux Mode of PAD_GPIO_RESET** 0: Keep; 1: CLR bit
2:0	GPIO0	SW	**Bitwise CLR of Aux Mode of PAD_GPIO_WPS** 0: Keep; 1: CLR bit

11D00318 GPIO_MODE1_CLR Bitwise Clear of Aux Mode of GPIO_MODE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15				GPIO14				GPIO13				GPIO12		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO15	SW	**Bitwise CLR of Aux Mode of PAD_PWM0** 0: Keep; 1: CLR bit
26:24	GPIO14	SW	**Bitwise CLR of Aux Mode of PAD_USB_VBUS** 0: Keep; 1: CLR bit
22:20	GPIO13	SW	**Bitwise CLR of Aux Mode of PAD_WO_JTAG_JTRST_N** 0: Keep; 1: CLR bit
18:16	GPIO12	SW	**Bitwise CLR of Aux Mode of PAD_WO_JTAG_JTCLK** 0: Keep; 1: CLR bit
14:12	GPIO11	SW	**Bitwise CLR of Aux Mode of PAD_WO_JTAG_JTMS** 0: Keep; 1: CLR bit
10:8	GPIO10	SW	**Bitwise CLR of Aux Mode of PAD_WO_JTAG_JTDI** 0: Keep; 1: CLR bit
6:4	GPIO9	SW	**Bitwise CLR of Aux Mode of PAD_WO_JTAG_JTDO** 0: Keep; 1: CLR bit
2:0	GPIO8	SW	**Bitwise CLR of Aux Mode of PAD_JTAG_JTRST_N** 0: Keep; 1: CLR bit

11D00328 GPIO_MODE2_CLR Bitwise Clear of Aux Mode of GPIO_MODE2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23				GPIO22				GPIO21				GPIO20		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO23	SW	**Bitwise CLR of Aux Mode of PAD_SPI1_MOSI** 0: Keep; 1: CLR bit
26:24	GPIO22	SW	**Bitwise CLR of Aux Mode of PAD_SPI1_CLK** 0: Keep; 1: CLR bit
22:20	GPIO21	SW	**Bitwise CLR of Aux Mode of PAD_SPI0_WP** 0: Keep; 1: CLR bit
18:16	GPIO20	SW	**Bitwise CLR of Aux Mode of PAD_SPI0_HOLD** 0: Keep; 1: CLR bit
14:12	GPIO19	SW	**Bitwise CLR of Aux Mode of PAD_SPI0_CS** 0: Keep; 1: CLR bit
10:8	GPIO18	SW	**Bitwise CLR of Aux Mode of PAD_SPI0_MISO** 0: Keep; 1: CLR bit
6:4	GPIO17	SW	**Bitwise CLR of Aux Mode of PAD_SPI0_MOSI** 0: Keep; 1: CLR bit
2:0	GPIO16	SW	**Bitwise CLR of Aux Mode of PAD_SPI0_CLK** 0: Keep; 1: CLR bit

11D00338 GPIO_MODE3_CLR Bitwise Clear of Aux Mode of GPIO_MODE3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO31				GPIO30				GPIO29				GPIO28		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO27				GPIO26				GPIO25				GPIO24		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO31	SW	**Bitwise CLR of Aux Mode of PAD_SPI2_WP** 0: Keep; 1: CLR bit
26:24	GPIO30	SW	**Bitwise CLR of Aux Mode of PAD_SPI2_HOLD** 0: Keep; 1: CLR bit
22:20	GPIO29	SW	**Bitwise CLR of Aux Mode of PAD_SPI2_CS** 0: Keep; 1: CLR bit
18:16	GPIO28	SW	**Bitwise CLR of Aux Mode of PAD_SPI2_MISO** 0: Keep; 1: CLR bit
14:12	GPIO27	SW	**Bitwise CLR of Aux Mode of PAD_SPI2_MOSI** 0: Keep; 1: CLR bit
10:8	GPIO26	SW	**Bitwise CLR of Aux Mode of PAD_SPI2_CLK** 0: Keep; 1: CLR bit
6:4	GPIO25	SW	**Bitwise CLR of Aux Mode of PAD_SPI1_CS** 0: Keep; 1: CLR bit
2:0	GPIO24	SW	**Bitwise CLR of Aux Mode of PAD_SPI1_MISO** 0: Keep; 1: CLR bit

11D00348 GPIO_MODE4_CLR Bitwise Clear of Aux Mode of GPIO_MODE4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO39				GPIO38				GPIO37				GPIO36		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO35				GPIO34				GPIO33				GPIO32		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO39	SW	**Bitwise CLR of Aux Mode of PAD_GBE_RESET** 0: Keep; 1: CLR bit
26:24	GPIO38	SW	**Bitwise CLR of Aux Mode of PAD_GBE_INT** 0: Keep; 1: CLR bit
22:20	GPIO37	SW	**Bitwise CLR of Aux Mode of PAD_SMI_MDIO** 0: Keep; 1: CLR bit
18:16	GPIO36	SW	**Bitwise CLR of Aux Mode of PAD_SMI_MDC** 0: Keep; 1: CLR bit
14:12	GPIO35	SW	**Bitwise CLR of Aux Mode of PAD_PCIE_WAKE_N** 0: Keep; 1: CLR bit
10:8	GPIO34	SW	**Bitwise CLR of Aux Mode of PAD_PCIE_CLK_REQ** 0: Keep; 1: CLR bit
6:4	GPIO33	SW	**Bitwise CLR of Aux Mode of PAD_UART0_TXD** 0: Keep; 1: CLR bit
2:0	GPIO32	SW	**Bitwise CLR of Aux Mode of PAD_UART0_RXD** 0: Keep; 1: CLR bit

11D00358 GPIO_MODE5_CLR Bitwise Clear of Aux Mode of GPIO_MODE5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO47				GPIO46				GPIO45				GPIO44		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO43				GPIO42				GPIO41				GPIO40		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO47	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB3** 0: Keep; 1: CLR bit
26:24	GPIO46	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB2** 0: Keep; 1: CLR bit
22:20	GPIO45	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB1** 0: Keep; 1: CLR bit
18:16	GPIO44	SW	**Bitwise CLR of Aux Mode of PAD_WF_TOP_DATA** 0: Keep; 1: CLR bit
14:12	GPIO43	SW	**Bitwise CLR of Aux Mode of PAD_WF_TOP_CLK** 0: Keep; 1: CLR bit
10:8	GPIO42	SW	**Bitwise CLR of Aux Mode of PAD_WF_XO_REQ** 0: Keep; 1: CLR bit
6:4	GPIO41	SW	**Bitwise CLR of Aux Mode of PAD_WF_CBA_RESETB** 0: Keep; 1: CLR bit
2:0	GPIO40	SW	**Bitwise CLR of Aux Mode of PAD_WF_DIG_RESETB** 0: Keep; 1: CLR bit

11D00368 GPIO_MODE6_CLR Bitwise Clear of Aux Mode of GPIO_MODE6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO55				GPIO54				GPIO53				GPIO52		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO51				GPIO50				GPIO49				GPIO48		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO55	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB9** 0: Keep; 1: CLR bit
26:24	GPIO54	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB8** 0: Keep; 1: CLR bit
22:20	GPIO53	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB7** 0: Keep; 1: CLR bit
18:16	GPIO52	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB6** 0: Keep; 1: CLR bit
14:12	GPIO51	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB5** 0: Keep; 1: CLR bit
10:8	GPIO50	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB0_B** 0: Keep; 1: CLR bit
6:4	GPIO49	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB0** 0: Keep; 1: CLR bit
2:0	GPIO48	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB4** 0: Keep; 1: CLR bit

11D00378 GPIO_MODE7_CLR Bitwise Clear of Aux Mode of GPIO_MODE7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO63				GPIO62				GPIO61				GPIO60		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO59				GPIO58				GPIO57				GPIO56		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Secure	Description
30:28	GPIO63	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
26:24	GPIO62	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
22:20	GPIO61	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
18:16	GPIO60	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
14:12	GPIO59	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
10:8	GPIO58	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
6:4	GPIO57	SW	**Bitwise CLR of Aux Mode of Reserved** 0: Keep; 1: CLR bit
2:0	GPIO56	SW	**Bitwise CLR of Aux Mode of PAD_WF_HB10** 0: Keep; 1: CLR bit

11D0030C GPIO_MODE0_MOD Alternative way to set Aux Mode of GPIO_MODE0_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7				GPIO6				GPIO5				GPIO4			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3				GPIO2				GPIO1				GPIO0			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO7	SW	**Alternative way to set up Aux mode of PAD_JTAG_JTCLK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO6	SW	**Alternative way to set up Aux mode of PAD_JTAG_JTMS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO5	SW	**Alternative way to set up Aux mode of PAD_JTAG_JTDI** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO4	SW	**Alternative way to set up Aux mode of PAD_JTAG_JTDO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO3	SW	**Alternative way to set up Aux mode of PAD_PCIE_PERESET_N** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO2	SW	**Alternative way to set up Aux mode of PAD_SYS_WATCHDOG** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO1	SW	**Alternative way to set up Aux mode of PAD_GPIO_RESET** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO0	SW	**Alternative way to set up Aux mode of PAD_GPIO_WPS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0031C GPIO_MODE1_MOD Alternative way to set Aux mode of GPIO_MODE1_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO15				GPIO14				GPIO13				GPIO12			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO11				GPIO10				GPIO9				GPIO8			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO15	SW	**Alternative way to set up Aux mode of PAD_PWM0** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO14	SW	**Alternative way to set up Aux mode of PAD_USB_VBUS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO13	SW	**Alternative way to set up Aux mode of PAD_WO_JTAG_JTRST_N** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO12	SW	**Alternative way to set up Aux mode of PAD_WO_JTAG_JTCLK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO11	SW	**Alternative way to set up Aux mode of PAD_WO_JTAG_JTMS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO10	SW	**Alternative way to set up Aux mode of PAD_WO_JTAG_JTDI** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO9	SW	**Alternative way to set up Aux mode of PAD_WO_JTAG_JTDO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO8	SW	**Alternative way to set up Aux mode of PAD_JTAG_JTRST_N** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0032C GPIO_MODE2_MOD Alternative way to set Aux mode of GPIO_MODE2_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO23				GPIO22				GPIO21				GPIO20			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO19				GPIO18				GPIO17				GPIO16			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO23	SW	**Alternative way to set up Aux mode of PAD_SPI1_MOSI** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO22	SW	**Alternative way to set up Aux mode of PAD_SPI1_CLK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO21	SW	**Alternative way to set up Aux mode of PAD_SPI0_WP** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO20	SW	**Alternative way to set up Aux mode of PAD_SPI0_HOLD** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO19	SW	**Alternative way to set up Aux mode of PAD_SPI0_CS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO18	SW	**Alternative way to set up Aux mode of PAD_SPI0_MISO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO17	SW	**Alternative way to set up Aux mode of PAD_SPI0_MOSI** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO16	SW	**Alternative way to set up Aux mode of PAD_SPI0_CLK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0033C GPIO_MODE3_MOD Alternative way to set Aux mode of GPIO_MODE3_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31				GPIO30				GPIO29				GPIO28			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO27				GPIO26				GPIO25				GPIO24			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO31	SW	**Alternative way to set up Aux mode of PAD_SPI2_WP** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO30	SW	**Alternative way to set up Aux mode of PAD_SPI2_HOLD** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO29	SW	**Alternative way to set up Aux mode of PAD_SPI2_CS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO28	SW	**Alternative way to set up Aux mode of PAD_SPI2_MISO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO27	SW	**Alternative way to set up Aux mode of PAD_SPI2_MOSI** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO26	SW	**Alternative way to set up Aux mode of PAD_SPI2_CLK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO25	SW	**Alternative way to set up Aux mode of PAD_SPI1_CS** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO24	SW	**Alternative way to set up Aux mode of PAD_SPI1_MISO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0034C GPIO_MODE4_MOD Alternative way to set Aux mode of GPIO_MODE4_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO39				GPIO38				GPIO37				GPIO36			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO35				GPIO34				GPIO33				GPIO32			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO39	SW	**Alternative way to set up Aux mode of PAD_GBE_RESET** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO38	SW	**Alternative way to set up Aux mode of PAD_GBE_INT** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO37	SW	**Alternative way to set up Aux mode of PAD_SMI_MDIO** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO36	SW	**Alternative way to set up Aux mode of PAD_SMI_MDC** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO35	SW	**Alternative way to set up Aux mode of PAD_PCIE_WAKE_N** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO34	SW	**Alternative way to set up Aux mode of PAD_PCIE_CLK_REQ** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO33	SW	**Alternative way to set up Aux mode of PAD_UART0_TXD** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO32	SW	**Alternative way to set up Aux mode of PAD_UART0_RXD** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0035C GPIO_MODE5_MOD Alternative way to set Aux mode of GPIO_MODE5_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO47				GPIO46				GPIO45				GPIO44			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO43				GPIO42				GPIO41				GPIO40			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO47	SW	**Alternative way to set up Aux mode of PAD_WF_HB3** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO46	SW	**Alternative way to set up Aux mode of PAD_WF_HB2** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO45	SW	**Alternative way to set up Aux mode of PAD_WF_HB1** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO44	SW	**Alternative way to set up Aux mode of PAD_WF_TOP_DATA** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO43	SW	**Alternative way to set up Aux mode of PAD_WF_TOP_CLK** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO42	SW	**Alternative way to set up Aux mode of PAD_WF_XO_REQ** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO41	SW	**Alternative way to set up Aux mode of PAD_WF_CBA_RESETB** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO40	SW	**Alternative way to set up Aux mode of PAD_WF_DIG_RESETB** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0036C GPIO_MODE6_MOD Alternative way to set Aux mode of GPIO_MODE6_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO55				GPIO54				GPIO53				GPIO52			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO51				GPIO50				GPIO49				GPIO48			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO55	SW	**Alternative way to set up Aux mode of PAD_WF_HB9** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO54	SW	**Alternative way to set up Aux mode of PAD_WF_HB8** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO53	SW	**Alternative way to set up Aux mode of PAD_WF_HB7** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO52	SW	**Alternative way to set up Aux mode of PAD_WF_HB6** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO51	SW	**Alternative way to set up Aux mode of PAD_WF_HB5** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO50	SW	**Alternative way to set up Aux mode of PAD_WF_HB0_B** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO49	SW	**Alternative way to set up Aux mode of PAD_WF_HB0** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO48	SW	**Alternative way to set up Aux mode of PAD_WF_HB4** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D0037C GPIO_MODE7_MOD Alternative way to set Aux mode of GPIO_MODE7_MOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO63				GPIO62				GPIO61				GPIO60			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO59				GPIO58				GPIO57				GPIO56			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:28	GPIO63	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
27:24	GPIO62	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
23:20	GPIO61	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
19:16	GPIO60	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
15:12	GPIO59	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
11:8	GPIO58	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
7:4	GPIO57	SW	**Alternative way to set up Aux mode of Reserved** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.
3:0	GPIO56	SW	**Alternative way to set up Aux mode of PAD_WF_HB10** [2:0]: Target Aux. mode [3]: Enable mode setup 0: Mode is not set. 1: Mode is set.

11D00600 MISC Chip Related Misc Options 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**Chip related misc options**

11D00604 MISC_SET Chip Related Misc Options 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**Chip related misc options** 0: Keep; 1: SET bit;

11D00608 MISC_CLR Chip Related Misc Options 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**Chip related misc options** 0: Keep; 1: CLR bit

11D006D0 DBG dbg_mon Control Bit 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	dbg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	dbg															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	dbg		**dbg_mon control bit**

11D006E0 BANK GPIO Reserved Control Register [0]: test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	GPIO_REG		**GPIO reserved control register [0]: test_normal_sel_bypreg**

11D006F0 **TPBANK0** **Trapping Force Enable** **00000920**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rev1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rev1				TRAP_LATCH			boot_xtal_sel40m	boot_mode		TRAP_FORCE_VAL			TRAP_FORCE_EN		
Type	RU				RU			RU	RU		RW			RW		
Reset	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:12	rev1		**Reserved bits**
11:9	TRAP_LATCH		**TRAP_LATCH value**
8	boot_xtal_sel40m		**boot_xtal_sel40m value**
7:6	boot_mode		**boot_mode value**
5:3	TRAP_FORCE_VAL		**Trapping force value**
2:0	TRAP_FORCE_EN		**Enable Trapping force**

11D00710 AP_GOOD Chip Related AP_GPPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**Chip related AP_GPPD control**

11D00714 AP_GOOD_SET Chip Related AP_GPPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**Chip related AP_GPPD control** 0: Keep; 1: SET bit;

11D00718 AP_GOOD_CLR Chip Related AP_GPPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**Chip related AP_GPPD control** 0: Keep; 1: CLR bit

11D00720 MODE_CFG_CT_REG GPIO Reserved Control Register [0]: test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**GPIO reserved control register [0]: test_normal_sel_bypreg**

11D00724 MODE_CFG_CT_REG_SET GPIO Reserved Control Register [0]: test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**GPIO reserved control register [0]: test_normal_sel_bypreg** 0: Keep; 1: SET bit;

11D00728 MODE_CFG_CT_REG_CLR GPIO Reserved Control Register [0]: test_normal_sel_bypreg 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DUMMY															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Secure	Description
31:0	DUMMY		**GPIO reserved control register [0]: test_normal_sel_bypreg** 0: Keep; 1: CLR bit

5 Connectivity

5.1 NETSYS

5.1.1 Register Definition

Module name: ETHDMASYS_SYSCTL Base address: (+0x1500_0000)

Address	Name	Width	Register Function
1500000C	REVISION_ID	32	ETHSYS Revision Identification
15000010	SYSCFG0	32	System Configuration Register 0
15000014	SYSCFG1	32	System Configuration Register 1
15000018	TESTSTAT0	32	Firmware Test Status 0
1500001C	TESTSTAT1	32	Firmware Test Status 1
15000024	BOOT_RELEASE	32	Release CPU's Command to Boot from SRAM
1500002C	CLKCFG0	32	Clock Configuration Register 0
15000030	CLKCFG1	32	Clock Configuration Register 1
15000034	RSTCTL	32	Reset Control Register
15000038	RSTSTAT	32	Reset Status Register
15000040	GPIO0_MODE	32	GPIO0 Purpose Selection
15000044	GPIO1_MODE	32	GPIO1 Purpose Selection
15000048	MEMO0	32	Memory0
1500004C	MEMO1	32	Memory1
15000050	MEMO2	32	Memory2
15000054	MEMO3	32	Memory3
15000058	MEMO4	32	Memory4
1500005C	MEMO5	32	Memory5
15000060	IOC_EN	32	NETSYS IO Coherence Enable Register
15000064	BIST_CTRL	32	NETSYS Global BIST Configuration Register
15000068	BIST_NETSYS2EMI0	32	NETSYS2EMI_M0 BIST Configuration Register 0
1500006C	BIST_NETSYS2EMI1	32	NETSYS2EMI_M0 BIST Configuration Register 1
15000070	BIST_NETSYS2EMI2	32	NETSYS2EMI_M1 BIST Configuration Register 0
15000074	BIST_NETSYS2EMI3	32	NETSYS2EMI_M1 BIST Configuration Register 1
15000078	BIST_NETSYS2INFRA0	32	NETSYS2INFRA BIST Configuration Register 0
1500007C	BIST_NETSYS2INFRA1	32	NETSYS2INFRA BIST Configuration Register 1
15000080	AXICFG0	32	AXI Sideband Configuration Register 0
15000084	AXICFG1	32	AXI Sideband Configuration Register 1
15000088	GALSCFG0	32	GALS Configuration Register 0
1500008C	GALSCFG1	32	GALS Configuration Register 1
15000090	MISTAT	32	NETSYS Bus MI Status Register
15000094	SI0STAT0	32	NETSYS Bus SI Status Register 0
15000098	SI0STAT1	32	NETSYS Bus SI Status Register 1
1500009C	SI0STAT2	32	NETSYS Bus SI Status Register 2
150000A0	S2PSTAT0	32	NETSYS Bus S2P Status Register 0
150000A4	S2PSTAT1	32	NETSYS Bus S2P Status Register 1
150000A8	X2SSTAT0	32	NETSYS Bus X2S Status Register 0
150000AC	X2SSTAT1	32	NETSYS Bus X2S Status Register 1
150000B0	R2XCFG0	32	R2X Configuration Register 0
150000B4	R2XCFG1	32	R2X Configuration Register 1
150000B8	R2XSTAT0	32	R2X Status Register 0
150000BC	R2XSTAT1	32	R2X Status Register 1
150000C0	APBCFG	32	NETSYS_APB Configuration Register
150000C4	APBSTAT	32	NETSYS_APB Status Register

1500000C **REVISION_ID** **ETHSYS Revision Identification** **22000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ETHSYS_VER															
Type	RO															
Reset	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ETHSYS_VER								ETHSYS_ECO_ID							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	ETHSYS_VER	**ETHSYS revision number**
7:0	ETHSYS_ECO_ID	**ETHSYS ECO ID (IPM version in FPGA)**

15000010 SYSCFG0 System Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST_CODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:24	TEST_CODE	**Default value is from bootstrap and can be modified by software.**

15000014 SYSCFG1 System Configuration Register 1 00110014

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RSV1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GE2_MODE		GE1_MODE		GE0_MODE		SGMII_CONFIG_0	SGMII_CONFIG_1	RSV0							
Type	RW		RW		RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
31:16	RSV1	**Reserved**
15:14	GE2_MODE	**Gigabit Port #2 Mode** Sets the interface mode on Gigabit port 2 0: RGMII Mode (10/100/1000 Mbps) 1: MII Mode (10/100 Mbps) 2: Reverse MII Mode (10/100 Mbps) 3: Reduced MII (10/100Mbps)
13:12	GE1_MODE	**Gigabit Port #1 Mode** Sets the interface mode on Gigabit port 1 0: RGMII Mode (10/100/1000 Mbps) 1: MII Mode (10/100 Mbps) 2: Reverse MII Mode (10/100 Mbps) 3: Reserved
11:10	GE0_MODE	**Gigabit Port #0 Mode** Sets the interface mode on Gigabit port 0 0: RGMII Mode (10/100/1000 Mbps) 1: MII Mode (10/100 Mbps) 2: Reverse MII Mode (10/100 Mbps) 3: Reserved
9	SGMII_CONFIG_0	**Enable SGMII path of GMAC1** 0: Disable SGMII 1: Enable SGMII
8	SGMII_CONFIG_1	**Enable SGMII path of GMAC2** 0: Disable SGMII

Bit(s)	Name	Description
		1: Enable SGMII
7:0	RSV0	**Reserved**

15000018 TESTSTAT0 Firmware Test Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTSTAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTSTAT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TESTSTAT0	**Firmware Test Status Register 0** NOTE: This register is reset only by a power-on reset.

1500001C **TESTSTAT1** **Firmware Test Status 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TESTSTAT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TESTSTAT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TESTSTAT1	**Firmware Test Status Register 1** NOTE: This register is reset only by a power-on reset.

15000024 BOOT_RELEASE Release CPU's Command to Boot from SRAM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BOOT_RELEASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BOOT_RELEASE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BOOT_RELEASE	**Reserved**

1500002C **CLKCFG0** **Clock Configuration Register 0** **C4001FE0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	OSC_1US_DIV															
Type	RW															
Reset	1	1	0	0	0	1										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:26	OSC_1US_DIV	**Oscillator 1 usec Divider** Sets the maximum for the reference clock counter for either a 20 MHz or 40 MHz external XTAL input. The count increments each 1usec (indicating 1 MHz), up to the maximum, before resetting to zero. This counts the frequency of an external XTAL. This count is used to output a 32 kHz frequency to the REFCLK0 pin. 0: Automatically generates a 1 usec system tick regardless of whether XTAL frequency is 20 MHz or 40 MHz. 49: Default value for a reference 50 MHz clock. 39: Default value for an external 40 MHz XTAL. 19: Default value for an external 20 MHz XTAL. Others: Manual mode for tick generation.

15000030 **CLKCFG1** **Clock Configuration Register 1** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																ESW_CLK_EN
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WOCPU0_CLK_EN	WOCPU1_CLK_EN					GP0_CLK_EN	GP1_CLK_EN	GP2_CLK_EN	FE_CLK_EN						
Type	RW	RW					RW	RW	RW	RW						
Reset	1	1					1	1	1	1						

Bit(s)	Name	Description
16	ESW_CLK_EN	**Ethernet switch clock control** 1: Enable clock 0: Disable clock
15	WOCPU0_CLK_EN	**WOCPU clock control** 1: Enable clock 0: Disable clock
14	WOCPU1_CLK_EN	**WOCPU clock control** 1: Enable clock 0: Disable clock
9	GP0_CLK_EN	**Giga port 0 clock control** 1: Enable clock 0: Disable clock
8	GP1_CLK_EN	**Giga port 1 clock control** 1: Enable clock 0: Disable clock
7	GP2_CLK_EN	**Giga port 2 clock control** 1: Enable clock 0: Disable clock
6	FE_CLK_EN	**Frame Engine clock control** 1: Enable clock 0: Disable clock

15000034 RSTCTL Reset Control Register 06000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE1_RST	PPE0_RST						RSV5	GMAC_RST							RSV2
Type	RW	RW						RW	RW							RW
Reset	0	0						0	0							0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PMTR_RST		FE_RST						
Type								RW		RW						
Reset								0		0						

Bit(s)	Name	Description
31	PPE1_RST	**PPE1 reset control** 1: Assert reset 0: De-assert reset
30	PPE0_RST	**PPE0 reset control** 1: Assert reset 0: De-assert reset
24	RSV5	**Reserved (EPHY reset control)** 1: Assert reset 0: De-assert reset
23	GMAC_RST	**GMAC reset control** 1: Assert reset 0: De-assert reset
16	RSV2	**Reserved (ETH switch reset control)** 1: Assert reset 0: De-assert reset
8	PMTR_RST	**PMTR reset control** 1: Assert reset 0: De-assert reset
6	FE_RST	**Frame Engine reset control** 1: Assert reset 0: De-assert reset

15000038 RSTSTAT Reset Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SWSYSRST		
Type														W1C		
Reset														0		

Bit(s)	Name	Description
2	SWSYSRST	**Software system reset occurred** This bit will be set if software resets the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect. NOTE: This register is reset only by a power-on reset. 0: Has no effect. 1: Clears this bit.

15000040 **GPIO0_MODE** **GPIO0 Purpose Selection** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO0_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO0_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPIO0_MODE	**Depend on SB_FIFO_SW_RD_EN.** If SB_FIFO_SW_RD_EN = 0: Reserved If SB_FIFO_SW_RD_EN = 1: Side band FIFO read LSB

15000044 GPIO1_MODE GPIO1 Purpose Selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO1_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO1_MODE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPIO1_MODE	**Depend on SB_FIFO_SW_RD_EN.** If SB_FIFO_SW_RD_EN = 0: Reserved If SB_FIFO_SW_RD_EN = 1: Side band FIFO read MSB

15000048 MEMO0 Memory0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO0	**Memory0**

1500004C **MEMO1** **Memory1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO1	**Memory1**

15000050 MEMO2 Memory2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO2	**Memory2 (utif_in debug read)**

15000054 MEMO3 Memory3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO3	**Memory3 (utif_out debug read)**

15000058 MEMO4 Memory4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31	MEMO4	**Memory4 (MCUSYS_DBG_SEL0)**

1500005C MEMO5 Memory5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MEMO5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MEMO5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MEMO5	**Memory5 (MCUSYS_DBG_SEL1)**

15000060 IOC_EN NETSYS IO Coherence Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GLOBAL_IOC_EN															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					WOCPU_IOC_EN	WED1_IOC_EN	WED0_IOC_EN	FDMA_IOC_EN	EDMA1_IOC_EN	EDMA0_IOC_EN	MDMA_IOC_EN	WDMA1_IOC_EN	WDMA0_IOC_EN	PPE1_IOC_EN	PPE0_IOC_EN	ADMA_IOC_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GLOBAL_IOC_EN	**Enable Global IOC** 0: Disable 1: Enable
11	WOCPU_IOC_EN	**Enable WOCPU IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
10	WED1_IOC_EN	**Enable WED1 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
9	WED0_IOC_EN	**Enable WED0 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
8	FDMA_IOC_EN	**Enable FDMA IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
7	EDMA1_IOC_EN	**Enable EDMA1 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable

Bit(s)	Name	Description
6	EDMA0_IOC_EN	**Enable EDMA0 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
5	MDMA_IOC_EN	**Enable MDMA IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
4	WDMA1_IOC_EN	**Enable WDMA1 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
3	WDMA0_IOC_EN	**Enable WDMA0 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
2	PPE1_IOC_EN	**Enable PPE1 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
1	PPE0_IOC_EN	**Enable PPE0 IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable
0	ADMA_IOC_EN	**Enable ADMA IOC** Only valid when GLOBAL_IOC_EN = 1 0: Disable 1: Enable

15000064 BIST_CTRL NETSYS Global BIST Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INFRA2NETSYS_NEAR_FULL															
Type	RO															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						NETSYS2INFRA_BIST_FAIL	NETSYS2INFRA_BIST_DONE	NETSYS2INFRA_BIST_EN		NETSYS2EMI_M1_BIST_FAIL	NETSYS2EMI_M1_BIST_DONE	NETSYS2EMI_M1_BIST_EN		NETSYS2EMI_M0_BIST_FAIL	NETSYS2EMI_M0_BIST_DONE	NETSYS2EMI_M0_BIST_EN
Type						RO	RO	RW		RO	RO	RW		RO	RO	RW
Reset						0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
31	INFRA2NETSYS_NEAR_FULL	**INFRA2NETSYS GALS read data FIFO near full flag**
10	NETSYS2INFRA_BIST_FAIL	**Asserted when NETSYS2INFRA BIST test fails.** Only valid when NETSYS2INFRA_BIST_DONE = 1
9	NETSYS2INFRA_BIST_DONE	**Asserted when NETSYS2INFRA BIST test finishes**
8	NETSYS2INFRA_BIST_EN	**Start NETSYS2INFRA BIST test** 0: Disable 1: Enable
6	NETSYS2EMI_M1_BIST_FAIL	**Asserted when NETSYS2EMI_M1 BIST test fails.** Only valid when NETSYS2EMI_M1_BIST_DONE = 1
5	NETSYS2EMI_M1_BIST_DONE	**Asserted when NETSYS2EMI_M1 BIST test finishes**
4	NETSYS2EMI_M1_BIST_EN	**Start NETSYS2EMI_M1 BIST test** 0: Disable 1: Enable
2	NETSYS2EMI_M0_BIST_FAIL	**Asserted when NETSYS2EMI_M0 BIST test fails.** Only valid when NETSYS2EMI_M0_BIST_DONE = 1
1	NETSYS2EMI_M0_BIST_DONE	**Asserted when NETSYS2EMI_M0 BIST test finishes**
0	NETSYS2EMI_M0_BIST_EN	**Start NETSYS2EMI_M0 BIST test** 0: Disable 1: Enable

15000068 BIST_NETSYS2EMI0 NETSYS2EMI_M0 BIST Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NETSYS2EMI_M0_AWULTRA_EN		NETSYS2EMI_M0_AWDOMAIN_EN	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M0_AWUSER_EN		NETSYS2EMI_M0_AWPROT_EN		NETSYS2EMI_M0_AWCACHE_EN		NETSYS2EMI_M0_AWBURST_EN		NETSYS2EMI_M0_AWSIZE_EN		NETSYS2EMI_M0_AWADDR_EN		NETSYS2EMI_M0_AWLEN_EN		NETSYS2EMI_M0_AWID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	NETSYS2EMI_M0_AWULTRA_EN	**Test NETSYS2EMI_M0 awultra signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
17:16	NETSYS2EMI_M0_AWDOMAIN_EN	**Test NETSYS2EMI_M0 awdomain signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
15:14	NETSYS2EMI_M0_AWUSER_EN	**Test NETSYS2EMI_M0 awuser signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
13:12	NETSYS2EMI_M0_AWPROT_EN	**Test NETSYS2EMI_M0 awprot signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
11:10	NETSYS2EMI_M0_AWCACHE_EN	**Test NETSYS2EMI_M0 awcache signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
9:8	NETSYS2EMI_M0_AWBURST_EN	**Test NETSYS2EMI_M0 awburst signal** 2'b00: Designed functional pattern enable 2'b01: INCR(01) enable

Bit(s)	Name	Description
		2'b10: WRAP(10) enable
		2'b11: FIXED(00) enable
7:6	NETSYS2EMI_M0_AWSIZE_EN	**Test NETSYS2EMI_M0 awsize signal**
		2'b00: Designed functional pattern enable
		2'b01: 7 enable
		2'b11: 0 enable
5:4	NETSYS2EMI_M0_AWADDR_EN	**Test NETSYS2EMI_M0 awaddr signal**
		2'b00: Designed functional pattern enable
		2'b01: 0xFFFFF800 enable
		2'b10: 0xFFFFFFFF enable
		2'b11: 0x00000000 enable
3:2	NETSYS2EMI_M0_AWLEN_EN	**Test NETSYS2EMI_M0 awlen signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable
1:0	NETSYS2EMI_M0_AWID_EN	**Test NETSYS2EMI_M0 awid signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable

1500006C BIST_NETSYS2EMI1 NETSYS2EMI_M0 BIST Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NETSYS2EMI_M0_RRESP_EN		NETSYS2EMI_M0_RDATA_EN		NETSYS2EMI_M0_BRESP_EN		NETSYS2EMI_M0_WSTRB_EN		NETSYS2EMI_M0_WDATA_EN		NETSYS2EMI_M0_ARULTRA_EN		NETSYS2EMI_M0_ARDOMAIN_EN	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M0_ARUSER_EN		NETSYS2EMI_M0_ARPROT_EN		NETSYS2EMI_M0_ARCACHE_EN		NETSYS2EMI_M0_ARBURST_EN		NETSYS2EMI_M0_ARSIZE_EN		NETSYS2EMI_M0_ARADDR_EN		NETSYS2EMI_M0_ARLEN_EN		NETSYS2EMI_M0_ARID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	NETSYS2EMI_M0_RRESP_EN	**Test NETSYS2EMI_M0 rresp signal** 2'b00: Designed functional pattern enable 2'b01: 11 enable 2'b11: 00 enable
27:26	NETSYS2EMI_M0_RDATA_EN	**Test NETSYS2EMI_M0 rdata signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable
25:24	NETSYS2EMI_M0_BRESP_EN	**Test NETSYS2EMI_M0 bresp signal** 2'b00: Designed functional pattern enable 2'b01: 11 enable 2'b11: 00 enable
23:22	NETSYS2EMI_M0_WSTRB_EN	**Test NETSYS2EMI_M0 wstrb signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable
21:20	NETSYS2EMI_M0_WDATA_EN	**Test NETSYS2EMI_M0 wdata signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable

Bit(s)	Name	Description
19:18	NETSYS2EMI_M0_ARULTRA_EN	**Test NETSYS2EMI_M0 arultra signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
17:16	NETSYS2EMI_M0_ARDOMAIN_EN	**Test NETSYS2EMI_M0 ardomain signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
15:14	NETSYS2EMI_M0_ARUSER_EN	**Test NETSYS2EMI_M0 aruser signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
13:12	NETSYS2EMI_M0_ARPROT_EN	**Test NETSYS2EMI_M0 arprot signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
11:10	NETSYS2EMI_M0_ARCACHE_EN	**Test NETSYS2EMI_M0 arcache signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
9:8	NETSYS2EMI_M0_ARBURST_EN	**Test NETSYS2EMI_M0 arburst signal** 2'b00: Designed functional pattern enable 2'b01: INCR(01) enable 2'b10: WRAP(10) enable 2'b11: FIXED(00) enable
7:6	NETSYS2EMI_M0_ARSIZE_EN	**Test NETSYS2EMI_M0 arsize signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
5:4	NETSYS2EMI_M0_ARADDR_EN	**Test NETSYS2EMI_M0 araddr signal** 2'b00: Designed functional pattern enable 2'b01: 0xFFFFF800 enable

Bit(s)	Name	Description
		2'b10: 0xFFFFFFFF enable
		2'b11: 0x00000000 enable
3:2	NETSYS2EMI_M0_ARLEN_EN	**Test NETSYS2EMI_M0 arlen signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable
1:0	NETSYS2EMI_M0_ARID_EN	**Test NETSYS2EMI_M0 arid signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable

15000070 BIST_NETSYS2EMI2 NETSYS2EMI_M1 BIST Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NETSYS2EMI_M1_AWULTRA_EN		NETSYS2EMI_M1_AWDOMAIN_EN	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M1_AWUSER_EN		NETSYS2EMI_M1_AWPROT_EN		NETSYS2EMI_M1_AWCACHE_EN		NETSYS2EMI_M1_AWBURST_EN		NETSYS2EMI_M1_AWSIZE_EN		NETSYS2EMI_M1_AWADDR_EN		NETSYS2EMI_M1_AWLEN_EN		NETSYS2EMI_M1_AWID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	NETSYS2EMI_M1_AWULTRA_EN	**Test NETSYS2EMI_M1 awultra signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
17:16	NETSYS2EMI_M1_AWDOMAIN_EN	**Test NETSYS2EMI_M1 awdomain signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
15:14	NETSYS2EMI_M1_AWUSER_EN	**Test NETSYS2EMI_M1 awuser signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
13:12	NETSYS2EMI_M1_AWPROT_EN	**Test NETSYS2EMI_M1 awprot signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
11:10	NETSYS2EMI_M1_AWCACHE_EN	**Test NETSYS2EMI_M1 awcache signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
9:8	NETSYS2EMI_M1_AWBURST_EN	**Test NETSYS2EMI_M1 awburst signal** 2'b00: Designed functional pattern enable 2'b01: INCR(01) enable

Bit(s)	Name	Description
		2'b10: WRAP(10) enable
		2'b11: FIXED(00) enable
7:6	NETSYS2EMI_M1_AWSIZE_EN	**Test NETSYS2EMI_M1 awsize signal**
		2'b00: Designed functional pattern enable
		2'b01: 7 enable
		2'b11: 0 enable
5:4	NETSYS2EMI_M1_AWADDR_EN	**Test NETSYS2EMI_M1 awaddr signal**
		2'b00: Designed functional pattern enable
		2'b01: 0xFFFFF800 enable
		2'b10: 0xFFFFFFFF enable
		2'b11: 0x00000000 enable
3:2	NETSYS2EMI_M1_AWLEN_EN	**Test NETSYS2EMI_M1 awlen signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable
1:0	NETSYS2EMI_M1_AWID_EN	**Test NETSYS2EMI_M1 awid signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable

15000074 BIST_NETSYS2EMI3 NETSYS2EMI_M1 BIST Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NETSYS2EMI_M1_RRESP_EN		NETSYS2EMI_M1_RDATA_EN		NETSYS2EMI_M1_BRESP_EN		NETSYS2EMI_M1_WSTRB_EN		NETSYS2EMI_M1_WDATA_EN		NETSYS2EMI_M1_ARULTRA_EN		NETSYS2EMI_M1_ARDOMAIN_EN	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2EMI_M1_ARUSER_EN		NETSYS2EMI_M1_ARPROT_EN		NETSYS2EMI_M1_ARCACHE_EN		NETSYS2EMI_M1_ARBURST_EN		NETSYS2EMI_M1_ARSIZE_EN		NETSYS2EMI_M1_ARADDR_EN		NETSYS2EMI_M1_ARLEN_EN		NETSYS2EMI_M1_ARID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	NETSYS2EMI_M1_RRESP_EN	**Test NETSYS2EMI_M1 rresp signal** 2'b00: Designed functional pattern enable 2'b01: 11 enable 2'b11: 00 enable
27:26	NETSYS2EMI_M1_RDATA_EN	**Test NETSYS2EMI_M1 rdata signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable
25:24	NETSYS2EMI_M1_BRESP_EN	**Test NETSYS2EMI_M1 bresp signal** 2'b00: Designed functional pattern enable 2'b01: 11 enable 2'b11: 00 enable
23:22	NETSYS2EMI_M1_WSTRB_EN	**Test NETSYS2EMI_M1 wstrb signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable
21:20	NETSYS2EMI_M1_WDATA_EN	**Test NETSYS2EMI_M1 wdata signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable

Bit(s)	Name	Description
19:18	NETSYS2EMI_M1_ARULTRA_EN	**Test NETSYS2EMI_M1 arultra signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
17:16	NETSYS2EMI_M1_ARDOMAIN_EN	**Test NETSYS2EMI_M1 ardomain signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
15:14	NETSYS2EMI_M1_ARUSER_EN	**Test NETSYS2EMI_M1 aruser signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
13:12	NETSYS2EMI_M1_ARPROT_EN	**Test NETSYS2EMI_M1 arprot signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
11:10	NETSYS2EMI_M1_ARCACHE_EN	**Test NETSYS2EMI_M1 arcache signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
9:8	NETSYS2EMI_M1_ARBURST_EN	**Test NETSYS2EMI_M1 arburst signal** 2'b00: Designed functional pattern enable 2'b01: INCR(01) enable 2'b10: WRAP(10) enable 2'b11: FIXED(00) enable
7:6	NETSYS2EMI_M1_ARSIZE_EN	**Test NETSYS2EMI_M1 arsize signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
5:4	NETSYS2EMI_M1_ARADDR_EN	**Test NETSYS2EMI_M1 araddr signal** 2'b00: Designed functional pattern enable 2'b01: 0xFFFFF800 enable

Bit(s)	Name	Description
		2'b10: 0xFFFFFFFF enable
		2'b11: 0x00000000 enable
3:2	NETSYS2EMI_M1_ARLEN_EN	**Test NETSYS2EMI_M1 arlen signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable
1:0	NETSYS2EMI_M1_ARID_EN	**Test NETSYS2EMI_M1 arid signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable

15000078 BIST_NETSYS2INFRA0 NETSYS2INFRA BIST Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													NETSYS2INFRA_AWULTRA_EN		NETSYS2INFRA_AWDOMAIN_EN	
Type													RW		RW	
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2INFRA_AWUSER_EN		NETSYS2INFRA_AWPROT_EN		NETSYS2INFRA_AWCACHE_EN		NETSYS2INFRA_AWBURST_EN		NETSYS2INFRA_AWSIZE_EN		NETSYS2INFRA_AWADDR_EN		NETSYS2INFRA_AWLEN_EN		NETSYS2INFRA_AWID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19:18	NETSYS2INFRA_AWULTRA_EN	**Test NETSYS2INFRA awultra signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
17:16	NETSYS2INFRA_AWDOMAIN_EN	**Test NETSYS2INFRA awdomain signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
15:14	NETSYS2INFRA_AWUSER_EN	**Test NETSYS2INFRA awuser signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
13:12	NETSYS2INFRA_AWPROT_EN	**Test NETSYS2INFRA awprot signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
11:10	NETSYS2INFRA_AWCACHE_EN	**Test NETSYS2INFRA awcache signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
9:8	NETSYS2INFRA_AWBURST_EN	**Test NETSYS2INFRA awburst signal** 2'b00: Designed functional pattern enable 2'b01: INCR(01) enable

Bit(s)	Name	Description
		2'b10: WRAP(10) enable
		2'b11: FIXED(00) enable
7:6	NETSYS2INFRA_AWSIZE_EN	**Test NETSYS2INFRA awsize signal**
		2'b00: Designed functional pattern enable
		2'b01: 7 enable
		2'b11: 0 enable
5:4	NETSYS2INFRA_AWADDR_EN	**Test NETSYS2INFRA awaddr signal**
		2'b00: Designed functional pattern enable
		2'b01: 0xFFFFF800 enable
		2'b10: 0xFFFFFFFF enable
		2'b11: 0x00000000 enable
3:2	NETSYS2INFRA_AWLEN_EN	**Test NETSYS2INFRA awlen signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable
1:0	NETSYS2INFRA_AWID_EN	**Test NETSYS2INFRA awid signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable

1500007C BIST_NETSYS2INFRA1 NETSYS2INFRA BIST Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			NETSYS2INFRA_RRESP_EN		NETSYS2INFRA_RDATA_EN		NETSYS2INFRA_BRESP_EN		NETSYS2INFRA_WSTRB_EN		NETSYS2INFRA_WDATA_EN		NETSYS2INFRA_ARULTRA_EN		NETSYS2INFRA_ARDOMAIN_EN	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS2INFRA_ARUSER_EN		NETSYS2INFRA_ARPROT_EN		NETSYS2INFRA_ARCACHE_EN		NETSYS2INFRA_ARBURST_EN		NETSYS2INFRA_ARSIZE_EN		NETSYS2INFRA_ARADDR_EN		NETSYS2INFRA_ARLEN_EN		NETSYS2INFRA_ARID_EN	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	NETSYS2INFRA_RRESP_EN	**Test NETSYS2INFRA rresp signal** 2'b00: Designed functional pattern enable 2'b01: 11 enable 2'b11: 00 enable
27:26	NETSYS2INFRA_RDATA_EN	**Test NETSYS2INFRA rdata signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable
25:24	NETSYS2INFRA_BRESP_EN	**Test NETSYS2INFRA bresp signal** 2'b00: Designed functional pattern enable 2'b01: 11 enable 2'b11: 00 enable
23:22	NETSYS2INFRA_WSTRB_EN	**Test NETSYS2INFRA wstrb signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable
21:20	NETSYS2INFRA_WDATA_EN	**Test NETSYS2INFRA wdata signal** 2'b00: 00-FF enable 2'b01: F enable 2'b10: 55-AA enable 2'b11: 0 enable

Bit(s)	Name	Description
19:18	NETSYS2INFRA_ARULTRA_EN	**Test NETSYS2INFRA arultra signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
17:16	NETSYS2INFRA_ARDOMAIN_EN	**Test NETSYS2INFRA ardomain signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
15:14	NETSYS2INFRA_ARUSER_EN	**Test NETSYS2INFRA aruser signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
13:12	NETSYS2INFRA_ARPROT_EN	**Test NETSYS2INFRA arprot signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
11:10	NETSYS2INFRA_ARCACHE_EN	**Test NETSYS2INFRA arcache signal** 2'b00: Designed functional pattern enable 2'b01: F enable 2'b11: 0 enable
9:8	NETSYS2INFRA_ARBURST_EN	**Test NETSYS2INFRA arburst signal** 2'b00: Designed functional pattern enable 2'b01: INCR(01) enable 2'b10: WRAP(10) enable 2'b11: FIXED(00) enable
7:6	NETSYS2INFRA_ARSIZE_EN	**Test NETSYS2INFRA arsize signal** 2'b00: Designed functional pattern enable 2'b01: 7 enable 2'b11: 0 enable
5:4	NETSYS2INFRA_ARADDR_EN	**Test NETSYS2INFRA araddr signal** 2'b00: Designed functional pattern enable 2'b01: 0xFFFFF800 enable

Bit(s)	Name	Description
		2'b10: 0xFFFFFFFF enable
		2'b11: 0x00000000 enable
3:2	NETSYS2INFRA_ARLEN_EN	**Test NETSYS2INFRA arlen signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable
1:0	NETSYS2INFRA_ARID_EN	**Test NETSYS2INFRA arid signal**
		2'b00: Designed functional pattern enable
		2'b01: F enable
		2'b11: 0 enable

15000080 AXICFG0 AXI Sideband Configuration Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_M_ARFLUSH		ADMA_M_ARULTRA		ADMA_M_ARDOMAIN				ADMA_M_AWFLUSH		ADMA_M_AWULTRA		ADMA_M_AWDOMAIN			
Type	RW		RW		RW				RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	ADMA_M_ARFLUSH	**ADMA arflush**
13:12	ADMA_M_ARULTRA	**ADMA arultra**
11:8	ADMA_M_ARDOMAIN	**ADMA ardomain**
7:6	ADMA_M_AWFLUSH	**ADMA awflush**
5:4	ADMA_M_AWULTRA	**ADMA awultra**
3:0	ADMA_M_AWDOMAIN	**ADMA awdomain**

15000084 AXICFG1 AXI Sideband Configuration Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE1_M_ARFLUSH		PPE1_M_ARULTRA		PPE1_M_ARDOMAIN				PPE1_M_AWFLUSH		PPE1_M_AWULTRA		PPE1_M_AWDOMAIN			
Type	RW		RW		RW				RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PPE0_M_ARFLUSH		PPE0_M_ARULTRA		PPE0_M_ARDOMAIN				PPE0_M_AWFLUSH		PPE0_M_AWULTRA		PPE0_M_AWDOMAIN			
Type	RW		RW		RW				RW		RW		RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	PPE1_M_ARFLUSH	**PPE1 arflush**
29:28	PPE1_M_ARULTRA	**PPE1 arultra**
27:24	PPE1_M_ARDOMAIN	**PPE1 ardomain**
23:22	PPE1_M_AWFLUSH	**PPE1 awflush**
21:20	PPE1_M_AWULTRA	**PPE1 awultra**
19:16	PPE1_M_AWDOMAIN	**PPE1 awdomain**
15:14	PPE0_M_ARFLUSH	**PPE0 arflush**
13:12	PPE0_M_ARULTRA	**PPE0 arultra**
11:8	PPE0_M_ARDOMAIN	**PPE0 ardomain**
7:6	PPE0_M_AWFLUSH	**PPE0 awflush**
5:4	PPE0_M_AWULTRA	**PPE0 awultra**
3:0	PPE0_M_AWDOMAIN	**PPE0 awdomain**

15000088 GALSCFG0 GALS Configuration Register 0 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		NETSYS2EMI_M1_IDLE_MASK						NETSYS2EMI_M1_SAMPLE_SEL	NETSYS2EMI_M1_SLV_SYNC_SEL		NETSYS2EMI_M1_MST_SYNC_SEL		NETSYS2EMI_M1_ARFLUSH_THRE		NETSYS2EMI_M1_AWFLUSH_THRE	
Type		RW						RW	RW		RW		RW		RW	
Reset		0	0	0				1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		NETSYS2EMI_M0_IDLE_MASK						NETSYS2EMI_M0_SAMPLE_SEL	NETSYS2EMI_M0_SLV_SYNC_SEL		NETSYS2EMI_M0_MST_SYNC_SEL		NETSYS2EMI_M0_ARFLUSH_THRE		NETSYS2EMI_M0_AWFLUSH_THRE	
Type		RW						RW	RW		RW		RW		RW	
Reset		0	0	0				1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30:28	NETSYS2EMI_M1_IDLE_MASK	**Idle signal mask** [2]: NETSYS2EMI_M1_BIST_idle [1]: NETSYS2EMI_M1_slpprot_idle [0]: NETSYS2EMI_M1_axi_idle
24	NETSYS2EMI_M1_SAMPLE_SEL	**NETSYS2EMI_M1 GALS select first step of sample clock edge of master & slaver synchronizer**
23:22	NETSYS2EMI_M1_SLV_SYNC_SEL	**NETSYS2EMI_M1 GALS slaver synchronizer step**
21:20	NETSYS2EMI_M1_MST_SYNC_SEL	**NETSYS2EMI_M1 GALS master synchronizer step**
19:18	NETSYS2EMI_M1_ARFLUSH_THRE	**NETSYS2EMI_M1 GALS read FIFO near full threshold**
17:16	NETSYS2EMI_M1_AWFLUSH_THRE	**NETSYS2EMI_M1 GALS write FIFO near full threshold**
14:12	NETSYS2EMI_M0_IDLE_MASK	**Idle signal mask** [2]: NETSYS2EMI_M0_BIST_idle [1]: NETSYS2EMI_M0_slpprot_idle [0]: NETSYS2EMI_M0_axi_idle
8	NETSYS2EMI_M0_SAMPLE_SEL	**NETSYS2EMI_M0 GALS select first step of sample clock edge of master & slaver synchronizer**
7:6	NETSYS2EMI_M0_SLV_SYNC_SEL	**NETSYS2EMI_M0 GALS slaver synchronizer step**
5:4	NETSYS2EMI_M0_MST_SYNC_SEL	**NETSYS2EMI_M0 GALS master synchronizer step**
3:2	NETSYS2EMI_M0_ARFLUSH_THRE	**NETSYS2EMI_M0 GALS read FIFO near full threshold**
1:0	NETSYS2EMI_M0_AWFLUSH_THRE	**NETSYS2EMI_M0 GALS write FIFO near full threshold**

1500008C GALSCFG1 GALS Configuration Register 1 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			INFRA2NETSYS_IDLE_MASK				INFRA2NETSYS_RFIFO_NEAR_FULL_EN	INFRA2NETSYS_SAMPLE_SEL	INFRA2NETSYS_SLV_SYNC_SEL		INFRA2NETSYS_MST_SYNC_SEL		INFRA2NETSYS_RFIFO_THRE			
Type			RW				RW	RW	RW		RW		RW			
Reset			0	0			0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		NETSYS2INFRA_IDLE_MASK						NETSYS2INFRA_SAMPLE_SEL	NETSYS2INFRA_SLV_SYNC_SEL		NETSYS2INFRA_MST_SYNC_SEL		NETSYS2INFRA_ARFLUSH_THRE		NETSYS2INFRA_AWFLUSH_THRE	
Type		RW						RW	RW		RW		RW		RW	
Reset		0	0	0				1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29:28	INFRA2NETSYS_IDLE_MASK	**Idle signal mask** [1]: INFRA2NETSYS_BIST_idle [0]: INFRA2NETSYS_slpprot_idle
25	INFRA2NETSYS_RFIFO_NEAR_FULL_EN	**Enable INFRA2NETSYS GALS read data FIFO near full control**
24	INFRA2NETSYS_SAMPLE_SEL	**INFRA2NETSYS GALS select first step of sample clock edge of master & slaver synchronizer**
23:22	INFRA2NETSYS_SLV_SYNC_SEL	**INFRA2NETSYS GALS slaver synchronizer step**
21:20	INFRA2NETSYS_MST_SYNC_SEL	**INFRA2NETSYS GALS master synchronizer step**
19:16	INFRA2NETSYS_RFIFO_THRE	**INFRA2NETSYS GALS read data FIFO near full threshold**
14:12	NETSYS2INFRA_IDLE_MASK	**Idle signal mask** [2]: NETSYS2INFRA_BIST_idle [1]: NETSYS2INFRA_slpprot_idle [0]: NETSYS2INFRA_axi_idle
8	NETSYS2INFRA_SAMPLE_SEL	**NETSYS2INFRA GALS select first step of sample clock edge of master & slaver synchronizer**
7:6	NETSYS2INFRA_SLV_SYNC_SEL	**NETSYS2INFRA GALS slaver synchronizer step**
5:4	NETSYS2INFRA_MST_SYNC_SEL	**NETSYS2INFRA GALS master synchronizer step**
3:2	NETSYS2INFRA_ARFLUSH_THRE	**NETSYS2INFRA GALS read FIFO near full threshold**
1:0	NETSYS2INFRA_AWFLUSH_THRE	**NETSYS2INFRA GALS write FIFO near full threshold**

15000090 MISTAT NETSYS Bus MI Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MAS_UP1_ERR_FLGA	MAS_UP0_ERR_FLGA		SLV_MI_LOCK_ERR_FLAG	SLV_MI_ERRMID_SET_RIRQ	SLV_MI_ERRMID_SET_BIRQ		MAS_MI1_LOCK_ERR_FLAG	MAS_MI1_ERRMID_SET_RIRQ	MAS_MI1_ERRMID_SET_BIRQ		MAS_MI0_LOCK_ERR_FLAG	MAS_MI0_ERRMID_SET_RIRQ	MAS_MI0_ERRMID_SET_BIRQ
Type			RO	RO		RO	RO	RO		RO	RO	RO		RO	RO	RO
Reset			0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
13	MAS_UP1_ERR_FLGA	**MAS_UP1 detects error**
12	MAS_UP0_ERR_FLGA	**MAS_UP0 detects error**
10	SLV_MI_LOCK_ERR_FLAG	**SLV_MI detects lock error**
9	SLV_MI_ERRMID_SET_RIRQ	**SLV_MI detects error MID from slave in R channel**
8	SLV_MI_ERRMID_SET_BIRQ	**SLV_MI detects error MID from slave in B channel**
6	MAS_MI1_LOCK_ERR_FLAG	**MAS_MI1 detects lock error**
5	MAS_MI1_ERRMID_SET_RIRQ	**MAS_MI1 detects error MID from slave in R channel**
4	MAS_MI1_ERRMID_SET_BIRQ	**MAS_MI1 detects error MID from slave in B channel**
2	MAS_MI0_LOCK_ERR_FLAG	**MAS_MI0 detects lock error**
1	MAS_MI0_ERRMID_SET_RIRQ	**MAS_MI0 detects error MID from slave in R channel**
0	MAS_MI0_ERRMID_SET_BIRQ	**MAS_MI0 detects error MID from slave in B channel**

15000094 SI0STAT0 NETSYS Bus SI Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_SI_VIO_ID												SLV_SI_VIO_WAY_EN			SLV_SI_VIO_WR
Type	RO												RO			RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_SI_VIO_RD	SLV_SI_VIO_DECERR	MAS_SI_VIO_ID								MAS_SI_VIO_WAY_EN			MAS_SI_VIO_WR	MAS_SI_VIO_RD	MAS_SI_VIO_DECERR
Type	RO	RO	RO								RO			RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SLV_SI_VIO_ID	**SLV_SI violation ID**
19:17	SLV_SI_VIO_WAY_EN	**SLV_SI violation way_en**
16	SLV_SI_VIO_WR	**SLV_SI violation write transaction**
15	SLV_SI_VIO_RD	**SLV_SI violation read transaction**
14	SLV_SI_VIO_DECERR	**SLV_SI violation decode error**
13:6	MAS_SI_VIO_ID	**MAS_SI violation ID**
5:3	MAS_SI_VIO_WAY_EN	**MAS_SI violation way_en**
2	MAS_SI_VIO_WR	**MAS_SI violation write transaction**
1	MAS_SI_VIO_RD	**MAS_SI violation read transaction**
0	MAS_SI_VIO_DECERR	**MAS_SI violation decode error**

15000098 SI0STAT1 NETSYS Bus SI Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAS_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAS_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAS_SI_VIO_ADDR	**MAS_SI violation address**

1500009C SI0STAT2 NETSYS Bus SI Status Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_SI_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SLV_SI_VIO_ADDR	**SLV_SI violation address**

150000A0 **S2PSTAT0** **NETSYS Bus S2P Status Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_S2P_VIO_ID															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_S2P_VIO_DOMAIN				SLV_S2P_VIO_WAY_EN								SLV_S2P_VIO_WR	SLV_S2P_VIO_RD	SLV_S2P_VIO_DECERR	SLV_S2P_VIO_ADDR_unaligned
Type	RO				RO								RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	SLV_S2P_VIO_ID	**SLV_S2P violation ID**
15:12	SLV_S2P_VIO_DOMAIN	**SLV_S2P violation domain**
11:4	SLV_S2P_VIO_WAY_EN	**SLV_S2P violation way_en**
3	SLV_S2P_VIO_WR	**SLV_S2P violation write transaction**
2	SLV_S2P_VIO_RD	**SLV_S2P violation read transaction**
1	SLV_S2P_VIO_DECERR	**SLV_S2P violation decode error**
0	SLV_S2P_VIO_ADDR_unaligned	**SLV_S2P violation unaligned address**

150000A4 **S2PSTAT1** **NETSYS Bus S2P Status Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_S2P_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_S2P_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SLV_S2P_VIO_ADDR	**SLV_S2P violation address**

150000A8 X2SSTAT0 NETSYS Bus X2S Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						SLV_X2S_VIO_ID										
Type						RO										
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_X2S_VIO_ID				SLV_X2S_VIO_WR	SLV_X2S_VIO_RD									SLV_X2S_VIO_DECERR	SLV_X2S_VIO_ADDR_unaligned
Type	RO				RO	RO									RO	RO
Reset	0	0	0	0	0	0									0	0

Bit(s)	Name	Description
26:12	SLV_X2S_VIO_ID	**SLV_X2S violation ID**
11	SLV_X2S_VIO_WR	**SLV_X2S violation write transaction**
10	SLV_X2S_VIO_RD	**SLV_X2S violation read transaction**
1	SLV_X2S_VIO_DECERR	**SLV_X2S violation decode error**
0	SLV_X2S_VIO_ADDR_unaligned	**SLV_X2S violation unaligned address**

150000AC **X2SSTAT1** **NETSYS Bus X2S Status Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SLV_X2S_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SLV_X2S_VIO_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SLV_X2S_VIO_ADDR	**SLV_X2S violation address**

150000B0 **R2XCFG0** **R2X Configuration Register 0** **000F00FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		R2X_MST_SEL							R2X_INT_B							
Type		RW							RO							
Reset		0	0	0					0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									R2X_INT_EN							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
30:28	R2X_MST_SEL	**R2X channel debug information select** 0: NETSYS ADMA 1: NETSYS PPE0 2: NETSYS PPE1
23:16	R2X_INT_B	**R2X interrupt status** R2X wrapper interrupt will set 1'b1 when receive len = 0 cmd from rbus master. [0]: NETSYS ADMA [1]: NETSYS PPE0 [2]: NETSYS PPE1 Others: Reserved
7:0	R2X_INT_EN	**Enable R2X Interrupt** Enable R2X wrapper interrupt when receive len = 0 cmd from rbus master. 0: Disable 1: Enable

150000B4 **R2XCFG1** **R2X Configuration Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_DBG_SEL_7				R2X_DBG_SEL_6				R2X_DBG_SEL_5				R2X_DBG_SEL_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_DBG_SEL_3				R2X_DBG_SEL_2				R2X_DBG_SEL_1				R2X_DBG_SEL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	R2X_DBG_SEL_7	**Select debug information from R2X (Reserved)**
27:24	R2X_DBG_SEL_6	**Select debug information from R2X (Reserved)**
23:20	R2X_DBG_SEL_5	**Select debug information from R2X (Reserved)**
19:16	R2X_DBG_SEL_4	**Select debug information from R2X (Reserved)**
15:12	R2X_DBG_SEL_3	**Select debug information from R2X (Reserved)**
11:8	R2X_DBG_SEL_2	**Select debug information from R2X (NETSYS PPE1)**
7:4	R2X_DBG_SEL_1	**Select debug information from R2X (NETSYS PPE0)**
3:0	R2X_DBG_SEL_0	**Select debug information from R2X (NETSYS ADMA)** 0: R2X interrupt status 1: R2X interrupt enable and Rbus status 2: Rbus address 3: AXI status 4: AXI write address 5: AXI read address 6: Internal buffer handshake 7: Coherence sequence and Coherence length 8: Coherence compare address

150000B8 **R2XSTAT0** **R2X Status Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_INT_STATUS	**Record the address when receive len = 0 cmd from R2X selected channel according to R2XCFG0[30:28]**

150000BC **R2XSTAT1** **R2X Status Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_DBG_INFO	**Record debug information from R2X selected channel according to R2XCFG0[30:28]**

150000C0 APBCFG NETSYS_APB Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																NETSYS_APB_INT_CLR
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS_APB_ERR_CNT						NETSYS_APB_INT_CNT									
Type	RO						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	NETSYS_APB_INT_CLR	**NETSYS_APB interrupt clear** Write 1 to clear this interrupt.
15:10	NETSYS_APB_ERR_CNT	**NETSYS_APB error counter**
9:0	NETSYS_APB_INT_CNT	**NETSYS_APB interrupt countdown timer** Sets a delay timer that begins counting down when an error is detected. When the timer reaches zero the interrupt is then triggered. 10'b0000000000: Disable NETSYS_APB monitoring 10'b0000000001: 20 us 10'b0000000010: 40 us 10'b1000000000: 40 ms

150000C4 APBSTAT NETSYS_APB Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	NETSYS_APB_ERR_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NETSYS_APB_ERR_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	NETSYS_APB_ERR_ADDR	**NETSYS_APB address record for previous error found**

5.2 Frame Engine

5.2.1 Register Definition

Module name: FE Base address: (+0x15100000)

Address	Name	Width	Register Function
15100000	FE_GLO_CFG	32	Frame Engine Global Configuration
15100004	FE_RST_GLO	32	Frame Engine Global Reset
15100008	FE_INT_STATUS	32	Frame Engine Interrupt Status
1510000C	FE_INT_ENABLE	32	Frame Engine Interrupt Enable
15100010	FE_FOE_TS_T	32	Frame Engine Time Stamp
15100014	FE_IPV6_EXT	32	Frame Engine IPv6 Extension Header
15100018	FE_RATE_COMP	32	Frame Engine Rate Limit Compensation
15100020	FE_INT_GRP	32	Frame Engine Interrupt Group
15100024	FE_GLO_CFG2	32	Frame Engine Global Configuration Part2
15100028	FE_INT_STATUS2	32	Frame Engine Interrupt Status Part2
1510002C	FE_INT_ENABLE2	32	Frame Engine Interrupt Enable Part2
15100100	PSE_FQFC_CFG1	32	PSE Free Queue Flow Control Part1
15100104	PSE_FQFC_CFG2	32	PSE Free Queue Flow Control Part2
15100110	PSE_PPE0_DROP	32	PPE0 Drop Packet Enable Port
15100114	PSE_PPE1_DROP	32	PPE1 Drop Packet Enable Port
15100130	FE_GDM_RXID1	32	FE GDM RXID Control 1
15100134	FE_GDM_RXID2	32	FE GDM RXID Control 2
15100140	PSE_IQ_REV1	32	PSE Input Queue Reservation Part1
15100144	PSE_IQ_REV2	32	PSE Input Queue Reservation Part2
15100148	PSE_IQ_REV3	32	PSE Input Queue Reservation Part3
1510014C	PSE_IQ_REV4	32	PSE Input Queue Reservation Part4
15100150	PSE_IQ_REV5	32	PSE Input Queue Reservation Part5
15100154	PSE_IQ_REV6	32	PSE Input Queue Reservation Part6
15100158	PSE_IQ_REV7	32	PSE Input Queue Reservation Part7
1510015C	PSE_IQ_REV8	32	PSE Input Queue Reservation Part8
15100160	PSE_OQ_TH1	32	PSE Output Queue Threshold Part1
15100164	PSE_OQ_TH2	32	PSE Output Queue Threshold Part2
15100168	PSE_OQ_TH3	32	PSE Output Queue Threshold Part3
1510016C	PSE_OQ_TH4	32	PSE Output Queue Threshold Part4
15100170	PSE_OQ_TH5	32	PSE Output Queue Threshold Part5
15100174	PSE_OQ_TH6	32	PSE Output Queue Threshold Part6
15100178	PSE_OQ_TH7	32	PSE Output Queue Threshold Part7
1510017C	PSE_OQ_TH8	32	PSE Output Queue Threshold Part8
15100180	PSE_IQ_STA1	32	PSE Input Queue Status Part1
15100184	PSE_IQ_STA2	32	PSE Input Queue Status Part2
15100188	PSE_IQ_STA3	32	PSE Input Queue Status Part3
1510018C	PSE_IQ_STA4	32	PSE Input Queue Status Part4
15100190	PSE_IQ_STA5	32	PSE Input Queue Status Part5
15100194	PSE_IQ_STA6	32	PSE Input Queue Status Part6
15100198	PSE_IQ_STA7	32	PSE Input Queue Status Part7
1510019C	PSE_IQ_STA8	32	PSE Input Queue Status Part8
151001A0	PSE_OQ_STA1	32	PSE Output Queue Status Part1
151001A4	PSE_OQ_STA2	32	PSE Output Queue Status Part2
151001A8	PSE_OQ_STA3	32	PSE Output Queue Status Part3
151001AC	PSE_OQ_STA4	32	PSE Output Queue Status Part4
151001B0	PSE_OQ_STA5	32	PSE Output Queue Status Part5
151001B4	PSE_OQ_STA6	32	PSE Output Queue Status Part6
151001B8	PSE_OQ_STA7	32	PSE Output Queue Status Part7
151001BC	PSE_OQ_STA8	32	PSE Output Queue Status Part8

Address	Name	Width	Register Function
151001C0	PSE_TDM_TBL0	32	PSE TDM Arbiter Table0
151001C4	PSE_TDM_TBL1	32	PSE TDM Arbiter Table1
151001C8	PSE_TDM_TBL2	32	PSE TDM Arbiter Table2
151001CC	PSE_TDM_TBL3	32	PSE TDM Arbiter Table3
151001D0	PSE_TDM_TBL4	32	PSE TDM Arbiter Table4
151001D4	PSE_TDM_TBL5	32	PSE TDM Arbiter Table5
151001D8	PSE_TDM_TBL6	32	PSE TDM Arbiter Table6
151001DC	PSE_TDM_TBL7	32	PSE TDM Arbiter Table7
151001E0	PSE_SP_CFG0	32	PSE Strict Priority Configure0
151001E4	PSE_SP_CFG1	32	PSE Strict Priority Configure1
151001E8	PSE_TDM_CFG	32	PSE TDM arbiter configure
15100200	FE_CDM1_DBG1	32	FE CDM1 Debug Part1
15100204	FE_CDM1_DBG2	32	FE CDM1 Debug Part2
15100208	FE_CDM2_DBG1	32	FE CDM2 Debug Part1
1510020C	FE_CDM2_DBG2	32	FE CDM2 Debug Part2
15100210	FE_GDM1_DBG1	32	FE GDM1 Debug Part1
15100214	FE_GDM1_DBG2	32	FE GDM1 Debug Part2
15100218	FE_GDM2_DBG1	32	FE GDM2 Debug Part1
1510021C	FE_GDM2_DBG2	32	FE GDM2 Debug Part2
15100220	FE_CDM1_FSM	32	FE CDM1 FSM Status
15100224	FE_CDM2_FSM	32	FE CDM2 FSM Status
15100228	FE_GDM1_FSM	32	FE GDM1 FSM Status
1510022C	FE_GDM2_FSM	32	FE GDM2 FSM Status
15100230	FE_CDM3_DBG1	32	FE CDM3 Debug Part1
15100234	FE_CDM3_DBG2	32	FE CDM3 Debug Part2
15100238	FE_CDM3_FSM	32	FE CDM3 FSM Status
15100240	FE_PSE_FREE	32	PSE Free Page Count
15100244	FE_DROP_FQ	32	FE Packet Drop by Free Queue
15100248	FE_DROP_FC	32	FE Packet Drop by Flow Control
1510024C	FE_DROP_PPE1	32	FE Packet Drop by PPE1
15100250	FE_DROP_PD_6	32	FE Packet Drop by Port 6 Disabled
15100254	FE_DROP_PD_5	32	FE Packet Drop by Port 5 Disabled
15100258	FE_DROP_PD_4	32	FE Packet Drop by Port 4 Disabled
1510025C	FE_DROP_PD_3	32	FE Packet Drop by Port 3 Disabled
15100260	FE_DROP_PD_2	32	FE Packet Drop by Port 2 Disabled
15100264	FE_DROP_PD_1	32	FE Packet Drop by Port 1 Disabled
15100268	FE_DROP_PD_0	32	FE Packet Drop by Port 0 Disabled
15100270	FE_DROP_PD_14	32	FE Packet Drop by Port 14 Disabled
15100274	FE_DROP_PD_13	32	FE Packet Drop by Port 13 Disabled
15100278	FE_DROP_PD_12	32	FE Packet Drop by Port 12 Disabled
1510027C	FE_DROP_PD_11	32	FE Packet Drop by Port 11 Disabled
15100280	FE_DROP_PD_10	32	FE Packet Drop by Port 10 Disabled
15100284	FE_DROP_PD_9	32	FE Packet Drop by Port 9 Disabled
15100288	FE_DROP_PD_8	32	FE Packet Drop by Port 8 Disabled
1510028C	FE_DROP_PD_7	32	FE Packet Drop by Port 7 Disabled
15100290	FE_CDM4_DBG1	32	FE CDM4 Debug Part1
15100294	FE_CDM4_DBG2	32	FE CDM4 Debug Part2
15100298	FE_CDM4_FSM	32	FE CDM4 FSM Status
151002A0	FE_DROP_PPE0	32	FE Packet Drop by PPE0
151002A4	FE_DROP_PPE0_P0_R01	32	FE Packet To Port0 Ring 0&1 Drop by PPE0
151002A8	FE_DROP_PPE0_P0_R23	32	FE Packet To Port0 Ring 2&3 Drop by PPE0
151002AC	FE_DROP_PPE0_P5	32	FE Packet To Port5 Drop by PPE0
151002B0	FE_DROP_PPE0_P8	32	FE Packet To Port8 Drop by PPE0
151002B4	FE_DROP_PPE0_P9	32	FE Packet To Port9 Drop by PPE0
151002B8	FE_DROP_PPE0_P10	32	FE Packet To Port10 Drop by PPE0
151002BC	FE_DROP_PPE0_P11	32	FE Packet To Port11 Drop by PPE0

Address	Name	Width	Register Function
151002C0	FE_DROP_PPE0_P12	32	FE Packet To Port12 Drop by PPE0
151002C4	FE_DROP_PPE1_P0_R01	32	FE Packet To Port0 Ring 0&1 Drop by PPE1
151002C8	FE_DROP_PPE1_P0_R23	32	FE Packet To Port0 Ring 2&3 Drop by PPE1
151002CC	FE_DROP_PPE1_P5	32	FE Packet To Port5 Drop by PPE1
151002D0	FE_DROP_PPE1_P8	32	FE Packet To Port8 Drop by PPE1
151002D4	FE_DROP_PPE1_P9	32	FE Packet To Port9 Drop by PPE1
151002D8	FE_DROP_PPE1_P10	32	FE Packet To Port10 Drop by PPE1
151002DC	FE_DROP_PPE1_P11	32	FE Packet To Port11 Drop by PPE1
151002E0	FE_DROP_PPE1_P12	32	FE Packet To Port12 Drop by PPE1
15100310	FE_CDM5_DBG1	32	FE CDM5 Debug Part1
15100314	FE_CDM5_DBG2	32	FE CDM5 Debug Part2
15100318	FE_CDM5_FSM	32	FE CDM5 FSM Status
15100320	FE_CDM6_DBG1	32	FE CDM6 Debug Part1
15100324	FE_CDM6_DBG2	32	FE CDM6 Debug Part2
15100328	FE_CDM6_FSM	32	FE CDM6 FSM Status
15100330	FE_CDM7_DBG1	32	FE CDM7 Debug Part1
15100334	FE_CDM7_DBG2	32	FE CDM7 Debug Part2
15100338	FE_CDM7_FSM	32	FE CDM7 FSM Status
15100400	CDMP_IG_CTRL	32	CDM Ingress Control
15100404	CDMP_EG_CTRL	32	CDM Egress Control
15100408	CDMP_PPE_GEN	32	CDM PPPoE Generation
15100500	GDM1_IG_CTRL	32	GDM Ingress Control
15100504	GDM1_EG_CTRL	32	GDM Egress Control
15100508	GDM1_MAC_LSB	32	GDM MY_MAC Address LSB
1510050C	GDM1_MAC_MSB	32	GDM MY_MAC Address MSB
15100510	GDM1_VLAN_GEN	32	GDM VLAN Generation
15100520	GDM1_DOS_CFG_0	32	GDM DOS Configuration 0
15100524	GDM1_DOS_CFG_1	32	GDM DOS Configuration 1
15100528	GDM1_DOS_CFG_2	32	GDM DOS Configuration 2
1510052C	GDM1_DOS_CFG_3	32	GDM DOS Configuration 3
15100C00	PFC_CFG_0	32	PFC GMAC1 Input Priority ReMap 0
15100C04	PFC_CFG_1	32	PFC GMAC1 Input Priority ReMap 1
15100C08	PFC_CFG_2	32	PFC GMAC2 Input Priority ReMap 0
15100C0C	PFC_CFG_3	32	PFC GMAC2 Input Priority ReMap 1
15100C10	PFC_CFG_4	32	PFC WDMA0_1 Input Priority ReMap 0
15100C60	PFC_CFG_5	32	PFC QDMA Input Priority ReMap 0
15100C64	PFC_CFG_6	32	PFC QDMA Input Priority ReMap 1
15100C68	PFC_CFG_7	32	PFC QDMA Input Priority ReMap 2
15100C6C	PFC_CFG_8	32	PFC QDMA Input Priority ReMap 3
15100C70	PFC_CFG_9	32	PFC QDMA Input Priority ReMap 4
15100C74	PFC_CFG_10	32	PFC QDMA Input Priority ReMap 5
15100C78	PFC_CFG_11	32	PFC QDMA Input Priority ReMap 6
15100C7C	PFC_CFG_12	32	PFC QDMA Input Priority ReMap 7
15100C80	PFC_CFG_13	32	PFC QDMA Input Priority ReMap 8
15100C84	PFC_CFG_14	32	PFC QDMA Input Priority ReMap 9
15100C88	PFC_CFG_15	32	PFC QDMA Input Priority ReMap 10
15100C8C	PFC_CFG_16	32	PFC QDMA Input Priority ReMap 11
15100C90	PFC_CFG_17	32	PFC QDMA Input Priority ReMap 12
15100C94	PFC_CFG_18	32	PFC QDMA Input Priority ReMap 13
15100C98	PFC_CFG_19	32	PFC QDMA Input Priority ReMap 14
15100C9C	PFC_CFG_20	32	PFC QDMA Input Priority ReMap 15
15100CA0	PFC_CFG_21	32	PFC QDMA Input Priority ReMap 16
15100CA4	PFC_CFG_22	32	PFC QDMA Input Priority ReMap 17
15100CA8	PFC_CFG_23	32	PFC QDMA Input Priority ReMap 18
15100CAC	PFC_CFG_24	32	PFC QDMA Input Priority ReMap 19
15100CB0	PFC_CFG_25	32	PFC QDMA Input Priority ReMap 20

Address	Name	Width	Register Function
15100CB4	PFC_CFG_26	32	PFC QDMA Input Priority ReMap 21
15100CB8	PFC_CFG_27	32	PFC QDMA Input Priority ReMap 22
15100CBC	PFC_CFG_28	32	PFC QDMA Input Priority ReMap 23
15100CC0	PFC_CFG_29	32	PFC QDMA Input Priority ReMap 24
15100CC4	PFC_CFG_30	32	PFC QDMA Input Priority ReMap 25
15100CC8	PFC_CFG_31	32	PFC QDMA Input Priority ReMap 26
15100CCC	PFC_CFG_32	32	PFC QDMA Input Priority ReMap 27
15100CD0	PFC_CFG_33	32	PFC QDMA Input Priority ReMap 28
15100CD4	PFC_CFG_34	32	PFC QDMA Input Priority ReMap 29
15100CD8	PFC_CFG_35	32	PFC QDMA Input Priority ReMap 30
15100CDC	PFC_CFG_36	32	PFC QDMA Input Priority ReMap 31
15100D60	PFC_CFG_37	32	PFC GMAC1 Output Priority ReMap 0
15100D64	PFC_CFG_38	32	PFC GMAC1 Output Priority ReMap 1
15100D68	PFC_CFG_39	32	PFC GMAC2 Output Priority ReMap 0
15100D6C	PFC_CFG_40	32	PFC GMAC2 Output Priority ReMap 1
15100D70	PFC_CFG_41	32	PFC WDMA0 Output Priority ReMap 0
15100D74	PFC_CFG_42	32	PFC WDMA1 Output Priority ReMap 0
15100DA0	PFC_CFG_43	32	PFC QDMA Output Priority ReMap 0
15100DA4	PFC_CFG_44	32	PFC QDMA Output Priority ReMap 1
15100DA8	PFC_CFG_45	32	PFC QDMA Output Priority ReMap 2
15100DAC	PFC_CFG_46	32	PFC QDMA Output Priority ReMap 3
15100DB0	PFC_CFG_47	32	PFC QDMA Output Priority ReMap 4
15100DB4	PFC_CFG_48	32	PFC QDMA Output Priority ReMap 5
15100DB8	PFC_CFG_49	32	PFC QDMA Output Priority ReMap 6
15100DBC	PFC_CFG_50	32	PFC QDMA Output Priority ReMap 7
15100DC0	PFC_CFG_51	32	PFC QDMA Output Priority ReMap 8
15100DC4	PFC_CFG_52	32	PFC QDMA Output Priority ReMap 9
15100DC8	PFC_CFG_53	32	PFC QDMA Output Priority ReMap 10
15100DCC	PFC_CFG_54	32	PFC QDMA Output Priority ReMap 11
15100DD0	PFC_CFG_55	32	PFC QDMA Output Priority ReMap 12
15100DD4	PFC_CFG_56	32	PFC QDMA Output Priority ReMap 13
15100DD8	PFC_CFG_57	32	PFC QDMA Output Priority ReMap 14
15100DDC	PFC_CFG_58	32	PFC QDMA Output Priority ReMap 15
15100DE0	PFC_CFG_59	32	PFC QDMA Output Priority ReMap 16
15100DE4	PFC_CFG_60	32	PFC QDMA Output Priority ReMap 17
15100DE8	PFC_CFG_61	32	PFC QDMA Output Priority ReMap 18
15100DEC	PFC_CFG_62	32	PFC QDMA Output Priority ReMap 19
15100DF0	PFC_CFG_63	32	PFC QDMA Output Priority ReMap 20
15100DF4	PFC_CFG_64	32	PFC QDMA Output Priority ReMap 21
15100DF8	PFC_CFG_65	32	PFC QDMA Output Priority ReMap 22
15100DFC	PFC_CFG_66	32	PFC QDMA Output Priority ReMap 23
15100E00	PFC_CFG_67	32	PFC QDMA Output Priority ReMap 24
15100E04	PFC_CFG_68	32	PFC QDMA Output Priority ReMap 25
15100E08	PFC_CFG_69	32	PFC QDMA Output Priority ReMap 26
15100E0C	PFC_CFG_70	32	PFC QDMA Output Priority ReMap 27
15100E10	PFC_CFG_71	32	PFC QDMA Output Priority ReMap 28
15100E14	PFC_CFG_72	32	PFC QDMA Output Priority ReMap 29
15100E18	PFC_CFG_73	32	PFC QDMA Output Priority ReMap 30
15100E1C	PFC_CFG_74	32	PFC QDMA Output Priority ReMap 31
15100EA0	PFC_CFG_75	32	PFC Enable Control to GMAC1
15100EA4	PFC_CFG_76	32	PFC Enable Control to GMAC1
15100EA8	PFC_CFG_77	32	PFC Enable Control to GMAC2
15100EAC	PFC_CFG_78	32	PFC Enable Control to GMAC2
15100EB0	PFC_CFG_79	32	PFC Enable Control to WDMA0
15100EB4	PFC_CFG_80	32	PFC Enable Control to WDMA0
15100EB8	PFC_CFG_81	32	PFC Enable Control to WDMA1

Address	Name	Width	Register Function
15100EBC	PFC_CFG_82	32	PFC Enable Control to WDMA1
15100EC0	PFC_CFG_83	32	PFC Enable Control to QDMA
15100EF0	PFC_CFG_85	32	PFC Debug 0
15100EF4	PFC_CFG_86	32	PFC Debug 1
15100EF8	PFC_CFG_87	32	PFC Debug 2
15100EFC	PFC_CFG_88	32	PFC Debug 3
15100F00	PFC_CFG_89	32	PFC Debug 4
15100F04	PFC_CFG_90	32	PFC Configuration
15101400	CDMQ_IG_CTRL	32	CDM VLAN Control
15101404	CDMQ_EG_CTRL	32	CDM Egress Control
15101408	CDMQ_PPP_GEN	32	CDM PPPoE Generation
15101500	GDM2_IG_CTRL	32	GDM Ingress Control
15101504	GDM2_EG_CTRL	32	GDM Egress Control
15101508	GDM2_MAC_LSB	32	GDM MY_MAC Address LSB
1510150C	GDM2_MAC_MSB	32	GDM MY_MAC Address MSB
15101510	GDM2_VLAN_GEN	32	GDM VLAN Generation
15101514	GDM2_FILTER_CRTL	32	GDM Filter Control
15101518	GDM2_VIDF01	32	GDM VID Filter Control 01
1510151C	GDM2_VIDF23	32	GDM VID Filter Control 23
15101520	GDM2_DOS_CFG_0	32	GDM DOS Configuration 0
15101524	GDM2_DOS_CFG_1	32	GDM DOS Configuration 1
15101528	GDM2_DOS_CFG_2	32	GDM DOS Configuration 2
1510152C	GDM2_DOS_CFG_3	32	GDM DOS Configuration 3
15101530	GDM2_THRES	32	GDM2 Threshold
15101600	CDMW0_IG_CTRL	32	CDM VLAN Control
15101604	CDMW0_EG_CTRL	32	CDM Egress Control
15101608	CDMW0_PPP_GEN	32	CDM PPPoE Generation
15101610	CDMW1_IG_CTRL	32	CDM VLAN Control
15101614	CDMW1_EG_CTRL	32	CDM Egress Control
15101618	CDMW1_PPP_GEN	32	CDM PPPoE Generation
15101620	CDME0_IG_CTRL	32	CDM VLAN Control
15101624	CDME0_EG_CTRL	32	CDM Egress Control
15101628	CDME0_PPP_GEN	32	CDM PPPoE Generation
15101630	CDME1_IG_CTRL	32	CDM VLAN Control
15101634	CDME1_EG_CTRL	32	CDM Egress Control
15101638	CDME1_PPP_GEN	32	CDM PPPoE Generation
15101640	CDMM_IG_CTRL	32	CDM VLAN Control
15101644	CDMM_EG_CTRL	32	CDM Egress Control
15101648	CDMM_PPP_GEN	32	CDM PPPoE Generation
1510164C	CDM_THRES0	32	CDM Threshold 0
15101650	CDM_THRES1	32	CDM Threshold 1
15101654	CDM_THRES2	32	CDM Threshold 2
15101658	CDM_THRES3	32	CDM Threshold 3
1510165C	CDM_THRES4	32	CDM Threshold 4
15102800	RSS_GLO_CFG	32	RSS Global Configuration
15102820	RSS_HASH_KEY_DW0	32	RSS Hash Key DW0
15102824	RSS_HASH_KEY_DW1	32	RSS Hash Key DW1
15102828	RSS_HASH_KEY_DW2	32	RSS Hash Key DW2
1510282C	RSS_HASH_KEY_DW3	32	RSS Hash Key DW3
15102830	RSS_HASH_KEY_DW4	32	RSS Hash Key DW4
15102834	RSS_HASH_KEY_DW5	32	RSS Hash Key DW5
15102838	RSS_HASH_KEY_DW6	32	RSS Hash Key DW6
1510283C	RSS_HASH_KEY_DW7	32	RSS Hash Key DW7
15102840	RSS_HASH_KEY_DW8	32	RSS Hash Key DW8
15102844	RSS_HASH_KEY_DW9	32	RSS Hash Key DW9
15102848	RSS_LFB_CFG0	32	RSS Low Flow Balance Configuration 0

Address	Name	Width	Register Function
15102850	RSS_INDR_TABLE_DW0	32	RSS Indirection Table DW0
15102854	RSS_INDR_TABLE_DW1	32	RSS Indirection Table DW1
15102858	RSS_INDR_TABLE_DW2	32	RSS Indirection Table DW2
1510285C	RSS_INDR_TABLE_DW3	32	RSS Indirection Table DW3
15102860	RSS_INDR_TABLE_DW4	32	RSS Indirection Table DW4
15102864	RSS_INDR_TABLE_DW5	32	RSS Indirection Table DW5
15102868	RSS_INDR_TABLE_DW6	32	RSS Indirection Table DW6
1510286C	RSS_INDR_TABLE_DW7	32	RSS Indirection Table DW7

15100000 FE_GLO_CFG Frame Engine Global Configuration 810000B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EXT_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LINK_DWN_0								L2_SPACE				INF_SPACE			
Type	RW								RW				RW			
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:16	EXT_TPID	**Extended VLAN TPID** User-defined TPID except for 0x8100, 0x88a8. [Note] This TPID field is used by CDM/GDM RX direction.
15:8	LINK_DWN_0	**Disable PSE Port 0~7** When PSE port is not valid on the Frame Engine, it is suggested to disable the corresponding port.
7:4	L2_SPACE	**L2 space** The space unit is 8 bytes.
3:0	INF_SPACE	**PKT_INFO space** The space unit is 8 bytes. [Note 1] Per received packet has already occupied 8 bytes (1 unit) by default. The actual PKT_INFO space is equal to (INF_SPACE + 1) [Note 2] (L2_SPACE + INF_SPACE + 1) <= 0xF

15100004 FE_RST_GLO Frame Engine Global Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0													PSE_RAM	PSE_MEM_EN	PSE_RESET
Type	RO													RW	RW	W1S
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:3	RESV0	**Reserved**
2	PSE_RAM	**PSE accessible RAM mode** [Note 1] When this bit is reset, PSE packet memory is only accessible by Pbus (0xA000~0xDFFF). [Note 2] When this bit is set, PSE packet memory is only accessible by Pbus (0x8000~0xDFFF) 0: Only 8KB PSE memory is left for iNIC initialization. 1: Make the whole PSE memory be used for Pbus access
1	PSE_MEM_EN	**Enable PSE access** 0: Disable 1: Enable PSE memory is accessible by PBUs
0	PSE_RESET	**PSE soft reset (self-cleared)** [Note] Whenever SW sets this bit, PSE will be initialized again and enter the normal mode. 0: Invalid 1: Write 1 to reset PSE

15100008 FE_INT_STATUS Frame Engine Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	GDM2_DOS_LIMIT	GDM1_DOS_LIMIT	MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	W1C	RO	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON_0							
Type	RO	W1C	W1C	W1C	RO		W1C	W1C	W1C							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	**MIB counter is almost full on PPE**
30	REV0	**Reserved**
29	GDM2_AF	**MIB counter is almost full on GDM2**
28	GDM1_AF	**MIB counter is almost full on GDM1**
27	GDM2_DOS_LIMIT	**Packet rate is reached (TCP SYN, UDP, ICMP) on GDM2**
26	GDM1_DOS_LIMIT	**Packet rate is reached (TCP SYN, UDP, ICMP) on GDM1**
25	MAC2_LINK	**Link Status Change on MAC2**
24	MAC1_LINK	**Link Status Change on MAC1**
23	GDM2_ERR	**Packet error (checksum, length, etc.) on GDM2**
		Including FIFO overflow, checksum error, undersize, oversize
22	GDM2_CRC	**Packet CRC error on GDM2**
21	GDM1_ERR	**Packet error (checksum, length, etc.) on GDM1**
		Including FIFO overflow, checksum error, undersize, oversize
20	GDM1_CRC	**Packet CRC error on GDM1**
19	RFIFO_UF	**Ring FIFO Underrun Defect**
18	RFIFO_OV	**Ring FIFO Overflow Defect**
17	INFIFO_GET_ERR	**IN FIFO Get Defect**
16	AFIFO_GET_ERR	**ASYNC FIFO Get Defect**
15	REV2	**Reserved**
14	CDM_TSO_ALIGN	**Detect EOF Alignment**
13	CDM_TSO_ILLEGAL	**Ignored illegal packet on CDM TSO**
12	CDM_TSO_FAIL	**TSO Fail on CDM**
11:10	REV3	**Reserved**
9	PSE_DROP	**Packet drop by PSE**

Bit(s)	Name	Description
8	FQ_EMPTY	**PSE free queue is empty**
7:0	PSE_FC_ON_0	**PSE PORT flow control is asserted** PSE port[n] enables the flow control.

1510000C FE_INT_ENABLE Frame Engine Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PPE_AF	REV0	GDM2_AF	GDM1_AF	GDM2_DOS_LIMIT	GDM1_DOS_LIMIT	MAC2_LINK	MAC1_LINK	GDM2_ERR	GDM2_CRC	GDM1_ERR	GDM1_CRC	RFIFO_UF	RFIFO_OV	INFIFO_GET_ERR	AFIFO_GET_ERR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	CDM_TSO_ALIGN	CDM_TSO_ILLEGAL	CDM_TSO_FAIL	REV3		PSE_DROP	FQ_EMPTY	PSE_FC_ON_0							
Type	RW	RW	RW	RW	RW		RW	RW	RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PPE_AF	**MIB counter is almost full on PPE**
30	REV0	**Reserved**
29	GDM2_AF	**MIB counter is almost full on GDM2**
28	GDM1_AF	**MIB counter is almost full on GDM1**
27	GDM2_DOS_LIMIT	**Packet rate is reached (TCP SYN, UDP, ICMP) on GDM2**
26	GDM1_DOS_LIMIT	**Packet rate is reached (TCP SYN, UDP, ICMP) on GDM1**
25	MAC2_LINK	**Link Status Change on MAC2**
24	MAC1_LINK	**Link Status Change on MAC1**
23	GDM2_ERR	**Packet error on GDM2 / Reserved on XGDM2** (GDM2) Including FIFO overflow, checksum error, undersize, oversize (XGDM2) n.a.
22	GDM2_CRC	**CRC error on GDM2 / Packet Error and CRC Error on XGDM2** (GDM2) Frame CRC Error only (XGDM2) Including frame CRC Error, coding error, FIFO overflow, over/undersize, checksum error
21	GDM1_ERR	**Packet error on GDM1 / Reserved on XGDM1** (GDM1) Including FIFO overflow, checksum error, undersize, oversize (XGDM1) n.a.
20	GDM1_CRC	**CRC error on GDM1 / Packet Error and CRC Error on XGDM1** (GDM1) Frame CRC Error only (XGDM1) Including frame CRC Error, coding error, FIFO overflow, over/undersize, checksum error
19	RFIFO_UF	**Ring FIFO Underrun Defect**
18	RFIFO_OV	**Ring FIFO Overflow Defect**
17	INFIFO_GET_ERR	**IN FIFO Get Defect**

Bit(s)	Name	Description
16	AFIFO_GET_ERR	**ASYNC FIFO Get Defect**
15	REV2	**Reserved**
14	CDM_TSO_ALIGN	**Detects EOF alignment**
13	CDM_TSO_ILLEGAL	**Ignores illegal packet on CDM TSO**
12	CDM_TSO_FAIL	**TSO Fail on CDM**
11:10	REV3	**Reserved**
9	PSE_DROP	**Packet drop by PSE**
8	FQ_EMPTY	**PSE free queue is empty**
7:0	PSE_FC_ON_0	**PSE port flow control is asserted** PSE port[n] enables the flow control.

15100010 FE_FOE_TS_T Frame Engine Time Stamp 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FOE_TS_T															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RESV0	**Reserved**
15:0	FOE_TS_T	**Time stamp** Time stamp unit is 1 sec. [Note] This timer is driven by free-running 125 MHz clock

15100014 FE_IPV6_EXT Frame Engine IPv6 Extension Header 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IP6_EXT3								IP6_EXT2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IP6_EXT1								IP6_EXT0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	IP6_EXT3	**IPv6 extension header #3**
23:16	IP6_EXT2	**IPv6 extension header #2**
15:8	IP6_EXT1	**IPv6 extension header #1**
7:0	IP6_EXT0	**IPv6 extension header #0**

15100018 FE_RATE_COMP Frame Engine Rate Limit Compensation 00001818

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_RATE_MINUS	DMA_RATE_BYTE							PSE_RATE_MINUS	PSE_RATE_BYTE						
Type	RW	RW							RW	RW						
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
31:16	REV0	**Reserved**
15	DMA_RATE_MINUS	1'b0: A specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE 1'b1: A specific byte count is subtracted from the incoming frame length.
14:8	DMA_RATE_BYTE	**Byte number for rate control** The byte number should be subtracted while calculating the rate limit.
7	PSE_RATE_MINUS	1'b0: A specific byte count is added to the frame length according to FE_GLO_CFG.RATE_BYTE 1'b1: A specific byte count is subtracted from the incoming frame length.
6:0	PSE_RATE_BYTE	**Byte number for rate control** The byte number should be subtracted while calculating the rate limit.

15100020 FE_INT_GRP Frame Engine Interrupt Group 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_G2_ASG				QDMA_INT_G1_ASG				QDMA_INT_G0_ASG				PDMA_INT_G2_ASG			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PDMA_INT_G1_ASG				PDMA_INT_G0_ASG				PDMA_INT_G3_ASG				FE_MISC_INT_ASG			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	QDMA_INT_G2_ASG	**QDMA group 2 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] 4'h3: Assign to fe_int[3] Others: Reserved
27:24	QDMA_INT_G1_ASG	**QDMA group 1 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] 4'h3: Assign to fe_int[3] Others: Reserved
23:20	QDMA_INT_G0_ASG	**QDMA group 0 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] 4'h3: Assign to fe_int[3] Others: Reserved
19:16	PDMA_INT_G2_ASG	**PDMA group 2 interrupt assignment** 4'h0: Assign to fe_int[0] 4'h1: Assign to fe_int[1] 4'h2: Assign to fe_int[2] 4'h3: Assign to fe_int[3] Others: Reserved
15:12	PDMA_INT_G1_ASG	**PDMA group 1 interrupt assignment**

Bit(s)	Name	Description
		4'h0: Assign to fe_int[0]
		4'h1: Assign to fe_int[1]
		4'h2: Assign to fe_int[2]
		4'h3: Assign to fe_int[3]
		Others: Reserved
11:8	PDMA_INT_G0_ASG	**PDMA group 0 interrupt assignment**
		4'h0: Assign to fe_int[0]
		4'h1: Assign to fe_int[1]
		4'h2: Assign to fe_int[2]
		4'h3: Assign to fe_int[3]
		Others: Reserved
7:4	PDMA_INT_G3_ASG	**PDMA group 3 interrupt assignment**
		4'h0: Assign to fe_int[0]
		4'h1: Assign to fe_int[1]
		4'h2: Assign to fe_int[2]
		4'h3: Assign to fe_int[3]
		Others: Reserved
3:0	FE_MISC_INT_ASG	**Frame engine misc. interrupt assignment**
		4'h0: Assign to fe_int[0]
		4'h1: Assign to fe_int[1]
		4'h2: Assign to fe_int[2]
		4'h3: Assign to fe_int[3]
		Others: Reserved

15100024 FE_GLO_CFG2 Frame Engine Global Configuration Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**LINK_DWN_1**						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	LINK_DWN_1	**Disable PSE Port 8~14** When PSE port is not valid on the Frame Engine, it is suggested to disable the corresponding port.

15100028 FE_INT_STATUS2 Frame Engine Interrupt Status Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PSE_FC_ON_1						
Type										W1C						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	PSE_FC_ON_1	**PSE PORT flow control is asserted** PSE port[n] enables the flow control.

1510002C FE_INT_ENABLE2 Frame Engine Interrupt Enable Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PSE_FC_ON_1						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	PSE_FC_ON_1	PSE PORT flow control interrupt enable

15100100 PSE_FQFC_CFG1 PSE Free Queue Flow Control Part1 01FF01FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FQ_PCNT								
Type								RO								
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FQ_MAX_PCNT								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24:16	FQ_PCNT	**Free queue page count**
8:0	FQ_MAX_PCNT	**Maximum free Q page count.** Please reset PSE after re-programming this register

15100104 PSE_FQFC_CFG2 PSE Free Queue Flow Control Part2 012000E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FQ_HIGH								
Type								RW								
Reset								1	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FQ_LOW								
Type								RW								
Reset								0	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	FQ_HIGH	**High threshold to release FC**
8:0	FQ_LOW	**Low threshold to trigger FC**

15100110 PSE_PPE0_DROP PPE0 Drop Packet Enable Port 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0	PPE0_DROP_P14_EN	PPE0_DROP_P13_EN	PPE0_DROP_P12_EN	PPE0_DROP_P11_EN	PPE0_DROP_P10_EN	PPE0_DROP_P9_EN	PPE0_DROP_P8_EN	PPE0_DROP_P7_EN	PPE0_DROP_P6_EN	PPE0_DROP_P5_EN	PPE0_DROP_P4_EN	PPE0_DROP_P3_EN	PPE0_DROP_P2_EN	PPE0_DROP_P1_EN	PPE0_DROP_P0_EN
Type	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:15	REV0	**Reserved**
14	PPE0_DROP_P14_EN	**Enable PPE0 drop packet to port 14 due to RX ring full** 0: Disable 1: Enable
13	PPE0_DROP_P13_EN	**Enable PPE0 drop packet to port 13 due to RX ring full** 0: Disable 1: Enable
12	PPE0_DROP_P12_EN	**Enable PPE0 drop packet to port 12 due to RX ring full** 0: Disable 1: Enable
11	PPE0_DROP_P11_EN	**Enable PPE0 drop packet to port 11 due to RX ring full** 0: Disable 1: Enable
10	PPE0_DROP_P10_EN	**Enable PPE0 drop packet to port 10 due to RX ring full** 0: Disable 1: Enable
9	PPE0_DROP_P9_EN	**Enable PPE0 drop packet to port 9 due to RX ring full** 0: Disable 1: Enable
8	PPE0_DROP_P8_EN	**Enable PPE0 drop packet to port 8 due to RX ring full** 0: Disable 1: Enable
7	PPE0_DROP_P7_EN	**Enable PPE0 drop packet to port 7 due to RX ring full** 0: Disable

Bit(s)	Name	Description
		1: Enable
6	PPE0_DROP_P6_EN	**Enable PPE0 drop packet to port 6 due to RX ring full** 0: Disable 1: Enable
5	PPE0_DROP_P5_EN	**Enable PPE0 drop packet to port 5 due to RX ring full** 0: Disable 1: Enable
4	PPE0_DROP_P4_EN	**Enable PPE0 drop packet to port 4 due to RX ring full** 0: Disable 1: Enable
3	PPE0_DROP_P3_EN	**Enable PPE0 drop packet to port 3 due to RX ring full** 0: Disable 1: Enable
2	PPE0_DROP_P2_EN	**Enable PPE0 drop packet to port 2 due to RX ring full** 0: Disable 1: Enable
1	PPE0_DROP_P1_EN	**Enable PPE0 drop packet to port 1 due to RX ring full** 0: Disable 1: Enable
0	PPE0_DROP_P0_EN	**Enable PPE0 drop packet to port 0 due to RX ring full** 0: Disable 1: Enable

15100114 PSE_PPE1_DROP PPE1 Drop Packet Enable Port 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0	PPE1_DROP_P14_EN	PPE1_DROP_P13_EN	PPE1_DROP_P12_EN	PPE1_DROP_P11_EN	PPE1_DROP_P10_EN	PPE1_DROP_P9_EN	PPE1_DROP_P8_EN	PPE1_DROP_P7_EN	PPE1_DROP_P6_EN	PPE1_DROP_P5_EN	PPE1_DROP_P4_EN	PPE1_DROP_P3_EN	PPE1_DROP_P2_EN	PPE1_DROP_P1_EN	PPE1_DROP_P0_EN
Type	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:15	REV0	**Reserved**
14	PPE1_DROP_P14_EN	**Enable PPE1 drop packet to port 14 due to RX ring full** 0: Disable 1: Enable
13	PPE1_DROP_P13_EN	**Enable PPE1 drop packet to port 13 due to RX ring full** 0: Disable 1: Enable
12	PPE1_DROP_P12_EN	**Enable PPE1 drop packet to port 12 due to RX ring full** 0: Disable 1: Enable
11	PPE1_DROP_P11_EN	**Enable PPE1 drop packet to port 11 due to RX ring full** 0: Disable 1: Enable
10	PPE1_DROP_P10_EN	**Enable PPE1 drop packet to port 10 due to RX ring full** 0: Disable 1: Enable
9	PPE1_DROP_P9_EN	**Enable PPE1 drop packet to port 9 due to RX ring full** 0: Disable 1: Enable
8	PPE1_DROP_P8_EN	**Enable PPE1 drop packet to port 8 due to RX ring full** 0: Disable 1: Enable
7	PPE1_DROP_P7_EN	**Enable PPE1 drop packet to port 7 due to RX ring full** 0: Disable

Bit(s)	Name	Description
		1: Enable
6	PPE1_DROP_P6_EN	**Enable PPE1 drop packet to port 6 due to RX ring full** 0: Disable 1: Enable
5	PPE1_DROP_P5_EN	**Enable PPE1 drop packet to port 5 due to RX ring full** 0: Disable 1: Enable
4	PPE1_DROP_P4_EN	**Enable PPE1 drop packet to port 4 due to RX ring full** 0: Disable 1: Enable
3	PPE1_DROP_P3_EN	**Enable PPE1 drop packet to port 3 due to RX ring full** 0: Disable 1: Enable
2	PPE1_DROP_P2_EN	**Enable PPE1 drop packet to port 2 due to RX ring full** 0: Disable 1: Enable
1	PPE1_DROP_P1_EN	**Enable PPE1 drop packet to port 1 due to RX ring full** 0: Disable 1: Enable
0	PPE1_DROP_P0_EN	**Enable PPE1 drop packet to port 0 due to RX ring full** 0: Disable 1: Enable

15100130 FE_GDM_RXID1 FE GDM RXID Control 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_VLAN_PRI7_RXID_SEL		GDM_VLAN_PRI6_RXID_SEL		GDM_VLAN_PRI5_RXID_SEL		GDM_VLAN_PRI4_RXID_SEL		GDM_VLAN_PRI3_RXID_SEL		GDM_VLAN_PRI2_RXID_SEL		GDM_VLAN_PRI1_RXID_SEL		GDM_VLAN_PRI0_RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GDM_TCP_ACK_RXID_SEL		GDM_TCP_ACK_WZPC	GDM_RXID_PRI_SEL		
Type											RW		RW	RW		
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
31:30	GDM_VLAN_PRI7_RXID_SEL	**GDM RXID Select for VLAN Priority = 7** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
29:28	GDM_VLAN_PRI6_RXID_SEL	**GDM RXID Select for VLAN Priority = 6** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
27:26	GDM_VLAN_PRI5_RXID_SEL	**GDM RXID Select for VLAN Priority = 5** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
25:24	GDM_VLAN_PRI4_RXID_SEL	**GDM RXID Select for VLAN Priority = 4** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
23:22	GDM_VLAN_PRI3_RXID_SEL	**GDM RXID Select for VLAN Priority = 3** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1)

Bit(s)	Name	Description
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
21:20	GDM_VLAN_PRI2_RXID_SEL	**GDM RXID Select for VLAN Priority = 2**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
19:18	GDM_VLAN_PRI1_RXID_SEL	**GDM RXID Select for VLAN Priority = 1**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
17:16	GDM_VLAN_PRI0_RXID_SEL	**GDM RXID Select for VLAN Priority = 0**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
5:4	GDM_TCP_ACK_RXID_SEL	**GDM RXID Select for TCP ACK**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
3	GDM_TCP_ACK_WZPC	**GDM TCP ACK with zero payload check (L3 payload = L4 header)**
2:0	GDM_RXID_PRI_SEL	**GDM RXID Select Priority Setting**
		Select Priority by PID/STAG, VLAD_PRI, and TCP_ACK
		3'b000: PID/STAG
		3'b001: VLAN_PRI --> PID/STAG
		3'b010: TCP_ACK --> PID/STAG
		3'b011: VLAN_PRI --> TCP_ACK --> PID/STAG
		3'b100: TCP_ACK --> VLAN_PRI --> PID/STAG

15100134 FE_GDM_RXID2 FE GDM RXID Control 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_STAG7_RXID_SEL		GDM_STAG6_RXID_SEL		GDM_STAG5_RXID_SEL		GDM_STAG4_RXID_SEL		GDM_STAG3_RXID_SEL		GDM_STAG2_RXID_SEL		GDM_STAG1_RXID_SEL		GDM_STAG0_RXID_SEL	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GDM_PID2_RXID_SEL		GDM_PID1_RXID_SEL	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
31:30	GDM_STAG7_RXID_SEL	**GDM RXID Select for STAG = 7** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
29:28	GDM_STAG6_RXID_SEL	**GDM RXID Select for STAG = 6** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
27:26	GDM_STAG5_RXID_SEL	**GDM RXID Select for STAG = 5** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
25:24	GDM_STAG4_RXID_SEL	**GDM RXID Select for STAG = 4** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2) 2'b11: Select PDMA RX Ring 3 (RXID = 3)
23:22	GDM_STAG3_RXID_SEL	**GDM RXID Select for STAG = 3** 2'b00: Select PDMA RX Ring 0 (RXID = 0) 2'b01: Select PDMA RX Ring 1 (RXID = 1) 2'b10: Select PDMA RX Ring 2 (RXID = 2)

Bit(s)	Name	Description
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
21:20	GDM_STAG2_RXID_SEL	**GDM RXID Select for STAG = 2**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
19:18	GDM_STAG1_RXID_SEL	**GDM RXID Select for STAG = 1**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
17:16	GDM_STAG0_RXID_SEL	**GDM RXID Select for STAG = 0**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
3:2	GDM_PID2_RXID_SEL	**GDM RXID Select for GDM2 (Port ID = 2)**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)
1:0	GDM_PID1_RXID_SEL	**GDM RXID Select for GDM1 (Port ID = 1)**
		2'b00: Select PDMA RX Ring 0 (RXID = 0)
		2'b01: Select PDMA RX Ring 1 (RXID = 1)
		2'b10: Select PDMA RX Ring 2 (RXID = 2)
		2'b11: Select PDMA RX Ring 3 (RXID = 3)

15100140 PSE_IQ_REV1 PSE Input Queue Reservation Part1 000C0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P0_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P1_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P0_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100144 PSE_IQ_REV2 PSE Input Queue Reservation Part2 01FF000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_IQ_RES								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
24:16	P3_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P2_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100148 PSE_IQ_REV3 PSE Input Queue Reservation Part3 000801FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_IQ_RES								
Type								RW								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24:16	P5_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P4_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

1510014C PSE_IQ_REV4 PSE Input Queue Reservation Part4 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P7_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P6_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100150 PSE_IQ_REV5 PSE Input Queue Reservation Part5 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P9_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P8_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100154 PSE_IQ_REV6 PSE Input Queue Reservation Part6 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P11_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P10_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100158 PSE_IQ_REV7 PSE Input Queue Reservation Part7 00080008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	P13_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).
8:0	P12_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

1510015C PSE_IQ_REV8 PSE Input Queue Reservation Part8 00100008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FREE_DROP								
Type								RW								
Reset								0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P14_IQ_RES								
Type								RW								
Reset								0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
24:16	FREE_DROP	**Free Buffer Drop Threshold**
8:0	P14_IQ_RES	**Virtual input Q reservation** [Note] After the flow control of the ingress port is asserted, it can be released when P[n]_IQ_PCNT is lower than (P[n]_IQ_RES/2).

15100160 PSE_OQ_TH1 PSE Output Queue Threshold Part1 00300020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_OQ_TH								
Type								RW								
Reset								0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P0_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P1_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P0_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100164 PSE_OQ_TH2 PSE Output Queue Threshold Part2 00400030

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_OQ_TH								
Type								RW								
Reset								0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_OQ_TH								
Type								RW								
Reset								0	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
24:16	P3_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P2_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100168 PSE_OQ_TH3 PSE Output Queue Threshold Part3 00200040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_OQ_TH								
Type								RW								
Reset								0	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P5_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P4_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

1510016C PSE_OQ_TH4 PSE Output Queue Threshold Part4 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P7_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P6_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100170 PSE_OQ_TH5 PSE Output Queue Threshold Part5 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P9_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P8_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100174 PSE_OQ_TH6 PSE Output Queue Threshold Part6 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P11_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P10_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100178 PSE_OQ_TH7 PSE Output Queue Threshold Part7 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	P13_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.
8:0	P12_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

1510017C PSE_OQ_TH8 PSE Output Queue Threshold Part8 00200020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								REV								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P14_OQ_TH								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
24:16	REV	**Reserved**
8:0	P14_OQ_TH	**Output Queue FC Threshold** [Note] After the flow control of the egress port is asserted, it can be released when the free buffer count is higher than FQ_HIGH.

15100180 PSE_IQ_STA1 PSE Input Queue Status Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P0_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P1_IQ_PCNT	**Virtual input Q page count**
8:0	P0_IQ_PCNT	**Virtual input Q page count**

15100184 PSE_IQ_STA2 PSE Input Queue Status Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P3_IQ_PCNT	**Virtual input Q page count**
8:0	P2_IQ_PCNT	**Virtual input Q page count**

15100188 PSE_IQ_STA3 PSE Input Queue Status Part3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P5_IQ_PCNT	**Virtual input Q page count**
8:0	P4_IQ_PCNT	**Virtual input Q page count**

1510018C PSE_IQ_STA4 PSE Input Queue Status Part4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P7_IQ_PCNT	**Virtual input Q page count**
8:0	P6_IQ_PCNT	**Virtual input Q page count**

15100190 PSE_IQ_STA5 PSE Input Queue Status Part5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P9_IQ_PCNT	**Virtual input Q page count**
8:0	P8_IQ_PCNT	**Virtual input Q page count**

15100194 PSE_IQ_STA6 PSE Input Queue Status Part6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P11_IQ_PCNT	**Virtual input Q page count**
8:0	P10_IQ_PCNT	**Virtual input Q page count**

15100198 PSE_IQ_STA7 PSE Input Queue Status Part7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_IQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P13_IQ_PCNT	**Virtual input Q page count**
8:0	P12_IQ_PCNT	**Virtual input Q page count**

1510019C PSE_IQ_STA8 PSE Input Queue Status Part8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**P14_IQ_PCNT**								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	P14_IQ_PCNT	**Virtual input Q page count**

151001A0 PSE_OQ_STA1 PSE Output Queue Status Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P1_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P0_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P1_OQ_PCNT	**Output Q page count**
8:0	P0_OQ_PCNT	**Output Q page count**

151001A4 **PSE_OQ_STA2** **PSE Output Queue Status Part2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P3_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P2_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P3_OQ_PCNT	**Output Q page count**
8:0	P2_OQ_PCNT	**Output Q page count**

151001A8 PSE_OQ_STA3 PSE Output Queue Status Part3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P5_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P4_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P5_OQ_PCNT	**Output Q page count**
8:0	P4_OQ_PCNT	**Output Q page count**

151001AC PSE_OQ_STA4 PSE Output Queue Status Part4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P7_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P6_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P7_OQ_PCNT	**Output Q page count**
8:0	P6_OQ_PCNT	**Output Q page count**

151001B0 PSE_OQ_STA5 PSE Output Queue Status Part5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P9_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P8_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P9_OQ_PCNT	**Output Q page count**
8:0	P8_OQ_PCNT	**Output Q page count**

151001B4 **PSE_OQ_STA6** **PSE Output Queue Status Part6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P11_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P10_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P11_OQ_PCNT	**Output Q page count**
8:0	P10_OQ_PCNT	**Output Q page count**

151001B8 PSE_OQ_STA7 PSE Output Queue Status Part7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P13_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								P12_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	P13_OQ_PCNT	**Output Q page count**
8:0	P12_OQ_PCNT	**Output Q page count**

151001BC **PSE_OQ_STA8** **PSE Output Queue Status Part8** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								P14_OQ_PCNT								
Type								RO								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
24:16	P14_OQ_PCNT	**Output Q page count**

151001C0 PSE_TDM_TBL0 PSE TDM Arbiter Table0 84321A43

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_7				TDM_TBL_6				TDM_TBL_5				TDM_TBL_4			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_3				TDM_TBL_2				TDM_TBL_1				TDM_TBL_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1

Bit(s)	Name	Description
31:28	TDM_TBL_7	**PSE TDM arbiter table entry 7**
27:24	TDM_TBL_6	**PSE TDM arbiter table entry 6**
23:20	TDM_TBL_5	**PSE TDM arbiter table entry 5**
19:16	TDM_TBL_4	**PSE TDM arbiter table entry 4**
15:12	TDM_TBL_3	**PSE TDM arbiter table entry 3**
11:8	TDM_TBL_2	**PSE TDM arbiter table entry 2**
7:4	TDM_TBL_1	**PSE TDM arbiter table entry 1**
3:0	TDM_TBL_0	**PSE TDM arbiter table entry 0**

151001C4 **PSE_TDM_TBL1** **PSE TDM Arbiter Table1** **321A4359**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_15				TDM_TBL_14				TDM_TBL_13				TDM_TBL_12			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_11				TDM_TBL_10				TDM_TBL_9				TDM_TBL_8			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	1	0	1	0	1	1	0	0	1

Bit(s)	Name	Description
31:28	TDM_TBL_15	**PSE TDM arbiter table entry 15**
27:24	TDM_TBL_14	**PSE TDM arbiter table entry 14**
23:20	TDM_TBL_13	**PSE TDM arbiter table entry 13**
19:16	TDM_TBL_12	**PSE TDM arbiter table entry 12**
15:12	TDM_TBL_11	**PSE TDM arbiter table entry 11**
11:8	TDM_TBL_10	**PSE TDM arbiter table entry 10**
7:4	TDM_TBL_9	**PSE TDM arbiter table entry 9**
3:0	TDM_TBL_8	**PSE TDM arbiter table entry 8**

151001C8 PSE_TDM_TBL2 PSE TDM Arbiter Table2 1A436984

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_23				TDM_TBL_22				TDM_TBL_21				TDM_TBL_20			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_19				TDM_TBL_18				TDM_TBL_17				TDM_TBL_16			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	1	0	0	1	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	TDM_TBL_23	**PSE TDM arbiter table entry 23**
27:24	TDM_TBL_22	**PSE TDM arbiter table entry 22**
23:20	TDM_TBL_21	**PSE TDM arbiter table entry 21**
19:16	TDM_TBL_20	**PSE TDM arbiter table entry 20**
15:12	TDM_TBL_19	**PSE TDM arbiter table entry 19**
11:8	TDM_TBL_18	**PSE TDM arbiter table entry 18**
7:4	TDM_TBL_17	**PSE TDM arbiter table entry 17**
3:0	TDM_TBL_16	**PSE TDM arbiter table entry 16**

151001CC **PSE_TDM_TBL3** **PSE TDM Arbiter Table3** **30A98432**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_31				TDM_TBL_30				TDM_TBL_29				TDM_TBL_28			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	0	0	1	0	1	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_27				TDM_TBL_26				TDM_TBL_25				TDM_TBL_24			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0

Bit(s)	Name	Description
31:28	TDM_TBL_31	**PSE TDM arbiter table entry 31**
27:24	TDM_TBL_30	**PSE TDM arbiter table entry 30**
23:20	TDM_TBL_29	**PSE TDM arbiter table entry 29**
19:16	TDM_TBL_28	**PSE TDM arbiter table entry 28**
15:12	TDM_TBL_27	**PSE TDM arbiter table entry 27**
11:8	TDM_TBL_26	**PSE TDM arbiter table entry 26**
7:4	TDM_TBL_25	**PSE TDM arbiter table entry 25**
3:0	TDM_TBL_24	**PSE TDM arbiter table entry 24**

151001D0 PSE_TDM_TBL4 PSE TDM Arbiter Table4 8A432154

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_39				TDM_TBL_38				TDM_TBL_37				TDM_TBL_36			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_35				TDM_TBL_34				TDM_TBL_33				TDM_TBL_32			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0

Bit(s)	Name	Description
31:28	TDM_TBL_39	**PSE TDM arbiter table entry 39**
27:24	TDM_TBL_38	**PSE TDM arbiter table entry 38**
23:20	TDM_TBL_37	**PSE TDM arbiter table entry 37**
19:16	TDM_TBL_36	**PSE TDM arbiter table entry 36**
15:12	TDM_TBL_35	**PSE TDM arbiter table entry 35**
11:8	TDM_TBL_34	**PSE TDM arbiter table entry 34**
7:4	TDM_TBL_33	**PSE TDM arbiter table entry 33**
3:0	TDM_TBL_32	**PSE TDM arbiter table entry 32**

151001D4 **PSE_TDM_TBL5** **PSE TDM Arbiter Table5** **321A6439**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_47				TDM_TBL_46				TDM_TBL_45				TDM_TBL_44			
Type	RW				RW				RW				RW			
Reset	0	0	1	1	0	0	1	0	0	0	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_43				TDM_TBL_42				TDM_TBL_41				TDM_TBL_40			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	1	0	0	0	0	1	1	1	0	0	1

Bit(s)	Name	Description
31:28	TDM_TBL_47	**PSE TDM arbiter table entry 47**
27:24	TDM_TBL_46	**PSE TDM arbiter table entry 46**
23:20	TDM_TBL_45	**PSE TDM arbiter table entry 45**
19:16	TDM_TBL_44	**PSE TDM arbiter table entry 44**
15:12	TDM_TBL_43	**PSE TDM arbiter table entry 43**
11:8	TDM_TBL_42	**PSE TDM arbiter table entry 42**
7:4	TDM_TBL_41	**PSE TDM arbiter table entry 41**
3:0	TDM_TBL_40	**PSE TDM arbiter table entry 40**

151001D8 **PSE_TDM_TBL6** **PSE TDM Arbiter Table6** **8435A984**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_55				TDM_TBL_54				TDM_TBL_53				TDM_TBL_52			
Type	RW				RW				RW				RW			
Reset	1	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_51				TDM_TBL_50				TDM_TBL_49				TDM_TBL_48			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	TDM_TBL_55	**PSE TDM arbiter table entry 55**
27:24	TDM_TBL_54	**PSE TDM arbiter table entry 54**
23:20	TDM_TBL_53	**PSE TDM arbiter table entry 53**
19:16	TDM_TBL_52	**PSE TDM arbiter table entry 52**
15:12	TDM_TBL_51	**PSE TDM arbiter table entry 51**
11:8	TDM_TBL_50	**PSE TDM arbiter table entry 50**
7:4	TDM_TBL_49	**PSE TDM arbiter table entry 49**
3:0	TDM_TBL_48	**PSE TDM arbiter table entry 48**

151001DC **PSE_TDM_TBL7** **PSE TDM Arbiter Table7** **602143A9**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDM_TBL_63				TDM_TBL_62				TDM_TBL_61				TDM_TBL_60			
Type	RW				RW				RW				RW			
Reset	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDM_TBL_59				TDM_TBL_58				TDM_TBL_57				TDM_TBL_56			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1

Bit(s)	Name	Description
31:28	TDM_TBL_63	**PSE TDM arbiter table entry 63**
27:24	TDM_TBL_62	**PSE TDM arbiter table entry 62**
23:20	TDM_TBL_61	**PSE TDM arbiter table entry 61**
19:16	TDM_TBL_60	**PSE TDM arbiter table entry 60**
15:12	TDM_TBL_59	**PSE TDM arbiter table entry 59**
11:8	TDM_TBL_58	**PSE TDM arbiter table entry 58**
7:4	TDM_TBL_57	**PSE TDM arbiter table entry 57**
3:0	TDM_TBL_56	**PSE TDM arbiter table entry 56**

151001E0 PSE_SP_CFG0 PSE Strict Priority Configure0 5CBA4312

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRIORITY_7				PRIORITY_6				PRIORITY_5				PRIORITY_4			
Type	RW				RW				RW				RW			
Reset	0	1	0	1	1	1	0	0	1	0	1	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRIORITY_3				PRIORITY_2				PRIORITY_1				PRIORITY_0			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	1	0	0	0	1	0	0	1	0

Bit(s)	Name	Description
31:28	PRIORITY_7	**PSE port num at priority 7**
27:24	PRIORITY_6	**PSE port num at priority 6**
23:20	PRIORITY_5	**PSE port num at priority 5**
19:16	PRIORITY_4	**PSE port num at priority 4**
15:12	PRIORITY_3	**PSE port num at priority 3**
11:8	PRIORITY_2	**PSE port num at priority 2**
7:4	PRIORITY_1	**PSE port num at priority 1**
3:0	PRIORITY_0	**PSE port num at priority 0**

151001E4 **PSE_SP_CFG1** **PSE Strict Priority Configure1** **77770986**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PRIORITY_15				PRIORITY_14				PRIORITY_13				PRIORITY_12			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRIORITY_11				PRIORITY_10				PRIORITY_9				PRIORITY_8			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0

Bit(s)	Name	Description
31:28	PRIORITY_15	**PSE port num at priority 15**
27:24	PRIORITY_14	**PSE port num at priority 14**
23:20	PRIORITY_13	**PSE port num at priority 13**
19:16	PRIORITY_12	**PSE port num at priority 12**
15:12	PRIORITY_11	**PSE port num at priority 11**
11:8	PRIORITY_10	**PSE port num at priority 10**
7:4	PRIORITY_9	**PSE port num at priority 9**
3:0	PRIORITY_8	**PSE port num at priority 8**

151001E8 **PSE_TDM_CFG** **PSE TDM arbiter configure** **003F0003**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											PSE_TDM_ARB_NUM					
Type											RW					
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PSE_SP_ARB_EN	PSE_TDM_ARB_EN
Type															RW	RW
Reset															1	1

Bit(s)	Name	Description
21:16	PSE_TDM_ARB_NUM	**TDM table entry number**
1	PSE_SP_ARB_EN	**Enable PSE Strict priority arbiter; it works if no request matches current TDM slot** 1'b1: Enable SP arbiter 1'b0: Disable SP arbiter
0	PSE_TDM_ARB_EN	**Enable PSE TDM arbiter** 1'b1: Enable TDM arbiter 1'b0: Disable PSE TDM arbiter, back to RR

15100200 FE_CDM1_DBG1 FE CDM1 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM1_FS_RINF_LSB	**CDM1 fs packet info [31:0]**

15100204 FE_CDM1_DBG2 FE CDM1 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM1_FS_RINF_MSB	**CDM1 fs packet info [63:32]**

15100208 FE_CDM2_DBG1 FE CDM2 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM2_FS_RINF_LSB	**CDM2 fs packet info [31:0]**

1510020C FE_CDM2_DBG2 FE CDM2 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM2_FS_RINF_MSB	**CDM2 fs packet info [63:32]**

15100210 FE_GDM1_DBG1 FE GDM1 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM1_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM1_FS_RINF_LSB	**GDM1 fs packet info [31:0]**

15100214 FE_GDM1_DBG2 FE GDM1 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM1_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM1_FS_RINF_MSB	**GDM1 fs packet info [63:32]**

15100218 FE_GDM2_DBG1 FE GDM2 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM2_FS_RINF_LSB	**GDM2 fs packet info [31:0]**

1510021C FE_GDM2_DBG2 FE GDM2 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GDM2_FS_RINF_MSB	**GDM2 fs packet info [63:32]**

15100220 **FE_CDM1_FSM** **FE CDM1 FSM Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

15100224 FE_CDM2_FSM FE CDM2 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

15100228 FE_GDM1_FSM FE GDM1 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				FS_FIFO_FSM					FS_PARSER_FSM				FS_FSM			
Type				RO					RO				RO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TS_PARSER_FSM				TS_FSM			
Type									RO				RO			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	FS_FIFO_FSM	**FSM status in gdm_fs_fifo**
23:20	FS_PARSER_FSM	**FSM status in gdm_fs_parser**
19:16	FS_FSM	**FSM status in gdm_fs_fsm**
7:4	TS_PARSER_FSM	**FSM status in gdm_ts_parser**
3:0	TS_FSM	**FSM status in gdm_ts_fsm**

1510022C FE_GDM2_FSM FE GDM2 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				FS_FIFO_FSM					FS_PARSER_FSM				FS_FSM			
Type				RO					RO				RO			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TS_PARSER_FSM				TS_FSM			
Type									RO				RO			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28:24	FS_FIFO_FSM	**FSM status in gdm_fs_fifo**
23:20	FS_PARSER_FSM	**FSM status in gdm_fs_parser**
19:16	FS_FSM	**FSM status in gdm_fs_fsm**
7:4	TS_PARSER_FSM	**FSM status in gdm_ts_parser**
3:0	TS_FSM	**FSM status in gdm_ts_fsm**

15100230 FE_CDM3_DBG1 FE CDM3 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM3_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM3_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM3_FS_RINF_LSB	**CDM3 fs packet info [31:0]**

15100234 FE_CDM3_DBG2 FE CDM3 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM3_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM3_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM3_FS_RINF_MSB	**CDM3 fs packet info [63:32]**

15100238 FE_CDM3_FSM FE CDM3 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

15100240 **FE_PSE_FREE** **PSE Free Page Count** **01FF01FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								FQ_PCNT_MIN								
Type								RC								
Reset								1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								FQ_PCNT								
Type								RO								
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
24:16	FQ_PCNT_MIN	**Free queue minimum page count since the last read** The minimum free page count will update the value whenever the free page is lower than the current record. The field will be reset to FF after MCU reads it.
8:0	FQ_PCNT	**Free queue page count**

15100244 FE_DROP_FQ FE Packet Drop by Free Queue 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_FQ															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_FQ															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_FQ	**Packet dropped by PSE when the free queue is low.** When GDM is receiving a packet and the free buffer is almost exhausted, PSE will drop any received packet no matter if FC is on or off. The field is reset to 0 after MCU reads it.

15100248 FE_DROP_FC FE Packet Drop by Flow Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_FC															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_FC															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_FC	**Packet dropped by PSE when the flow control is off** When GDM receives the packets over the FC threshold and the flow control is off, PSE will drop the received packet to prevent the free buffer from being exhausted. The field is reset to 0 after MCU reads it.

1510024C FE_DROP_PPE1 FE Packet Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_PPE1	**Packet dropped by PPE1** The PPE1 forwarded packet is dropped because PDMA RX Ring is almost full when PSE_MIR_PORT.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

15100250 FE_DROP_PD_6 FE Packet Drop by Port 6 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P6															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P6	**MIB counter for packet dropped by destination port P6 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[6] = 1 The field is reset to 0 after MCU reads it.

15100254 FE_DROP_PD_5 FE Packet Drop by Port 5 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P5															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P5	**MIB counter for packet dropped by destination port P5 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[5] = 1 The field is reset to 0 after MCU reads it.

15100258 FE_DROP_PD_4 FE Packet Drop by Port 4 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P4															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P4	**MIB counter for packet dropped by destination port P4 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[4] = 1 or PPE_GLO_CFG.PPE_EN = 0 The field is reset to 0 after MCU reads it.

1510025C FE_DROP_PD_3 FE Packet Drop by Port 3 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P3															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P3	**MIB counter for packet dropped by destination port P3 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[3] = 1 The field is reset to 0 after MCU reads it.

15100260 FE_DROP_PD_2 FE Packet Drop by Port 2 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P2															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P2	**MIB counter for packet dropped by destination port P2 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[2] = 1 or MAC_P2_SR.LINK_STATUS = 0 The field is reset to 0 after MCU reads it.

15100264 FE_DROP_PD_1 FE Packet Drop by Port 1 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P1	**MIB counter for packet dropped by destination port P1 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[1] = 1 or MAC_P1_SR.LINK_STATUS = 0 The field is reset to 0 after MCU reads it.

15100268 FE_DROP_PD_0 FE Packet Drop by Port 0 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P0	**MIB counter for packet dropped by destination port P0 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[0] = 1 The field is reset to 0 after MCU reads it.

15100270 FE_DROP_PD_14 FE Packet Drop by Port 14 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P14															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P14	**MIB counter for packet dropped by destination port P14 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[6] = 1 The field is reset to 0 after MCU reads it.

15100274 FE_DROP_PD_13 FE Packet Drop by Port 13 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P13															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P13	**MIB counter for packet dropped by destination port P13 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[5] = 1 The field is reset to 0 after MCU reads it.

15100278 FE_DROP_PD_12 FE Packet Drop by Port 12 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P12															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P12	**MIB counter for packet dropped by destination port P12 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[4] = 1 The field is reset to 0 after MCU reads it.

1510027C FE_DROP_PD_11 FE Packet Drop by Port 11 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P11															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P11	**MIB counter for packet dropped by destination port P11 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[3] = 1 The field is reset to 0 after MCU reads it.

15100280 FE_DROP_PD_10 FE Packet Drop by Port 10 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P10															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P10	**MIB counter for packet dropped by destination port P10 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[2] = 1 The field is reset to 0 after MCU reads it.

15100284 FE_DROP_PD_9 FE Packet Drop by Port 9 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P9															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P9	**MIB counter for packet dropped by destination port P9 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[1] = 1 The field is reset to 0 after MCU reads it.

15100288 FE_DROP_PD_8 FE Packet Drop by Port 8 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P8															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P8	**MIB counter for packet dropped by destination port P8 is disabled** Packet dropped by PSE due to FE_GLO_CFG2.LINK_DWN[0] = 1 The field is reset to 0 after MCU reads it.

1510028C FE_DROP_PD_7 FE Packet Drop by Port 7 Disabled 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_P7															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	PSE_DROP_P7	**MIB counter for packet dropped by destination port P7 is disabled** Packet dropped by PSE due to FE_GLO_CFG.LINK_DWN[7] = 1 The field is reset to 0 after MCU reads it.

15100290 FE_CDM4_DBG1 FE CDM4 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM4_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM4_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM4_FS_RINF_LSB	**CDM4 fs packet info [31:0]**

15100294 FE_CDM4_DBG2 FE CDM4 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM4_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM4_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM4_FS_RINF_MSB	**CDM4 fs packet info [63:32]**

15100298 FE_CDM4_FSM FE CDM4 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

151002A0 FE_DROP_PPE0 FE Packet Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PSE_DROP_PPE0	**Packet dropped by PPE0** The PPE0 forwarded packet is dropped because PDMA RX Ring is almost full when PSE_MIR_PORT.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002A4 FE_DROP_PPE0_P0_R01 FE Packet To Port0 Ring 0&1 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P0_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P0_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P0_R1	**Packet to ADMA Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because ADMA RX Ring 1 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P0_R0	**Packet to ADMA Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because ADMA RX Ring 0 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002A8 FE_DROP_PPE0_P0_R23 FE Packet To Port0 Ring 2&3 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P0_R3															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P0_R2															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P0_R3	**Packet to ADMA Ring 3 dropped by PPE0** The PPE0 forwarded packet is dropped because ADMA RX Ring 3 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P0_R2	**Packet to ADMA Ring 2 dropped by PPE0** The PPE0 forwarded packet is dropped because ADMA RX Ring 2 is almost full when FE_DROP_PPE0.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002AC FE_DROP_PPE0_P5 FE Packet To Port5 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P5_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P5_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P5_R1	**Packet to QDMA Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because QDMA RX Ring 1 is almost full when FE_DROP_PPE0.P5_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P5_R0	**Packet to QDMA Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because QDMA RX Ring 0 is almost full when FE_DROP_PPE0.P5_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002B0 FE_DROP_PPE0_P8 FE Packet To Port8 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P8_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P8_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P8_R1	**Packet to WDMA0 Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because WDMA0 RX Ring 1 is almost full when FE_DROP_PPE0.P8_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P8_R0	**Packet to WDMA0 Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because WDMA0 RX Ring 0 is almost full when FE_DROP_PPE0.P8_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002B4 FE_DROP_PPE0_P9 FE Packet To Port9 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P9_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P9_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P9_R1	**Packet to WDMA1 Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because WDMA1 RX Ring 1 is almost full when FE_DROP_PPE0.P9_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P9_R0	**Packet to WDMA1 Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because WDMA1 RX Ring 0 is almost full when FE_DROP_PPE0.P9_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002B8 FE_DROP_PPE0_P10 FE Packet To Port10 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P10_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P10_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P10_R1	**Packet to MDMA Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because MDMA RX Ring 1 is almost full when FE_DROP_PPE0.P10_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P10_R0	**Packet to MDMA Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because MDMA RX Ring 0 is almost full when FE_DROP_PPE0.P10_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002BC FE_DROP_PPE0_P11 FE Packet To Port11 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P11_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P11_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P11_R1	**Packet to EDMA0 Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because GMAC0 RX Ring 1 is almost full when FE_DROP_PPE0.P11_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P11_R0	**Packet to EDMA0 Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because GMAC0 RX Ring 0 is almost full when FE_DROP_PPE0.P11_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002C0 FE_DROP_PPE0_P12 FE Packet To Port12 Drop by PPE0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE0_P12_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE0_P12_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE0_P12_R1	**Packet to EDMA1 Ring 1 dropped by PPE0** The PPE0 forwarded packet is dropped because GMAC1 RX Ring 1 is almost full when FE_DROP_PPE0.P12_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE0_P12_R0	**Packet to EDMA1 Ring 0 dropped by PPE0** The PPE0 forwarded packet is dropped because GMAC1 RX Ring 0 is almost full when FE_DROP_PPE0.P12_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002C4 FE_DROP_PPE1_P0_R01 FE Packet To Port0 Ring 0&1 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P0_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P0_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P0_R1	**Packet to ADMA Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because ADMA RX Ring 1 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P0_R0	**Packet to ADMA Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because ADMA RX Ring 0 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002C8 FE_DROP_PPE1_P0_R23 FE Packet To Port0 Ring 2&3 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P0_R3															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P0_R2															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P0_R3	**Packet to ADMA Ring 3 dropped by PPE1** The PPE1 forwarded packet is dropped because ADMA RX Ring 3 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P0_R2	**Packet to ADMA Ring 2 dropped by PPE1** The PPE1 forwarded packet is dropped because ADMA RX Ring 2 is almost full when FE_DROP_PPE1.P0_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002CC **FE_DROP_PPE1_P5** **FE Packet To Port5 Drop by PPE1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P5_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P5_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P5_R1	**Packet to QDMA Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because QDMA RX Ring 1 is almost full when FE_DROP_PPE1.P5_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P5_R0	**Packet to QDMA Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because QDMA RX Ring 0 is almost full when FE_DROP_PPE1.P5_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002D0 FE_DROP_PPE1_P8 FE Packet To Port8 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P8_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P8_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P8_R1	**Packet to WDMA0 Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because WDMA0 RX Ring 1 is almost full when FE_DROP_PPE1.P8_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P8_R0	**Packet to WDMA0 Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because WDMA0 RX Ring 0 is almost full when FE_DROP_PPE1.P8_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002D4 FE_DROP_PPE1_P9 FE Packet To Port9 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P9_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P9_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P9_R1	**Packet to WDMA1 Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because WDMA1 RX Ring 1 is almost full when FE_DROP_PPE1.P9_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P9_R0	**Packet to WDMA1 Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because WDMA1 RX Ring 0 is almost full when FE_DROP_PPE1.P9_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002D8 FE_DROP_PPE1_P10 FE Packet To Port10 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P10_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P10_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P10_R1	**Packet to MDMA Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because MDMA RX Ring 1 is almost full when FE_DROP_PPE1.P10_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P10_R0	**Packet to MDMA Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because MDMA RX Ring 0 is almost full when FE_DROP_PPE1.P10_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002DC FE_DROP_PPE1_P11 FE Packet To Port11 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P11_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P11_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P11_R1	**Packet to EDMA0 Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because GMAC0 RX Ring 1 is almost full when FE_DROP_PPE1.P11_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P11_R0	**Packet to EDMA0 Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because GMAC0 RX Ring 0 is almost full when FE_DROP_PPE1.P11_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

151002E0 FE_DROP_PPE1_P12 FE Packet To Port12 Drop by PPE1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PSE_DROP_PPE1_P12_R1															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PSE_DROP_PPE1_P12_R0															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	PSE_DROP_PPE1_P12_R1	**Packet to EDMA1 Ring 1 dropped by PPE1** The PPE1 forwarded packet is dropped because GMAC1 RX Ring 1 is almost full when FE_DROP_PPE1.P12_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.
15:0	PSE_DROP_PPE1_P12_R0	**Packet to EDMA1 Ring 0 dropped by PPE1** The PPE1 forwarded packet is dropped because GMAC1 RX Ring 0 is almost full when FE_DROP_PPE1.P12_DROP_PPE is enabled. The field is reset to 0 after MCU reads it.

15100310 FE_CDM5_DBG1 FE CDM5 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM5_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM5_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM5_FS_RINF_LSB	**CDM5 fs packet info [31:0]**

15100314 FE_CDM5_DBG2 FE CDM5 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM5_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM5_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM5_FS_RINF_MSB	**CDM5 fs packet info [63:32]**

15100318 FE_CDM5_FSM FE CDM5 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

15100320 FE_CDM6_DBG1 FE CDM6 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM6_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM6_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM6_FS_RINF_LSB	**CDM6 fs packet info [31:0]**

15100324 FE_CDM6_DBG2 FE CDM6 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM6_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM6_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM6_FS_RINF_MSB	**CDM6 fs packet info [63:32]**

15100328 FE_CDM6_FSM FE CDM6 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

15100330 FE_CDM7_DBG1 FE CDM7 Debug Part1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM7_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM7_FS_RINF_LSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM7_FS_RINF_LSB	**CDM7 fs packet info [31:0]**

15100334 FE_CDM7_DBG2 FE CDM7 Debug Part2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM7_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CDM7_FS_RINF_MSB															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CDM7_FS_RINF_MSB	**CDM7 fs packet info [63:32]**

15100338 FE_CDM7_FSM FE CDM7 FSM Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					FS_PARSER_FSM								FS_FSM			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				TS_PARSER_FSM									TS_FSM			
Type				RO									RO			
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27:24	FS_PARSER_FSM	**FSM status in cdm_fs_parser**
19:16	FS_FSM	**FSM status in cdm_fs_fsm**
12:8	TS_PARSER_FSM	**FSM status in cdm_ts_parser**
3:0	TS_FSM	**FSM status in cdm_ts_fsm**

15100400 CDMP_IG_CTRL CDM Ingress Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU. 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.

15100404 CDMP_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**TACK2RING_ID**		**TACK2RING_EN**			**UNTAG_EN**
Type											RW		RW			RW
Reset											0	0	0	0		0

Bit(s)	Name	Description
5:4	TACK2RING_ID	**Force mode ring selection of TCP ACK to dedicate Rx Ring function** 0: Ring 0 1: Ring 1 2: RIng2 3: Ring3
3:2	TACK2RING_EN	**Enable TCP ACK to dedicate Rx Ring function** 2'b00: Disable 2'b10: Disable 2'b01: Enable force mode (select ring according to control register) 2'b11: Enable PSE mode (select ring according to PSE assignment)
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15100408 CDMP_PPE_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

15100500 GDM1_IG_CTRL GDM Ingress Control 20717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0						INSV_EN	STAG_EN		GDM_ICS_EN	GDM_TCS_EN	GDM_UCS_EN	DROP_256B			STRP_CRC
Type	RW						RW	RW		RW	RW	RW	RW			RW
Reset	0	0	1	0			0	0		1	1	1	0			1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:28	REV0	**Reserved**
25	INSV_EN	**VLAN insertion** Insert Port VID on the received packets on the corresponding GDM port. 0: Disable 1: Insert 4-byte VLAN tag after Source Address
24	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from GDM port. 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.
22	GDM_ICS_EN	**IPv4 header checksum error drop** 0: Checksum error status reported on RX descriptor (IP4F) 1: Checksum error packet will be dropped
21	GDM_TCS_EN	**TCP checksum error drop** 0: Checksum error status reported on RX descriptor (L4F) 1: Checksum error packet will be dropped
20	GDM_UCS_EN	**UDP checksum error drop** 0: Checksum error status reported on RX descriptor (L4F) 1: Checksum error packet will be dropped
19	DROP_256B	**A special mode to drop packets with payload > 256-bytes** 0: Drop packets according to the standard Ethernet frame length limitation. 1: Drop packets with payload > 256 bytes
16	STRP_CRC	**GDM RX CRC Stripping** 1'b: Disable GDM RX CRC stripping

Bit(s)	Name	Description
		1'b1: Enable GDM RX CRC stripping
15:12	MYMAC_DP	**MY_MAC frames destination port** 4'b0000: ADMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: PPE0 4'b0100: PPE1 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1000: WDMA0 4'b1001: WDMA1 4'b1010: MDMA 4'b1011: EDMA0 4'b1100: EDMA1
11:8	BC_DP	**Broadcast frame destination port** 4'b0000: ADMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: PPE0 4'b0100: PPE1 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1000: WDMA0 4'b1001: WDMA1 4'b1010: MDMA 4'b1011: EDMA0 4'b1100: EDMA1
7:4	MC_DP	**Multicast frame destination port** 4'b0000: ADMA 4'b0001: GDM1

Bit(s)	Name	Description
		4'b0010: GDM2
		4'b0011: PPE0
		4'b0100: PPE1
		4'b0101: QDMA
		4'b0110: Reserved
		4'b0111: Discard
		4'b1000: WDMA0
		4'b1001: WDMA1
		4'b1010: MDMA
		4'b1011: EDMA0
		4'b1100: EDMA1
3:0	UN_DP	**Other frame destination port**
		4'b0000: ADMA
		4'b0001: GDM1
		4'b0010: GDM2
		4'b0011: PPE0
		4'b0100: PPE1
		4'b0101: QDMA
		4'b0110: Reserved
		4'b0111: Discard
		4'b1000: WDMA0
		4'b1001: WDMA1
		4'b1010: MDMA
		4'b1011: EDMA0
		4'b1100: EDMA1

15100504 GDM1_EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		UNTAG_EN	DIS_PAD	DIS_CRC				SHPR_EN	BK_SIZE							
Type		RW	RW	RW				RW	RW							
Reset		0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK		TK_RATE													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from GDM. 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged
29	DIS_PAD	**GMAC TX padding function** 1'b0: Enable GMAC TX padding 1'b1: Disable GMAC TX padding
28	DIS_CRC	**GMAC TX CRC generation** 1'b0: Enable GMAC TX CRC generation 1'b1: Disable GMAC TX CRC generation
24	SHPR_EN	**Enable GDM output shaper** 1'b0: Disable 1'b1: Enable
23:16	BK_SIZE	**GDM output shaper bucket size.** This unit is 1K-byte
15	TK_TICK	**GDM shaper token period** 1'b0: GDM shaper add token every 1ms 1'b1: GDM shaper add token every 20us
13:0	TK_RATE	**GDM output shaper token rate** The unit is 8-byte/ms or 8-byte/20us according to TK_TICK.

15100508 GDM1_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	**MY_MAC Address [31:0]**

1510050C GDM1_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MAC_ADR	**MY_MAC Address [47:32]**

15100510 GDM1_VLAN_GEN GDM VLAN Generation 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	**Inserted VLAN TPID**
15:13	GDM_PRI	**Inserted PRI**
12	GDM_CFI	**Inserted CFI**
11:0	GDM_VID	**Inserted VLAN ID**

15100520 GDM1_DOS_CFG_0 GDM DOS Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPD_2P5G_MODE	ICMP_AND_TOS_EQ_ZERO	MY_MAC_CHECK						TCP_DROP_INT_STATUS	TCP_RATE_LIMITER_RST	TCP_DROP_INT_EN	TCP_SYN_PKT_DROP_EN	TCP_SYN_LIMIT_MODE	TCP_SYN_LIMIT_UNIT		
Type	RW	RW	RW						W1C	RW	RW	RW	RW	RW		
Reset	0	0	0						0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DROP_INT_STATUS	UDP_RATE_LIMITER_RST	UDP_DROP_INT_EN	UDP_PKT_DROP_EN	UDP_LIMIT_MODE	UDP_LIMIT_UNIT			ICMP_DROP_INT_STATUS	ICMP_RATE_LIMITER_RST	ICMP_DROP_INT_EN	ICMP_PKT_DROP_EN	ICMP_LIMIT_MODE	ICMP_LIMIT_UNIT		
Type	W1C	RW	RW	RW	RW	RW			W1C	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SPD_2P5G_MODE	**Support 2.5G rate limitation (only enable in 2.5G mode)** 1'b0: Disable 1'b1: Enable
30	ICMP_AND_TOS_EQ_ZERO	**IPv4 ICMP Packet Recognition Control, check if ipv4 TOS field is 0.** 1'b0: Ignore TOS field of IPv4 header; only check if PROTOCOL field equals 1 to regard it as IPv4 ICMP packet 1'b1: It will also check if TOS field equals 0 besides checking if PROTOCOL field equals 1
29	MY_MAC_CHECK	**MY MAC Address Check Control, only do rate limit on DA=MY MAC packet.** 1'b0: Ignore DA checking of incoming packet involved in rate limit mechanism directly 1'b1: It will check DA of incoming packet to see whether it equals MY_MAC address. If YES, given packet will be involved in rate limit mechanism; otherwise, pass this packet directly
23	TCP_DROP_INT_STATUS	**TCP Packet Drop Interrupt Event Status** 1'b0: No interrupt 1'b1: Interrupt event trigger
22	TCP_RATE_LIMITER_RST	**TCP Rate Limiter Reset Control, assert to reset the rate limit calculation.** 1'b0: Reset asserted 1'b1: Reset de-asserted
21	TCP_DROP_INT_EN	**TCP Packet Drop Interrupt Event Control, assert to enable DDoS event interrupt** 1'b0: Disable interrupt event to final interrupt 1'b1: Enable interrupt event to final interrupt

Bit(s)	Name	Description
20	TCP_SYN_PKT_DROP_EN	**TCP SYN Packet Drop Control when Reaching Rate Limitation, assert to enable DDoS prevent** 1'b0: No packet drop 1'b1: Packet drop for the following TCP SYN packet
19	TCP_SYN_LIMIT_MODE	**TCP SYN Rate Limitation by Packet-based or Rate-based** 1'b0: Packet-based (1 second period) 1'b1: Rate-based
18:16	TCP_SYN_LIMIT_UNIT	**Basic unit setting for TCP SYN DDoS Rate Limitation** 3'b000: 64 packets or 64 Kbps 3'b001: 256 packets or 256 Kbps 3'b010: 1 K packets or 1 Mbps 3'b011: 4 K packets or 4 Mbps 3'b1XX: 16 K packets or 16 Mbps
15	UDP_DROP_INT_STATUS	**UDP Packet Drop Interrupt Event Status** 1'b0: No interrupt 1'b1: Interrupt event trigger
14	UDP_RATE_LIMITER_RST	**UDP Rate Limiter Reset Control, assert to reset the rate limit calculation.** 1'b0: Reset asserted 1'b1: Reset de-asserted
13	UDP_DROP_INT_EN	**UDP Packet Drop Interrupt Event Control, assert to enable DDoS event interrupt** 1'b0: Disable interrupt event to final interrupt 1'b1: Enable interrupt event to final interrupt
12	UDP_PKT_DROP_EN	**UDP Packet Drop Control when Reaching Rate Limitation, assert to enable DDoS prevent** 1'b0: No packet drop 1'b1: Packet drop for the following UDP packet
11	UDP_LIMIT_MODE	**UDP Rate Limitation by Packet-based or Rate-based** 1'b0: Packet-based (1 second period) 1'b1: Rate-based
10:8	UDP_LIMIT_UNIT	**Basic unit setting for UDP DDoS Rate Limitation** 3'b000: 64 packets or 64 Kbps 3'b001: 256 packets or 256 Kbps

Bit(s)	Name	Description
		3'b010: 1 K packets or 1 Mbps
		3'b011: 4 K packets or 4 Mbps
		3'b1XX: 16 K packets or 16 Mbps
7	ICMP_DROP_INT_STATUS	**ICMP Packet Drop Interrupt Event Status**
		1'b0: No interrupt
		1'b1: Interrupt event trigger
6	ICMP_RATE_LIMITER_RST	**ICMP Rate Limiter Reset Control, assert to reset the rate limit calculation.**
		1'b0: Reset asserted
		1'b1: Reset de-asserted
5	ICMP_DROP_INT_EN	**ICMP Packet Drop Interrupt Event Control, assert to enable DDoS event interrupt**
		1'b0: Disable interrupt event to final interrupt
		1'b1: Enable interrupt event to final interrupt
4	ICMP_PKT_DROP_EN	**ICMP Packet Drop Control when Reaching Rate Limitation, assert to enable DDoS prevent**
		1'b0: No packet drop
		1'b1: Packet drop for the following ICMP packet
3	ICMP_LIMIT_MODE	**ICMP Rate Limitation by Packet-based or Rate-based**
		1'b0: Packet-based (1 second period)
		1'b1: Rate-based
2:0	ICMP_LIMIT_UNIT	**ICMP Rate Limitation by Packet-based or Rate-based**
		3'b000: 64 packets or 64 Kbps
		3'b001: 256 packets or 256 Kbps
		3'b010: 1 K packets or 1 Mbps
		3'b011: 4 K packets or 4 Mbps
		3'b1XX: 16 K packets or 16 Mbps

15100524 GDM1_DOS_CFG_1 GDM DOS Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCP_SYN_LIMIT_2P5G								TCP_SYN_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TCP_SYN_LIMIT_100M								TCP_SYN_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TCP_SYN_LIMIT_2P5G	**2500 link speed Mbps TCP_SYN Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps
23:16	TCP_SYN_LIMIT_1G	**1000 Mbps link speed TCP_SYN Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps
15:8	TCP_SYN_LIMIT_100M	**100 Mbps link speed TCP_SYN Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps
7:0	TCP_SYN_LIMIT_10M	**10 Mbps link speed TCP_SYN Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps

15100528 GDM1_DOS_CFG_2 GDM DOS Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_LIMIT_2P5G								UDP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_LIMIT_100M								UDP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	UDP_LIMIT_2P5G	**2500 link speed Mbps UDP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps
23:16	UDP_LIMIT_1G	**1000 link speed Mbps UDP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps
15:8	UDP_LIMIT_100M	**100 link speed Mbps UDP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps
7:0	UDP_LIMIT_10M	**10 link speed Mbps UDP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps

1510052C GDM1_DOS_CFG_3 GDM DOS Configuration 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ICMP_LIMIT_2P5G								ICMP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ICMP_LIMIT_100M								ICMP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ICMP_LIMIT_2P5G	**2500 link speed Mbps ICMP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps
23:16	ICMP_LIMIT_1G	**1000 link speed Mbps ICMP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps
15:8	ICMP_LIMIT_100M	**100 link speed Mbps ICMP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128 (unit number) 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps
7:0	ICMP_LIMIT_10M	**10 link speed Mbps ICMP Rate Limit Control unit number.** Limit rate calculation = Basic unit * unit number. Example: 8Mbps = 64K bytes (basic unit) * 128(unit number) 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps

15100C00 PFC_CFG_0 PFC GMAC1 Input Priority ReMap 0 08040201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_IN_PRI_3								GMAC1_IN_PRI_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_IN_PRI_1								GMAC1_IN_PRI_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC1_IN_PRI_3	**GMAC1 Input Priority Re-Map Selection for Priority 3**
23:16	GMAC1_IN_PRI_2	**GMAC1 Input Priority Re-Map Selection for Priority 2**
15:8	GMAC1_IN_PRI_1	**GMAC1 Input Priority Re-Map Selection for Priority 1**
7:0	GMAC1_IN_PRI_0	**GMAC1 Input Priority Re-Map Selection for Priority 0**

15100C04 **PFC_CFG_1** **PFC GMAC1 Input Priority ReMap 1** **80402010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_IN_PRI_7								GMAC1_IN_PRI_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_IN_PRI_5								GMAC1_IN_PRI_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC1_IN_PRI_7	**GMAC1 Input Priority Re-Map Selection for Priority 7**
23:16	GMAC1_IN_PRI_6	**GMAC1 Input Priority Re-Map Selection for Priority 6**
15:8	GMAC1_IN_PRI_5	**GMAC1 Input Priority Re-Map Selection for Priority 5**
7:0	GMAC1_IN_PRI_4	**GMAC1 Input Priority Re-Map Selection for Priority 4**

15100C08 **PFC_CFG_2** **PFC GMAC2 Input Priority ReMap 0** **08040201**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_IN_PRI_3								GMAC2_IN_PRI_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_IN_PRI_1								GMAC2_IN_PRI_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC2_IN_PRI_3	**GMAC2 Input Priority Re-Map Selection for Priority 3**
23:16	GMAC2_IN_PRI_2	**GMAC2 Input Priority Re-Map Selection for Priority 2**
15:8	GMAC2_IN_PRI_1	**GMAC2 Input Priority Re-Map Selection for Priority 1**
7:0	GMAC2_IN_PRI_0	**GMAC2 Input Priority Re-Map Selection for Priority 0**

15100C0C **PFC_CFG_3** **PFC GMAC2 Input Priority ReMap 1** **80402010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_IN_PRI_7								GMAC2_IN_PRI_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_IN_PRI_5								GMAC2_IN_PRI_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC2_IN_PRI_7	**GMAC2 Input Priority Re-Map Selection for Priority 7**
23:16	GMAC2_IN_PRI_6	**GMAC2 Input Priority Re-Map Selection for Priority 6**
15:8	GMAC2_IN_PRI_5	**GMAC2 Input Priority Re-Map Selection for Priority 5**
7:0	GMAC2_IN_PRI_4	**GMAC2 Input Priority Re-Map Selection for Priority 4**

15100C10 PFC_CFG_4 PFC WDMA0_1 Input Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA1_IN_PRI_7		WDMA1_IN_PRI_6		WDMA1_IN_PRI_5		WDMA1_IN_PRI_4		WDMA1_IN_PRI_3		WDMA1_IN_PRI_2		WDMA1_IN_PRI_1		WDMA1_IN_PRI_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA0_IN_PRI_7		WDMA0_IN_PRI_6		WDMA0_IN_PRI_5		WDMA0_IN_PRI_4		WDMA0_IN_PRI_3		WDMA0_IN_PRI_2		WDMA0_IN_PRI_1		WDMA0_IN_PRI_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	WDMA1_IN_PRI_7	**WDMA1 Input Priority Re-Map Selection for Priority 7**
29:28	WDMA1_IN_PRI_6	**WDMA1 Input Priority Re-Map Selection for Priority 6**
27:26	WDMA1_IN_PRI_5	**WDMA1 Input Priority Re-Map Selection for Priority 5**
25:24	WDMA1_IN_PRI_4	**WDMA1 Input Priority Re-Map Selection for Priority 4**
23:22	WDMA1_IN_PRI_3	**WDMA1 Input Priority Re-Map Selection for Priority 3**
21:20	WDMA1_IN_PRI_2	**WDMA1 Input Priority Re-Map Selection for Priority 2**
19:18	WDMA1_IN_PRI_1	**WDMA1 Input Priority Re-Map Selection for Priority 1**
17:16	WDMA1_IN_PRI_0	**WDMA1 Input Priority Re-Map Selection for Priority 0**
15:14	WDMA0_IN_PRI_7	**WDMA0 Input Priority Re-Map Selection for Priority 7**
13:12	WDMA0_IN_PRI_6	**WDMA0 Input Priority Re-Map Selection for Priority 6**
11:10	WDMA0_IN_PRI_5	**WDMA0 Input Priority Re-Map Selection for Priority 5**
9:8	WDMA0_IN_PRI_4	**WDMA0 Input Priority Re-Map Selection for Priority 4**
7:6	WDMA0_IN_PRI_3	**WDMA0 Input Priority Re-Map Selection for Priority 3**
5:4	WDMA0_IN_PRI_2	**WDMA0 Input Priority Re-Map Selection for Priority 2**
3:2	WDMA0_IN_PRI_1	**WDMA0 Input Priority Re-Map Selection for Priority 1**
1:0	WDMA0_IN_PRI_0	**WDMA0 Input Priority Re-Map Selection for Priority 0**

15100C60 PFC_CFG_5 PFC QDMA Input Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_31_0	**QDMA Input Priority Re-Map Selection for Priority 0 [31:0]**

15100C64 **PFC_CFG_6** **PFC QDMA Input Priority ReMap 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_63_32	**QDMA Input Priority Re-Map Selection for Priority 0 [63:32]**

15100C68 **PFC_CFG_7** **PFC QDMA Input Priority ReMap 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_95_64	**QDMA Input Priority Re-Map Selection for Priority 0 [95:64]**

15100C6C **PFC_CFG_8** **PFC QDMA Input Priority ReMap 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_0_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_0_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_0_127_96	**QDMA Input Priority Re-Map Selection for Priority 0 [127:96]**

15100C70 PFC_CFG_9 PFC QDMA Input Priority ReMap 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_31_0	**QDMA Input Priority Re-Map Selection for Priority 1 [31:0]**

15100C74 PFC_CFG_10 PFC QDMA Input Priority ReMap 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_63_32	**QDMA Input Priority Re-Map Selection for Priority 1 [63:32]**

15100C78 PFC_CFG_11 PFC QDMA Input Priority ReMap 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_95_64	**QDMA Input Priority Re-Map Selection for Priority 1 [95:64]**

15100C7C PFC_CFG_12 PFC QDMA Input Priority ReMap 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_1_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_1_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_1_127_96	**QDMA Input Priority Re-Map Selection for Priority 1 [127:96]**

15100C80 PFC_CFG_13 PFC QDMA Input Priority ReMap 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_31_0	**QDMA Input Priority Re-Map Selection for Priority 2 [31:0]**

15100C84 **PFC_CFG_14** **PFC QDMA Input Priority ReMap 9** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_63_32	**QDMA Input Priority Re-Map Selection for Priority 2 [63:32]**

15100C88 PFC_CFG_15 PFC QDMA Input Priority ReMap 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_95_64	**QDMA Input Priority Re-Map Selection for Priority 2 [95:64]**

15100C8C **PFC_CFG_16** **PFC QDMA Input Priority ReMap 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_2_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_2_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_2_127_96	**QDMA Input Priority Re-Map Selection for Priority 2 [127:96]**

15100C90 PFC_CFG_17 PFC QDMA Input Priority ReMap 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_31_0	**QDMA Input Priority Re-Map Selection for Priority 3 [31:0]**

15100C94 PFC_CFG_18 PFC QDMA Input Priority ReMap 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_63_32	**QDMA Input Priority Re-Map Selection for Priority 3 [63:32]**

15100C98 PFC_CFG_19 PFC QDMA Input Priority ReMap 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_95_64	**QDMA Input Priority Re-Map Selection for Priority 3 [95:64]**

15100C9C **PFC_CFG_20** **PFC QDMA Input Priority ReMap 15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_3_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_3_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_3_127_96	**QDMA Input Priority Re-Map Selection for Priority 3 [127:96]**

15100CA0 PFC_CFG_21 PFC QDMA Input Priority ReMap 16 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_31_0	**QDMA Input Priority Re-Map Selection for Priority 4 [31:0]**

15100CA4 **PFC_CFG_22** **PFC QDMA Input Priority ReMap 17** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_63_32	**QDMA Input Priority Re-Map Selection for Priority 4 [63:32]**

15100CA8 PFC_CFG_23 PFC QDMA Input Priority ReMap 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_95_64	**QDMA Input Priority Re-Map Selection for Priority 4 [95:64]**

15100CAC **PFC_CFG_24** **PFC QDMA Input Priority ReMap 19** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_4_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_4_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_4_127_96	**QDMA Input Priority Re-Map Selection for Priority 4 [127:96]**

15100CB0 PFC_CFG_25 PFC QDMA Input Priority ReMap 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_31_0	**QDMA Input Priority Re-Map Selection for Priority 5 [31:0]**

15100CB4 PFC_CFG_26 PFC QDMA Input Priority ReMap 21 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_63_32	**QDMA Input Priority Re-Map Selection for Priority 5 [63:32]**

15100CB8 PFC_CFG_27 PFC QDMA Input Priority ReMap 22 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_95_64	**QDMA Input Priority Re-Map Selection for Priority 5 [95:64]**

15100CBC **PFC_CFG_28** **PFC QDMA Input Priority ReMap 23** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_5_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_5_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_5_127_96	**QDMA Input Priority Re-Map Selection for Priority 5 [127:96]**

15100CC0 PFC_CFG_29 PFC QDMA Input Priority ReMap 24 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_31_0	**QDMA Input Priority Re-Map Selection for Priority 6 [31:0]**

15100CC4 PFC_CFG_30 PFC QDMA Input Priority ReMap 25 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_63_32	**QDMA Input Priority Re-Map Selection for Priority 6 [63:32]**

15100CC8 PFC_CFG_31 PFC QDMA Input Priority ReMap 26 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_95_64	**QDMA Input Priority Re-Map Selection for Priority 6 [95:64]**

15100CCC **PFC_CFG_32** **PFC QDMA Input Priority ReMap 27** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_6_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_6_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_6_127_96	**QDMA Input Priority Re-Map Selection for Priority 6 [127:96]**

15100CD0 PFC_CFG_33 PFC QDMA Input Priority ReMap 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_31_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_31_0	**QDMA Input Priority Re-Map Selection for Priority 7 [31:0]**

15100CD4 PFC_CFG_34 PFC QDMA Input Priority ReMap 29 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_63_32															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_63_32	**QDMA Input Priority Re-Map Selection for Priority 7 [63:32]**

15100CD8 PFC_CFG_35 PFC QDMA Input Priority ReMap 30 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_95_64															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_95_64	**QDMA Input Priority Re-Map Selection for Priority 7 [95:64]**

15100CDC PFC_CFG_36 PFC QDMA Input Priority ReMap 31 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_IN_PRI_7_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_7_127_96															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_IN_PRI_7_127_96	**QDMA Input Priority Re-Map Selection for Priority 7 [127:96]**

15100D60 PFC_CFG_37 PFC GMAC1 Output Priority ReMap 0 08040201

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_OUT_PRI_Q_3								GMAC1_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_OUT_PRI_Q_1								GMAC1_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC1_OUT_PRI_Q_3	**GMAC1 Output Priority Queue 3 Re-Map Selection**
23:16	GMAC1_OUT_PRI_Q_2	**GMAC1 Output Priority Queue 2 Re-Map Selection**
15:8	GMAC1_OUT_PRI_Q_1	**GMAC1 Output Priority Queue 1 Re-Map Selection**
7:0	GMAC1_OUT_PRI_Q_0	**GMAC1 Output Priority Queue 0 Re-Map Selection**

15100D64 **PFC_CFG_38** **PFC GMAC1 Output Priority ReMap 1** **80402010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC1_OUT_PRI_Q_7								GMAC1_OUT_PRI_Q_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC1_OUT_PRI_Q_5								GMAC1_OUT_PRI_Q_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC1_OUT_PRI_Q_7	**GMAC1 Output Priority Queue 7 Re-Map Selection**
23:16	GMAC1_OUT_PRI_Q_6	**GMAC1 Output Priority Queue 6 Re-Map Selection**
15:8	GMAC1_OUT_PRI_Q_5	**GMAC1 Output Priority Queue 5 Re-Map Selection**
7:0	GMAC1_OUT_PRI_Q_4	**GMAC1 Output Priority Queue 4 Re-Map Selection**

15100D68 **PFC_CFG_39** **PFC GMAC2 Output Priority ReMap 0** **08040201**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_OUT_PRI_Q_3								GMAC2_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_OUT_PRI_Q_1								GMAC2_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:24	GMAC2_OUT_PRI_Q_3	**GMAC2 Output Priority Queue 3 Re-Map Selection**
23:16	GMAC2_OUT_PRI_Q_2	**GMAC2 Output Priority Queue 2 Re-Map Selection**
15:8	GMAC2_OUT_PRI_Q_1	**GMAC2 Output Priority Queue 1 Re-Map Selection**
7:0	GMAC2_OUT_PRI_Q_0	**GMAC2 Output Priority Queue 0 Re-Map Selection**

15100D6C **PFC_CFG_40** **PFC GMAC2 Output Priority ReMap 1** **80402010**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GMAC2_OUT_PRI_Q_7								GMAC2_OUT_PRI_Q_6							
Type	RW								RW							
Reset	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GMAC2_OUT_PRI_Q_5								GMAC2_OUT_PRI_Q_4							
Type	RW								RW							
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:24	GMAC2_OUT_PRI_Q_7	**GMAC2 Output Priority Queue 7 Re-Map Selection**
23:16	GMAC2_OUT_PRI_Q_6	**GMAC2 Output Priority Queue 6 Re-Map Selection**
15:8	GMAC2_OUT_PRI_Q_5	**GMAC2 Output Priority Queue 5 Re-Map Selection**
7:0	GMAC2_OUT_PRI_Q_4	**GMAC2 Output Priority Queue 4 Re-Map Selection**

15100D70 PFC_CFG_41 PFC WDMA0 Output Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA0_OUT_PRI_Q_3								WDMA0_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA0_OUT_PRI_Q_1								WDMA0_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	WDMA0_OUT_PRI_Q_3	**WDMA0 Output Priority Queue 3 Re-Map Selection**
23:16	WDMA0_OUT_PRI_Q_2	**WDMA0 Output Priority Queue 2 Re-Map Selection**
15:8	WDMA0_OUT_PRI_Q_1	**WDMA0 Output Priority Queue 1 Re-Map Selection**
7:0	WDMA0_OUT_PRI_Q_0	**WDMA0 Output Priority Queue 0 Re-Map Selection**

15100D74 PFC_CFG_42 PFC WDMA1 Output Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDMA1_OUT_PRI_Q_3								WDMA1_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDMA1_OUT_PRI_Q_1								WDMA1_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	WDMA1_OUT_PRI_Q_3	**WDMA1 Output Priority Queue 3 Re-Map Selection**
23:16	WDMA1_OUT_PRI_Q_2	**WDMA1 Output Priority Queue 2 Re-Map Selection**
15:8	WDMA1_OUT_PRI_Q_1	**WDMA1 Output Priority Queue 1 Re-Map Selection**
7:0	WDMA1_OUT_PRI_Q_0	**WDMA1 Output Priority Queue 0 Re-Map Selection**

15100DA0 PFC_CFG_43 PFC QDMA Output Priority ReMap 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_3								QDMA_OUT_PRI_Q_2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_1								QDMA_OUT_PRI_Q_0							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_3	**QDMA Output Priority Queue 3 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_2	**QDMA Output Priority Queue 2 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_1	**QDMA Output Priority Queue 1 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_0	**QDMA Output Priority Queue 0 Re-Map Selection**

15100DA4 PFC_CFG_44 PFC QDMA Output Priority ReMap 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_7								QDMA_OUT_PRI_Q_6							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_5								QDMA_OUT_PRI_Q_4							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_7	**QDMA Output Priority Queue 7 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_6	**QDMA Output Priority Queue 6 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_5	**QDMA Output Priority Queue 5 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_4	**QDMA Output Priority Queue 4 Re-Map Selection**

15100DA8 PFC_CFG_45 PFC QDMA Output Priority ReMap 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_11								QDMA_OUT_PRI_Q_10							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_9								QDMA_OUT_PRI_Q_8							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_11	**QDMA Output Priority Queue 11 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_10	**QDMA Output Priority Queue 10 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_9	**QDMA Output Priority Queue 9 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_8	**QDMA Output Priority Queue 8 Re-Map Selection**

15100DAC **PFC_CFG_46** **PFC QDMA Output Priority ReMap 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_15								QDMA_OUT_PRI_Q_14							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_13								QDMA_OUT_PRI_Q_12							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_15	**QDMA Output Priority Queue 15 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_14	**QDMA Output Priority Queue 14 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_13	**QDMA Output Priority Queue 13 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_12	**QDMA Output Priority Queue 12 Re-Map Selection**

15100DB0 PFC_CFG_47 PFC QDMA Output Priority ReMap 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_19								QDMA_OUT_PRI_Q_18							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_17								QDMA_OUT_PRI_Q_16							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_19	**QDMA Output Priority Queue 19 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_18	**QDMA Output Priority Queue 18 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_17	**QDMA Output Priority Queue 17 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_16	**QDMA Output Priority Queue 16 Re-Map Selection**

15100DB4 **PFC_CFG_48** **PFC QDMA Output Priority ReMap 5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_23								QDMA_OUT_PRI_Q_22							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_21								QDMA_OUT_PRI_Q_20							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_23	**QDMA Output Priority Queue 23 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_22	**QDMA Output Priority Queue 22 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_21	**QDMA Output Priority Queue 21 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_20	**QDMA Output Priority Queue 20 Re-Map Selection**

15100DB8 PFC_CFG_49 PFC QDMA Output Priority ReMap 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_27								QDMA_OUT_PRI_Q_26							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_25								QDMA_OUT_PRI_Q_24							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_27	**QDMA Output Priority Queue 27 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_26	**QDMA Output Priority Queue 26 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_25	**QDMA Output Priority Queue 25 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_24	**QDMA Output Priority Queue 24 Re-Map Selection**

15100DBC **PFC_CFG_50** **PFC QDMA Output Priority ReMap 7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_31								QDMA_OUT_PRI_Q_30							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_29								QDMA_OUT_PRI_Q_28							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_31	**QDMA Output Priority Queue 31 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_30	**QDMA Output Priority Queue 30 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_29	**QDMA Output Priority Queue 29 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_28	**QDMA Output Priority Queue 28 Re-Map Selection**

15100DC0 PFC_CFG_51 PFC QDMA Output Priority ReMap 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_35								QDMA_OUT_PRI_Q_34							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_33								QDMA_OUT_PRI_Q_32							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_35	**QDMA Output Priority Queue 35 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_34	**QDMA Output Priority Queue 34 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_33	**QDMA Output Priority Queue 33 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_32	**QDMA Output Priority Queue 32 Re-Map Selection**

15100DC4 PFC_CFG_52 PFC QDMA Output Priority ReMap 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_39								QDMA_OUT_PRI_Q_38							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_37								QDMA_OUT_PRI_Q_36							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_39	**QDMA Output Priority Queue 39 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_38	**QDMA Output Priority Queue 38 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_37	**QDMA Output Priority Queue 37 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_36	**QDMA Output Priority Queue 36 Re-Map Selection**

15100DC8 PFC_CFG_53 PFC QDMA Output Priority ReMap 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_43								QDMA_OUT_PRI_Q_42							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_41								QDMA_OUT_PRI_Q_40							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_43	**QDMA Output Priority Queue 43 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_42	**QDMA Output Priority Queue 42 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_41	**QDMA Output Priority Queue 41 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_40	**QDMA Output Priority Queue 40 Re-Map Selection**

15100DCC **PFC_CFG_54** **PFC QDMA Output Priority ReMap 11** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_47								QDMA_OUT_PRI_Q_46							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_45								QDMA_OUT_PRI_Q_44							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_47	**QDMA Output Priority Queue 47 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_46	**QDMA Output Priority Queue 46 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_45	**QDMA Output Priority Queue 45 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_44	**QDMA Output Priority Queue 44 Re-Map Selection**

15100DD0 **PFC_CFG_55** **PFC QDMA Output Priority ReMap 12** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_51								QDMA_OUT_PRI_Q_50							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_49								QDMA_OUT_PRI_Q_48							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_51	**QDMA Output Priority Queue 51 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_50	**QDMA Output Priority Queue 50 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_49	**QDMA Output Priority Queue 49 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_48	**QDMA Output Priority Queue 48 Re-Map Selection**

15100DD4 PFC_CFG_56 PFC QDMA Output Priority ReMap 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_55								QDMA_OUT_PRI_Q_54							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_53								QDMA_OUT_PRI_Q_52							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_55	**QDMA Output Priority Queue 55 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_54	**QDMA Output Priority Queue 54 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_53	**QDMA Output Priority Queue 53 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_52	**QDMA Output Priority Queue 52 Re-Map Selection**

15100DD8 PFC_CFG_57 PFC QDMA Output Priority ReMap 14 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_59								QDMA_OUT_PRI_Q_58							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_57								QDMA_OUT_PRI_Q_56							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_59	**QDMA Output Priority Queue 59 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_58	**QDMA Output Priority Queue 58 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_57	**QDMA Output Priority Queue 57 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_56	**QDMA Output Priority Queue 56 Re-Map Selection**

15100DDC **PFC_CFG_58** **PFC QDMA Output Priority ReMap 15** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_63								QDMA_OUT_PRI_Q_62							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_61								QDMA_OUT_PRI_Q_60							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_63	**QDMA Output Priority Queue 63 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_62	**QDMA Output Priority Queue 62 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_61	**QDMA Output Priority Queue 61 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_60	**QDMA Output Priority Queue 60 Re-Map Selection**

15100DE0 **PFC_CFG_59** **PFC QDMA Output Priority ReMap 16** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_67								QDMA_OUT_PRI_Q_66							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_65								QDMA_OUT_PRI_Q_64							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_67	**QDMA Output Priority Queue 67 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_66	**QDMA Output Priority Queue 66 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_65	**QDMA Output Priority Queue 65 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_64	**QDMA Output Priority Queue 64 Re-Map Selection**

15100DE4 **PFC_CFG_60** **PFC QDMA Output Priority ReMap 17** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_71								QDMA_OUT_PRI_Q_70							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_69								QDMA_OUT_PRI_Q_68							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_71	**QDMA Output Priority Queue 71 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_70	**QDMA Output Priority Queue 70 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_69	**QDMA Output Priority Queue 69 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_68	**QDMA Output Priority Queue 68 Re-Map Selection**

15100DE8 PFC_CFG_61 PFC QDMA Output Priority ReMap 18 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_75								QDMA_OUT_PRI_Q_74							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_73								QDMA_OUT_PRI_Q_72							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_75	**QDMA Output Priority Queue 75 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_74	**QDMA Output Priority Queue 74 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_73	**QDMA Output Priority Queue 73 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_72	**QDMA Output Priority Queue 72 Re-Map Selection**

15100DEC **PFC_CFG_62** **PFC QDMA Output Priority ReMap 19** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_79								QDMA_OUT_PRI_Q_78							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_77								QDMA_OUT_PRI_Q_76							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_79	**QDMA Output Priority Queue 79 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_78	**QDMA Output Priority Queue 78 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_77	**QDMA Output Priority Queue 77 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_76	**QDMA Output Priority Queue 76 Re-Map Selection**

15100DF0 PFC_CFG_63 PFC QDMA Output Priority ReMap 20 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_83								QDMA_OUT_PRI_Q_82							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_81								QDMA_OUT_PRI_Q_80							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_83	**QDMA Output Priority Queue 83 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_82	**QDMA Output Priority Queue 82 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_81	**QDMA Output Priority Queue 81 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_80	**QDMA Output Priority Queue 80 Re-Map Selection**

15100DF4 **PFC_CFG_64** **PFC QDMA Output Priority ReMap 21** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_87								QDMA_OUT_PRI_Q_86							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_85								QDMA_OUT_PRI_Q_84							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_87	**QDMA Output Priority Queue 87 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_86	**QDMA Output Priority Queue 86 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_85	**QDMA Output Priority Queue 85 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_84	**QDMA Output Priority Queue 84 Re-Map Selection**

15100DF8 **PFC_CFG_65** **PFC QDMA Output Priority ReMap 22** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_91								QDMA_OUT_PRI_Q_90							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_89								QDMA_OUT_PRI_Q_88							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_91	**QDMA Output Priority Queue 91 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_90	**QDMA Output Priority Queue 90 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_89	**QDMA Output Priority Queue 89 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_88	**QDMA Output Priority Queue 88 Re-Map Selection**

15100DFC **PFC_CFG_66** **PFC QDMA Output Priority ReMap 23** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_95								QDMA_OUT_PRI_Q_94							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_93								QDMA_OUT_PRI_Q_92							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_95	**QDMA Output Priority Queue 95 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_94	**QDMA Output Priority Queue 94 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_93	**QDMA Output Priority Queue 93 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_92	**QDMA Output Priority Queue 92 Re-Map Selection**

15100E00 **PFC_CFG_67** **PFC QDMA Output Priority ReMap 24** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_99								QDMA_OUT_PRI_Q_98							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_97								QDMA_OUT_PRI_Q_96							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_99	**QDMA Output Priority Queue 99 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_98	**QDMA Output Priority Queue 98 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_97	**QDMA Output Priority Queue 97 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_96	**QDMA Output Priority Queue 96 Re-Map Selection**

15100E04 **PFC_CFG_68** **PFC QDMA Output Priority ReMap 25** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_103								QDMA_OUT_PRI_Q_102							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_101								QDMA_OUT_PRI_Q_100							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_103	**QDMA Output Priority Queue 103 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_102	**QDMA Output Priority Queue 102 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_101	**QDMA Output Priority Queue 101 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_100	**QDMA Output Priority Queue 100 Re-Map Selection**

15100E08 **PFC_CFG_69** **PFC QDMA Output Priority ReMap 26** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_107								QDMA_OUT_PRI_Q_106							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_105								QDMA_OUT_PRI_Q_104							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_107	**QDMA Output Priority Queue 107 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_106	**QDMA Output Priority Queue 106 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_105	**QDMA Output Priority Queue 105 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_104	**QDMA Output Priority Queue 104 Re-Map Selection**

15100E0C **PFC_CFG_70** **PFC QDMA Output Priority ReMap 27** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_111								QDMA_OUT_PRI_Q_110							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_109								QDMA_OUT_PRI_Q_108							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_111	**QDMA Output Priority Queue 111 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_110	**QDMA Output Priority Queue 110 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_109	**QDMA Output Priority Queue 109 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_108	**QDMA Output Priority Queue 108 Re-Map Selection**

15100E10 PFC_CFG_71 PFC QDMA Output Priority ReMap 28 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_115								QDMA_OUT_PRI_Q_114							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_113								QDMA_OUT_PRI_Q_112							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_115	**QDMA Output Priority Queue 115 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_114	**QDMA Output Priority Queue 114 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_113	**QDMA Output Priority Queue 113 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_112	**QDMA Output Priority Queue 112 Re-Map Selection**

15100E14 **PFC_CFG_72** **PFC QDMA Output Priority ReMap 29** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_119								QDMA_OUT_PRI_Q_118							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_117								QDMA_OUT_PRI_Q_116							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_119	**QDMA Output Priority Queue 119 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_118	**QDMA Output Priority Queue 118 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_117	**QDMA Output Priority Queue 117 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_116	**QDMA Output Priority Queue 116 Re-Map Selection**

15100E18 **PFC_CFG_73** **PFC QDMA Output Priority ReMap 30** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_123								QDMA_OUT_PRI_Q_122							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_121								QDMA_OUT_PRI_Q_120							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_123	**QDMA Output Priority Queue 123 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_122	**QDMA Output Priority Queue 122 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_121	**QDMA Output Priority Queue 121 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_120	**QDMA Output Priority Queue 120 Re-Map Selection**

15100E1C **PFC_CFG_74** **PFC QDMA Output Priority ReMap 31** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_OUT_PRI_Q_127								QDMA_OUT_PRI_Q_126							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_OUT_PRI_Q_125								QDMA_OUT_PRI_Q_124							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	QDMA_OUT_PRI_Q_127	**QDMA Output Priority Queue 127 Re-Map Selection**
23:16	QDMA_OUT_PRI_Q_126	**QDMA Output Priority Queue 126 Re-Map Selection**
15:8	QDMA_OUT_PRI_Q_125	**QDMA Output Priority Queue 125 Re-Map Selection**
7:0	QDMA_OUT_PRI_Q_124	**QDMA Output Priority Queue 124 Re-Map Selection**

15100EA0 **PFC_CFG_75** **PFC Enable Control to GMAC1** **FFFFFF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_GMAC1								EN_WDMA0_GMAC1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_GMAC1								EN_GMAC1_GMAC1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	EN_WDMA1_GMAC1	**Enable Control from WDMA1 to GMAC1**
23:16	EN_WDMA0_GMAC1	**Enable Control from WDMA0 to GMAC1**
15:8	EN_GMAC2_GMAC1	**Enable Control from GMAC2 to GMAC1**
7:0	EN_GMAC1_GMAC1	**Enable Control from GMAC1 to GMAC1**

15100EA4 **PFC_CFG_76** **PFC Enable Control to GMAC1** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**EN_QDMA_GMAC1**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_GMAC1	**Enable Control from QDMA to GMAC1**

15100EA8 **PFC_CFG_77** **PFC Enable Control to GMAC2** **FFFF00FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_GMAC2								EN_WDMA0_GMAC2							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_GMAC2								EN_GMAC1_GMAC2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_GMAC2	**Enable Control from WDMA1 to GMAC2**
23:16	EN_WDMA0_GMAC2	**Enable Control from WDMA0 to GMAC2**
15:8	EN_GMAC2_GMAC2	**Enable Control from GMAC2 to GMAC2**
7:0	EN_GMAC1_GMAC2	**Enable Control from GMAC1 to GMAC2**

15100EAC **PFC_CFG_78** **PFC Enable Control to GMAC2** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EN_QDMA_GMAC2							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_GMAC2	**Enable Control from QDMA to GMAC2**

15100EB0 **PFC_CFG_79** **PFC Enable Control to WDMA0** **FF00FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_WDMA0								EN_WDMA0_WDMA0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_WDMA0								EN_GMAC1_WDMA0							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_WDMA0	**Enable Control from WDMA1 to WDMA0**
23:16	EN_WDMA0_WDMA0	**Enable Control from WDMA0 to WDMA0**
15:8	EN_GMAC2_WDMA0	**Enable Control from GMAC2 to WDMA0**
7:0	EN_GMAC1_WDMA0	**Enable Control from GMAC1 to WDMA0**

15100EB4 **PFC_CFG_80** **PFC Enable Control to WDMA0** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EN_QDMA_WDMA0							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_WDMA0	**Enable Control from QDMA to WDMA0**

15100EB8 PFC_CFG_81 PFC Enable Control to WDMA1 00FFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_WDMA1								EN_WDMA0_WDMA1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_WDMA1								EN_GMAC1_WDMA1							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_WDMA1	**Enable Control from WDMA1 to WDMA1**
23:16	EN_WDMA0_WDMA1	**Enable Control from WDMA0 to WDMA1**
15:8	EN_GMAC2_WDMA1	**Enable Control from GMAC2 to WDMA1**
7:0	EN_GMAC1_WDMA1	**Enable Control from GMAC1 to WDMA1**

15100EBC **PFC_CFG_82** **PFC Enable Control to WDMA1** **000000FF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**EN_QDMA_WDMA1**							
Type									RW							
Reset									1	1	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	EN_QDMA_WDMA1	**Enable Control from QDMA to WDMA1**

15100EC0 **PFC_CFG_83** **PFC Enable Control to QDMA** **FFFFFFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_WDMA1_QDMA								EN_WDMA0_QDMA							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_GMAC2_QDMA								EN_GMAC1_QDMA							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	EN_WDMA1_QDMA	**Enable Control from WDMA1 to QDMA**
23:16	EN_WDMA0_QDMA	**Enable Control from WDMA0 to QDMA**
15:8	EN_GMAC2_QDMA	**Enable Control from GMAC2 to QDMA**
7:0	EN_GMAC1_QDMA	**Enable Control from GMAC1 to QDMA**

15100EF0 PFC_CFG_85 PFC Debug 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_WDMA1								DEBUG_WDMA0							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_GMAC2								DEBUG_GMAC1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEBUG_WDMA1	**Debug for Output Module: WDMA1**
23:16	DEBUG_WDMA0	**Debug for Output Module: WDMA0**
15:8	DEBUG_GMAC2	**Debug for Output Module: GMAC2** Debug for PFC vector source from MAC/QDMA/WDMA in central; MAC TX will ignore this event in half duplex mode
7:0	DEBUG_GMAC1	**Debug for Output Module: GMAC1** Debug for PFC vector source from MAC/QDMA/WDMA in central; MAC TX will ignore this event in half duplex mode

15100EF4 **PFC_CFG_86** **PFC Debug 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_31_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_31_0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_31_0	**Debug for Output Module: QDMA bit 31~0**

15100EF8 **PFC_CFG_87** **PFC Debug 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_63_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_63_32															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_63_32	**Debug for Output Module: QDMA bit 63~32**

15100EFC **PFC_CFG_88** **PFC Debug 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_95_64															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_95_64															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_95_64	**Debug for Output Module: QDMA bit 95~64**

15100F00 **PFC_CFG_89** **PFC Debug 4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_QDMA_127_96															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEBUG_QDMA_127_96															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DEBUG_QDMA_127_96	**Debug for Output Module: QDMA bit 127~96**

15100F04 PFC_CFG_90 PFC Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_IN_PRI_PAGE_WR	QDMA_IN_PRI_PAGE_SEL			QDMA_OUT_PRI_PAGE_WR	QDMA_OUT_PRI_PAGE_SEL								STATUS_UPDATE_PERIOD_SEL		
Type	RW	RW			RW	RW								RW		
Reset	0	0	0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description
15	QDMA_IN_PRI_PAGE_WR	**Enable QDMA Input Priority Page Write** 0: Disable 1: Enable
14:12	QDMA_IN_PRI_PAGE_SEL	**QDMA Input Priority Page Selection** It will latch input priority remap setting (PFC_CFG_5~PFC_CFG_36) to selected page when QDMA_IN_PRI_PAGE_WR = 1. It will be read back into PFC_CFG_5~PFC_CFG_36 according to selected source when QDMA_IN_PRI_PAGE_WR = 0. 3'b000: GMAC1 3'b001: GMAC2 3'b010: WDMA0 3'b011: WDMA1 3'b100 ~ 3'b111: Reserved
11	QDMA_OUT_PRI_PAGE_WR	**Enable QDMA Output Priority Page Write** 0: Disable 1: Enable
10:8	QDMA_OUT_PRI_PAGE_SEL	**QDMA Output Priority Page Selection** It will latch output priority remap setting (PFC_CFG_43~PFC_CFG_74) to selected page when QDMA_OUT_PRI_PAGE_WR = 1. It will be read back into PFC_CFG_43~PFC_CFG_74 according to selected source when QDMA_OUT_PRI_PAGE_WR = 0. 3'b000: GMAC1 3'b001: GMAC2 3'b010: WDMA0 3'b011: WDMA1

Bit(s)	Name	Description
		3'b100 ~ 3'b111: Reserved
2:0	STATUS_UPDATE_PERIOD_SEL	**Status Update Period Selection** 3'b000: Bypass 3'b001: 1us 3'b010: 20us 3'b011: 125us 3'b100: 1ms

15101400 CDMQ_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															UNTAG_EN	STAG_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
1	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.

15101404 CDMQ_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15101408 CDMQ_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

15101500 GDM2_IG_CTRL GDM Ingress Control 20717777

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0						INSV_EN	STAG_EN		GDM_ICS_EN	GDM_TCS_EN	GDM_UCS_EN	DROP_256B			STRP_CRC
Type	RW						RW	RW		RW	RW	RW	RW			RW
Reset	0	0	1	0			0	0		1	1	1	0			1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MYMAC_DP				BC_DP				MC_DP				UN_DP			
Type	RW				RW				RW				RW			
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Bit(s)	Name	Description
31:28	REV0	**Reserved**
25	INSV_EN	**VLAN insertion** Insert Port VID on the received packets on the corresponding GDM port. 0: Disable 1: Insert 4-byte VLAN tag after Source Address
24	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from GDM port. 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.
22	GDM_ICS_EN	**IPv4 header checksum error drop** 0: Checksum error status reported on RX descriptor (IP4F) 1: Checksum error packet will be dropped
21	GDM_TCS_EN	**TCP checksum error drop** 0: Checksum error status reported on RX descriptor (L4F) 1: Checksum error packet will be dropped
20	GDM_UCS_EN	**UDP checksum error drop** 0: Checksum error status reported on RX descriptor (L4F) 1: Checksum error packet will be dropped
19	DROP_256B	**A special mode to drop packets with payload > 256 bytes** 1'b0: Drop packets according to the standard Ethernet frame length limitation. 1'b1: Drop packets with payload > 256 bytes
16	STRP_CRC	**GDM RX CRC Stripping** 1'b: Disable GDM RX CRC stripping

Bit(s)	Name	Description
		1'b1: Enable GDM RX CRC stripping
15:12	MYMAC_DP	**MY_MAC frames destination port** 4'b0000: ADMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: PPE0 4'b0100: PPE1 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1000: WDMA0 4'b1001: WDMA1 4'b1010: MDMA 4'b1011: EDMA0 4'b1100: EDMA1
11:8	BC_DP	**Broadcast frame destination port** 4'b0000: ADMA 4'b0001: GDM1 4'b0010: GDM2 4'b0011: PPE0 4'b0100: PPE1 4'b0101: QDMA 4'b0110: Reserved 4'b0111: Discard 4'b1000: WDMA0 4'b1001: WDMA1 4'b1010: MDMA 4'b1011: EDMA0 4'b1100: EDMA1
7:4	MC_DP	**Multicast frame destination port** 4'b0000: ADMA 4'b0001: GDM1

Bit(s)	Name	Description
		4'b0010: GDM2
		4'b0011: PPE0
		4'b0100: PPE1
		4'b0101: QDMA
		4'b0110: Reserved
		4'b0111: Discard
		4'b1000: WDMA0
		4'b1001: WDMA1
		4'b1010: MDMA
		4'b1011: EDMA0
		4'b1100: EDMA1
3:0	UN_DP	**Other frame destination port**
		4'b0000: ADMA
		4'b0001: GDM1
		4'b0010: GDM2
		4'b0011: PPE0
		4'b0100: PPE1
		4'b0101: QDMA
		4'b0110: Reserved
		4'b0111: Discard
		4'b1000: WDMA0
		4'b1001: WDMA1
		4'b1010: MDMA
		4'b1011: EDMA0
		4'b1100: EDMA1

15101504 GDM2_EG_CTRL GDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		UNTAG_EN	DIS_PAD	DIS_CRC				SHPR_EN	BK_SIZE							
Type		RW	RW	RW				RW	RW							
Reset		0	0	0				0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TK_TICK		TK_RATE													
Type	RW		RW													
Reset	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
30	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from GDM. 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged
29	DIS_PAD	**GMAC TX padding function** 1'b0: Enable GMAC TX padding 1'b1: Disable GMAC TX padding
28	DIS_CRC	**GMAC TX CRC generation** 1'b0: Enable GMAC TX CRC generation 1'b1: Disable GMAC TX CRC generation
24	SHPR_EN	**Enable GDM output shaper** 1'b0: Disable 1'b1: Enable
23:16	BK_SIZE	**GDM output shaper bucket size.** This unit is 1K-byte
15	TK_TICK	**GDM shaper token period** 1'b0: GDM shaper add token every 1ms 1'b1: GDM shaper add token every 20us
13:0	TK_RATE	**GDM output shaper token rate** The unit is 8-byte/ms or 8-byte/20us according to TK_TICK.

15101508 GDM2_MAC_LSB GDM MY_MAC Address LSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MAC_ADR	**MY_MAC Address [31:0]**

1510150C GDM2_MAC_MSB GDM MY_MAC Address MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAC_ADR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	MAC_ADR	**MY_MAC Address [47:32]**

15101510 GDM2_VLAN_GEN GDM VLAN Generation 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM_PRI			GDM_CFI	GDM_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	GDM_TPID	**Inserted VLAN TPID**
15:13	GDM_PRI	**Inserted PRI**
12	GDM_CFI	**Inserted CFI**
11:0	GDM_VID	**Inserted VLAN ID**

15101514 GDM2_FILTER_CRTL GDM Filter Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**GDM_VIDF_EN**	**GMD_HASH_ALG**	**GDM_DAF_MODE**	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	GDM_VIDF_EN	**Enable GDM VLAN ID filter**
2	GMD_HASH_ALG	**Hash Algorithm setting** 0: Direct map - Using DA40 and DA 7~0 as Hash Key. Receive packet if corresponding bit is set. 1: CRC32 - Using 32-bit CRC bit 8~0 of DA as hash key. Receive packet if corresponding bit is set.
1:0	GDM_DAF_MODE	**Receive packet with DA Filter function** 0: Promiscuous mode - Receive all packets. 1: Filter packet by MAC_MAC/Broadcast/Hash table 2: Filter packet by MAC_MAC/Broadcast 3: Reserved

15101518 GDM2_VIDF01 GDM VID Filter Control 01 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID1_VLD				GDM2_VID1											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID0_VLD				GDM2_VID0											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID1_VLD	**VLAN ID #1 valid bit**
27:16	GDM2_VID1	**VLAN ID #1**
15	GDM2_VID0_VLD	**VLAN ID #0 valid bit**
11:0	GDM2_VID0	**VLAN ID #0**

1510151C GDM2_VIDF23 GDM VID Filter Control 23 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GDM2_VID3_VLD				GDM2_VID3											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GDM2_VID2_VLD				GDM2_VID2											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	GDM2_VID3_VLD	**VLAN ID #3 valid bit**
27:16	GDM2_VID3	**VLAN ID #3**
15	GDM2_VID2_VLD	**VLAN ID #2 valid bit**
11:0	GDM2_VID2	**VLAN ID #2**

15101520 GDM2_DOS_CFG_0 GDM DOS Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPD_2P5G_MODE	ICMP_AND_TOS_EQ_ZERO	MY_MAC_CHECK						TCP_DROP_INT_STATUS	TCP_RATE_LIMITER_RST	TCP_DROP_INT_EN	TCP_SYN_PKT_DROP_EN	TCP_SYN_LIMIT_MODE	TCP_SYN_LIMIT_UNIT		
Type	RW	RW	RW						W1C	RW	RW	RW	RW	RW		
Reset	0	0	0						0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DROP_INT_STATUS	UDP_RATE_LIMITER_RST	UDP_DROP_INT_EN	UDP_PKT_DROP_EN	UDP_LIMIT_MODE	UDP_LIMIT_UNIT			ICMP_DROP_INT_STATUS	ICMP_RATE_LIMITER_RST	ICMP_DROP_INT_EN	ICMP_PKT_DROP_EN	ICMP_LIMIT_MODE	ICMP_LIMIT_UNIT		
Type	W1C	RW	RW	RW	RW	RW			W1C	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	SPD_2P5G_MODE	**Reference *_LIMIT_2P5G Setting for Rate Limitation** 1'b0: Disable 1'b1: Enable
30	ICMP_AND_TOS_EQ_ZERO	**IPv4 ICMP Packet Recognition Control** 1'b0: Ignore TOS field of IPv4 header; only check if PROTOCOL field equals 1 to regard it as IPv4 ICMP packet 1'b1: It will also check if TOS field equals 0 besides checking if PROTOCOL field equals 1
29	MY_MAC_CHECK	**MY MAC Address Check Control** 1'b0: Ignore DA checking of incoming packet involved in rate limit mechanism directly 1'b1: It will check DA of incoming packet to see whether it equals MY_MAC address. If YES, given packet will be involved in rate limit mechanism; otherwise, pass this packet directly.
23	TCP_DROP_INT_STATUS	**TCP Packet Drop Interrupt Event Status** 1'b0: No interrupt 1'b1: Interrupt event trigger
22	TCP_RATE_LIMITER_RST	**TCP Rate Limiter Reset Control** 1'b0: Reset asserted 1'b1: Reset de-asserted
21	TCP_DROP_INT_EN	**TCP Packet Drop Interrupt Event Control** 1'b0: Disable interrupt event to final interrupt 1'b1: Enable interrupt event to final interrupt
20	TCP_SYN_PKT_DROP_EN	**TCP SYN Packet Drop Control when Reaching Rate Limitation**

Bit(s)	Name	Description
		1'b0: No packet drop
		1'b1: Packet drop for the following TCP SYN packet
19	TCP_SYN_LIMIT_MODE	**TCP SYN Rate Limitation Mode**
		1'b0: Packet-based (1 second period)
		1'b1: Rate-based
18:16	TCP_SYN_LIMIT_UNIT	**Unit of TCP SYN Rate Limitation**
		3'b000: 64 packets or 64 Kbps
		3'b001: 256 packets or 256 Kbps
		3'b010: 1 K packets or 1 Mbps
		3'b011: 4 K packets or 4 Mbps
		3'b1XX: 16 K packets or 16 Mbps
15	UDP_DROP_INT_STATUS	**UDP Packet Drop Interrupt Event Status**
		1'b0: No interrupt
		1'b1: Interrupt event trigger
14	UDP_RATE_LIMITER_RST	**UDP Rate Limiter Reset Control**
		1'b0: Reset asserted
		1'b1: Reset de-asserted
13	UDP_DROP_INT_EN	**UDP Packet Drop Interrupt Event Control**
		1'b0: Disable interrupt event to final interrupt
		1'b1: Enable interrupt event to final interrupt
12	UDP_PKT_DROP_EN	**UDP Packet Drop Control when Reaching Rate Limitation**
		1'b0: No packet drop
		1'b1: Packet drop for the following UDP packet
11	UDP_LIMIT_MODE	**UDP Rate Limitation Mode**
		1'b0: Packet-based (1 second period)
		1'b1: Rate-based
10:8	UDP_LIMIT_UNIT	**Unit of UDP Rate Limitation**
		3'b000: 64 packets or 64 Kbps
		3'b001: 256 packets or 256 Kbps
		3'b010: 1 K packets or 1 Mbps
		3'b011: 4 K packets or 4 Mbps
		3'b1XX: 16 K packets or 16 Mbps

Bit(s)	Name	Description
7	ICMP_DROP_INT_STATUS	**ICMP Packet Drop Interrupt Event Status** 1'b0: No interrupt 1'b1: Interrupt event trigger
6	ICMP_RATE_LIMITER_RST	**ICMP Rate Limiter Reset Control** 1'b0: Reset asserted 1'b1: Reset de-asserted
5	ICMP_DROP_INT_EN	**ICMP Packet Drop Interrupt Event Control** 1'b0: Disable interrupt event to final interrupt 1'b1: Enable interrupt event to final interrupt
4	ICMP_PKT_DROP_EN	**ICMP Packet Drop Control when Reaching Rate Limitation** 1'b0: No packet drop 1'b1: Packet drop for the following ICMP packet
3	ICMP_LIMIT_MODE	**ICMP Rate Limitation Mode** 1'b0: Packet-based (1 second period) 1'b1: Rate-based
2:0	ICMP_LIMIT_UNIT	**Unit of ICMP Rate Limitation** 3'b000: 64 packets or 64 Kbps 3'b001: 256 packets or 256 Kbps 3'b010: 1 K packets or 1 Mbps 3'b011: 4 K packets or 4 Mbps 3'b1XX: 16 K packets or 16 Mbps

15101524 GDM2_DOS_CFG_1 GDM DOS Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TCP_SYN_LIMIT_2P5G								TCP_SYN_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TCP_SYN_LIMIT_100M								TCP_SYN_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TCP_SYN_LIMIT_2P5G	**2500 Mbps TCP_SYN Rate Limit Control** The TCP_SYN rate limit for 2500 Mbps link speed 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps
23:16	TCP_SYN_LIMIT_1G	**1000 Mbps TCP_SYN Rate Limit Control** The TCP_SYN rate limit for 1000 Mbps link speed 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps
15:8	TCP_SYN_LIMIT_100M	**100 Mbps TCP_SYN Rate Limit Control** The TCP_SYN rate limit for 100 Mbps link speed 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps
7:0	TCP_SYN_LIMIT_10M	**10 Mbps TCP_SYN Rate Limit Control** The TCP_SYN rate limit for 10 Mbps link speed 8'h0: (0* TCP_SYN_LIMIT_UNIT) packets or bps 8'h1: (1* TCP_SYN_LIMIT_UNIT) packets or bps

15101528 GDM2_DOS_CFG_2 GDM DOS Configuration 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_LIMIT_2P5G								UDP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_LIMIT_100M								UDP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	UDP_LIMIT_2P5G	**2500 Mbps UDP Rate Limit Control** The UDP rate limit for 2500 Mbps link speed 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps
23:16	UDP_LIMIT_1G	**1000 Mbps UDP Rate Limit Control** The UDP rate limit for 1000 Mbps link speed 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps
15:8	UDP_LIMIT_100M	**100 Mbps UDP Rate Limit Control** The UDP rate limit for 100 Mbps link speed 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps
7:0	UDP_LIMIT_10M	**10 Mbps UDP Rate Limit Control** The UDP rate limit for 10 Mbps link speed 8'h0: (0* UDP_LIMIT_UNIT) packets or bps 8'h1: (1* UDP_LIMIT_UNIT) packets or bps

1510152C GDM2_DOS_CFG_3 GDM DOS Configuration 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ICMP_LIMIT_2P5G								ICMP_LIMIT_1G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ICMP_LIMIT_100M								ICMP_LIMIT_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	ICMP_LIMIT_2P5G	**2500 Mbps ICMP Rate Limit Control** The ICMP rate limit for 2500 Mbps link speed 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps
23:16	ICMP_LIMIT_1G	**1000 Mbps ICMP Rate Limit Control** The ICMP rate limit for 1000 Mbps link speed 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps
15:8	ICMP_LIMIT_100M	**100 Mbps ICMP Rate Limit Control** The ICMP rate limit for 100 Mbps link speed 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps
7:0	ICMP_LIMIT_10M	**10 Mbps ICMP Rate Limit Control** The ICMP rate limit for 10 Mbps link speed 8'h0: (0* ICMP_LIMIT_UNIT) packets or bps 8'h1: (1* ICMP_LIMIT_UNIT) packets or bps

15101530 GDM2_THRES GDM2 Threshold 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB

15101600 CDMW0_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU 0: No special tag inserted. 1: The first 2-byte after Source Address are the special tag.

15101604 CDMW0_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15101608 CDMW0_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

15101610 CDMW1_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.

15101614 CDMW1_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15101618 CDMW1_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

15101620 CDME0_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.

15101624 CDME0_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15101628 CDME0_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

15101630 CDME1_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.

15101634 CDME1_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																UNTAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15101638 CDME1_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

15101640 CDMM_IG_CTRL CDM VLAN Control 81000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CDM_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STAG_EN
Type																RW
Reset																0

Bit(s)	Name	Description
31:16	CDM_TPID	**Inserted VLAN TPID**
0	STAG_EN	**Special tag indication** Indicate that the received packets are carrying the special tag from CPU 0: No special tag inserted. 1: The first 2 bytes after Source Address are the special tag.

15101644 CDMM_EG_CTRL CDM Egress Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**UNTAG_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	UNTAG_EN	**VLAN un-tag** Un-tag the egress packets transmitted from CDM to CPU 0: Disable 1: The first 4-byte VLAN tag after Source Address will be un-tagged

15101648 CDMM_PPP_GEN CDM PPPoE Generation 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																PPP_INS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SESS_ID															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	PPP_INS	**PPPoE Header Insertion**
15:0	SESS_ID	**PPPoE Session ID**

1510164C CDM_THRES0 CDM Threshold 0 08000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					cdma_high_threshold											
Type					RW											
Reset					1	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdmw0_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
27:24	cdma_high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB
3:0	cdmw0_high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB

15101650 CDM_THRES1 CDM Threshold 1 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdmw1_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	cdmw1_high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB

15101654 CDM_THRES2 CDM Threshold 2 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdme0_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	cdme0_high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB

15101658 CDM_THRES3 CDM Threshold 3 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													cdme1_high_threshold			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	cdme1_high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB

1510165C CDM_THRES4 CDM Threshold 4 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**cdmm_high_threshold**			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	cdmm_high_threshold	**Memory high threshold value** Memory size: high_threshold*1KB

15102800 RSS_GLO_CFG RSS Global Configuration 1F1F3370

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IPV4_TUPLE_EN								IPV6_TUPLE_EN				
Type				RW								RW				
Reset				1	1	1	1	1				1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IPV4_TYPE				IPV6_TYPE				INDR_TBL_SIZE			RSS_CFG_RDY	RSS_CFG_REQ	RSS_BUSY	RSS_ENABLE
Type		RW				RW				RW			RO	RW	RO	RW
Reset		0	1	1		0	1	1		1	1	1	0	0	0	0

Bit(s)	Name	Description
28:24	IPV4_TUPLE_EN	**IPv4 Hash Tuple Global Enable** This field controls which hash tuple is valid for IPv4 hash calculation. The invalid (disabled) tuple can be seen as0x0 when calculating HASH. For example, when SIP is disabled, the 2-tuple and 4-tuple hash will not consider SIP. Another example is when DPORT is disabled, the 4-tuple hash will not consider DPORT. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation. 5'b00000: Disable All 5'b00010: Enable SIP for HASH 5'b00100: Enable DIP for HASH 5'b01000: Enable SPORT for HASH 5'b10000: Enable DPORT for HASH 5'b11111: Enable DPORT, SPORT, DIP, SIP for HASH Others: Combinations of the above hash tuple
20:16	IPV6_TUPLE_EN	**IPv6 Hash Tuple Global Enable** This field controls which hash tuple is valid for IPv6 hash calculation. See description of IPV4_TUPLE_EN for more detail. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation. 5'b00000: Disable All

Bit(s)	Name	Description
		5'b00010: Enable SIP for HASH 5'b00100: Enable DIP for HASH 5'b01000: Enable SPORT for HASH 5'b10000: Enable DPORT for HASH 5'b11111: Enable DPORT, SPORT, DIP, SIP for HASH Others: Combinations of the above hash tuple
14:12	IPV4_TYPE	**IPv4 Hash Type Selection Flag** This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv4 packets. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} RSS performs the hash calculations as specified for the enabled case. For example, if IPV4_TYPE = 3'b011, RSS will use the 4-tuple hash for IPv4 TCP packets and 2-tuple hash for IPv4 non-TCP packets (such as IPv4 fragment packets). 3'b000: Disable IPv4 packets for RSS. RSS does not accept IPv4 packets 3'b001: Enable IPv4 2-tuple hash 3'b010: Enable TCP 4-tuple hash 3'b100: Enable UDP 4-tuple hash 3'b011: Enable IPv4 2-tuple hash + TCP 4-tuple hash 3'b101: Enable IPv4 2-tuple hash + UDP 4-tuple hash 3'b110: TCP 4-tuple hash + UDP 4-tuple hash 3'b111: IPv4 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash
10:8	IPV6_TYPE	**IPv6 Hash Type Selection Flag** This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv6 packets. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} See description of IPV4_TYPE for more detail. 3'b000: Disable IPv6 packets for RSS. RSS does not accept IPv4 packets 3'b001: Enable IPv6 2-tuple hash 3'b010: Enable TCP 4-tuple hash 3'b100: Enable UDP 4-tuple hash 3'b011: Enable IPv6 2-tuple hash + TCP 4-tuple hash 3'b101: Enable IPv6 2-tuple hash + UDP 4-tuple hash

Bit(s)	Name	Description
		3'b110: TCP 4-tuple hash + UDP 4-tuple hash 3'b111: IPv6 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash
6:4	INDR_TBL_SIZE	**Change the size of indirection table.** This register field affects how many bits of hash result will be used as the entry of indirection table. For example, INDR_TBL_SIZE = 6 means RSS uses only 6 bits of hash result as indirection table entry, which also means that indirection table has 2^6 = 64 entries. 3'd1: Indirection table size = 2 entries 3'd2: Indirection table size = 4 entries 3'd3: Indirection table size = 8 entries 3'd4: Indirection table size = 16 entries 3'd5: Indirection table size = 32 entries 3'd6: Indirection table size = 64 entries 3'd7: Indirection table size = 128 entries Other: Invalid value
3	RSS_CFG_RDY	**RSS is ready to accept new register configuration.** This register will be asserted after RSS accepted the request from RSS_CFG_REQ. See description of RSS_CFG_REQ for more detail. 0: Not Ready 1: Ready
2	RSS_CFG_REQ	**Request to change RSS register configuration.** When request is asserted, RSS will be paused after the process of current packet has finished. Note that assert RSS_CFG_REQ is required before enabling RSS or changing other register setting (such as indirection table). Must wait until RSS_CFG_RDY = 1 before changing RSS register value (including RSS_ENABLE). 0: Deassert request 1: Assert request
1	RSS_BUSY	**RSS is working or not** 0: RSS IDLE 1: RSS BUSY
0	RSS_ENABLE	**Enable/Disable RSS** 0: Disable RSS 1: Enable RSS

Bit(s)	Name	Description

15102820 RSS_HASH_KEY_DW0 RSS Hash Key DW0 BEAC01FA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW0															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	0	1	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW0															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW0	**Hash Key bit 31~0**

15102824 RSS_HASH_KEY_DW1 RSS Hash Key DW1 6A42B73B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW1															
Type	RW															
Reset	0	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW1															
Type	RW															
Reset	1	0	1	1	0	1	1	1	0	0	1	1	1	0	1	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW1	**Hash Key bit 63~32**

15102828 RSS_HASH_KEY_DW2 RSS Hash Key DW2 8030F20C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW2															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW2															
Type	RW															
Reset	1	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW2	**Hash Key bit 95~64**

1510282C RSS_HASH_KEY_DW3 RSS Hash Key DW3 77CB2DA3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW3															
Type	RW															
Reset	0	1	1	1	0	1	1	1	1	1	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW3															
Type	RW															
Reset	0	0	1	0	1	1	0	1	1	0	1	0	0	0	1	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW3	**Hash Key bit 127~96**

15102830 RSS_HASH_KEY_DW4 RSS Hash Key DW4 AE7B30B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW4															
Type	RW															
Reset	1	0	1	0	1	1	1	0	0	1	1	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW4															
Type	RW															
Reset	0	0	1	1	0	0	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW4	**Hash Key bit 159~128**

15102834 RSS_HASH_KEY_DW5 RSS Hash Key DW5 D0CA2BCB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW5															
Type	RW															
Reset	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW5															
Type	RW															
Reset	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW5	**Hash Key bit 191~160**

15102838 RSS_HASH_KEY_DW6 RSS Hash Key DW6 43A38FB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW6															
Type	RW															
Reset	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW6															
Type	RW															
Reset	1	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW6	**Hash Key bit 223~192**

1510283C RSS_HASH_KEY_DW7 RSS Hash Key DW7 4167253D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW7															
Type	RW															
Reset	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW7															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	0	1	1	1	1	0	1

Bit(s)	Name	Description
31:0	HASH_KEY_DW7	**Hash Key bit 255~224**

15102840 RSS_HASH_KEY_DW8 RSS Hash Key DW8 255B0EC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW8															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	1	0	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW8															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW8	**Hash Key bit 287~256**

15102844 RSS_HASH_KEY_DW9 RSS Hash Key DW9 6D5A56DA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_KEY_DW9															
Type	RW															
Reset	0	1	1	0	1	1	0	1	0	1	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_KEY_DW9															
Type	RW															
Reset	0	1	0	1	0	1	1	0	1	1	0	1	1	0	1	0

Bit(s)	Name	Description
31:0	HASH_KEY_DW9	**Hash Key bit 319~288**

15102848 RSS_LFB_CFG0 RSS Low Flow Balance Configuration 0 00C7FF02

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TICK_TIMER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_TIMER													CMP_TCP_UDP	CMP_IPV4_IPV6	EN
Type	RW													RW	RW	RW
Reset	1	1	1	1	1	1	1	1						0	1	0

Bit(s)	Name	Description
31:16	TICK_TIMER	**Low Flow Balance Table Age Tick Timer** An internal generated timeout timer based on 20us tick time. When timeout occurs, it will trigger a tick to age timer to count forward. If set to zero: tick timer is disabled and the trigger of age timer is the copy of raw 20us tick instead.
15:8	AGE_TIMER	**Low Flow Balance Table Age Timer** Entry ageout timer of low flow balance table. The applied age out timer is equal to (AGE_TIMER+1)*(TICK_TIMER)*20us
2	CMP_TCP_UDP	**Low Flow Balance Table TCP/UDP Flow Compare** When enabled, TCP flow and UDP flow will be seen as different flows even if they have the same DPORT and SPORT. 0: Disable 1: Enable
1	CMP_IPV4_IPV6	**Low Flow Balance Table IPv4/IPv6 Flow Compare** When enabled, IPv4 flow and IPv6 flow will be seen as different flow even if the flow has same DIP and SIP. 0: Disable 1: Enable
0	EN	**Enable Low Flow Balance Table** 0: Disable 1: Enable

15102850 RSS_INDR_TABLE_DW0 RSS Indirection Table DW0 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW0															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW0															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW0	**Indirection Table Entry 15~0** Each entry has 2 bits

15102854 RSS_INDR_TABLE_DW1 RSS Indirection Table DW1 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW1															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW1															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW1	**Indirection Table Entry 31~16** Each entry has 2 bits

15102858 RSS_INDR_TABLE_DW2 RSS Indirection Table DW2 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW2															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW2															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW2	**Indirection Table Entry 47~32** Each entry has 2 bits

1510285C RSS_INDR_TABLE_DW3 RSS Indirection Table DW3 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW3															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW3															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW3	**Indirection Table Entry 63~48** Each entry has 2 bits

15102860 RSS_INDR_TABLE_DW4 RSS Indirection Table DW4 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW4															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW4															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW4	**Indirection Table Entry 79~64** Each entry has 2 bits

15102864 RSS_INDR_TABLE_DW5 RSS Indirection Table DW5 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW5															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW5															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW5	**Indirection Table Entry 95~80** Each entry has 2 bits

15102868 RSS_INDR_TABLE_DW6 RSS Indirection Table DW6 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW6															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW6															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW6	**Indirection Table Entry 111~96** Each entry has 2 bits

1510286C RSS_INDR_TABLE_DW7 RSS Indirection Table DW7 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INDR_TABLE_DW7															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDR_TABLE_DW7															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	INDR_TABLE_DW7	**Indirection Table Entry 127~112** Each entry has 2 bits

5.3 QDMA

5.3.1 Register Definition

Module name: QDMA Base address: (+0x15104400)

Address	Name	Width	Register Function
15104400	QTX_CFG_0	32	TX Queue #0, #(16 * n) Configuration
15104404	QTX_SCH_0	32	TX Queue #0, #(16 * n) Schedule
15104408	QTX_HEAD_0	32	TX Queue #0, #(16 * n) Head Pointer
1510440C	QTX_TAIL_0	32	TX Queue #0, #(16 * n) Tail Pointer
15104410	QTX_CFG_1	32	TX Queue #1, #(16 * n + 1) Configuration
15104414	QTX_SCH_1	32	TX Queue #1, #(16 * n + 1) Schedule
15104418	QTX_HEAD_1	32	TX Queue #1, #(16 * n + 1) Head Pointer
1510441C	QTX_TAIL_1	32	TX Queue #1, #(16 * n + 1) Tail Pointer
15104420	QTX_CFG_2	32	TX Queue #2, #(16 * n + 2) Configuration
15104424	QTX_SCH_2	32	TX Queue #2, #(16 * n + 2) Schedule
15104428	QTX_HEAD_2	32	TX Queue #2, #(16 * n + 2) Head Pointer
1510442C	QTX_TAIL_2	32	TX Queue #2, #(16 * n + 2) Tail Pointer
15104430	QTX_CFG_3	32	TX Queue #3, #(16 * n + 3) Configuration
15104434	QTX_SCH_3	32	TX Queue #3, #(16 * n + 3) Schedule
15104438	QTX_HEAD_3	32	TX Queue #3, #(16 * n + 3) Head Pointer
1510443C	QTX_TAIL_3	32	TX Queue #3, #(16 * n + 3) Tail Pointer
15104440	QTX_CFG_4	32	TX Queue #4, #(16 * n + 4) Configuration
15104444	QTX_SCH_4	32	TX Queue #4, #(16 * n + 4) Schedule
15104448	QTX_HEAD_4	32	TX Queue #4, #(16 * n + 4) Head Pointer
1510444C	QTX_TAIL_4	32	TX Queue #4, #(16 * n + 4) Tail Pointer
15104450	QTX_CFG_5	32	TX Queue #5, #(16 * n + 5) Configuration
15104454	QTX_SCH_5	32	TX Queue #5, #(16 * n + 5) Schedule
15104458	QTX_HEAD_5	32	TX Queue #5, #(16 * n + 5) Head Pointer
1510445C	QTX_TAIL_5	32	TX Queue #5, #(16 * n + 5) Tail Pointer
15104460	QTX_CFG_6	32	TX Queue #6, #(16 * n + 6) Configuration
15104464	QTX_SCH_6	32	TX Queue #6, #(16 * n + 6) Schedule
15104468	QTX_HEAD_6	32	TX Queue #6, #(16 * n + 6) Head Pointer
1510446C	QTX_TAIL_6	32	TX Queue #6, #(16 * n + 6) Tail Pointer
15104470	QTX_CFG_7	32	TX Queue #7, #(16 * n + 7) Configuration
15104474	QTX_SCH_7	32	TX Queue #7, #(16 * n + 7) Schedule
15104478	QTX_HEAD_7	32	TX Queue #7, #(16 * n + 7) Head Pointer
1510447C	QTX_TAIL_7	32	TX Queue #7, #(16 * n + 7) Tail Pointer
15104480	QTX_CFG_8	32	TX Queue #8, #(16 * n + 8) Configuration
15104484	QTX_SCH_8	32	TX Queue #8, #(16 * n + 8) Schedule
15104488	QTX_HEAD_8	32	TX Queue #8, #(16 * n + 8) Head Pointer
1510448C	QTX_TAIL_8	32	TX Queue #8, #(16 * n + 8) Tail Pointer
15104490	QTX_CFG_9	32	TX Queue #9, #(16 * n + 9) Configuration
15104494	QTX_SCH_9	32	TX Queue #9, #(16 * n + 9) Schedule
15104498	QTX_HEAD_9	32	TX Queue #9, #(16 * n + 9) Head Pointer
1510449C	QTX_TAIL_9	32	TX Queue #9, #(16 * n + 9) Tail Pointer
151044A0	QTX_CFG_10	32	TX Queue #10, #(16 * n + 10) Configuration
151044A4	QTX_SCH_10	32	TX Queue #10, #(16 * n + 10) Schedule
151044A8	QTX_HEAD_10	32	TX Queue #10, #(16 * n + 10) Head Pointer
151044AC	QTX_TAIL_10	32	TX Queue #10, #(16 * n + 10) Tail Pointer
151044B0	QTX_CFG_11	32	TX Queue #11, #(16 * n + 11) Configuration
151044B4	QTX_SCH_11	32	TX Queue #11, #(16 * n + 11) Schedule
151044B8	QTX_HEAD_11	32	TX Queue #11, #(16 * n + 11) Head Pointer

Address	Name	Width	Register Function
151044BC	QTX_TAIL_11	32	TX Queue #11, #(16 * n + 11) Tail Pointer
151044C0	QTX_CFG_12	32	TX Queue #12, #(16 * n + 12) Configuration
151044C4	QTX_SCH_12	32	TX Queue #12, #(16 * n + 12) Schedule
151044C8	QTX_HEAD_12	32	TX Queue #12, #(16 * n + 12) Head Pointer
151044CC	QTX_TAIL_12	32	TX Queue #12, #(16 * n + 12) Tail Pointer
151044D0	QTX_CFG_13	32	TX Queue #13, #(16 * n + 13) Configuration
151044D4	QTX_SCH_13	32	TX Queue #13, #(16 * n + 13) Schedule
151044D8	QTX_HEAD_13	32	TX Queue #13, #(16 * n + 13) Head Pointer
151044DC	QTX_TAIL_13	32	TX Queue #13, #(16 * n + 13) Tail Pointer
151044E0	QTX_CFG_14	32	TX Queue #14, #(16 * n + 14) Configuration
151044E4	QTX_SCH_14	32	TX Queue #14, #(16 * n + 14) Schedule
151044E8	QTX_HEAD_14	32	TX Queue #14, #(16 * n + 14) Head Pointer
151044EC	QTX_TAIL_14	32	TX Queue #14, #(16 * n + 14) Tail Pointer
151044F0	QTX_CFG_15	32	TX Queue #15, #(16 * n + 15) Configuration
151044F4	QTX_SCH_15	32	TX Queue #15, #(16 * n + 15) Schedule
151044F8	QTX_HEAD_15	32	TX Queue #15, #(16 * n + 15) Head Pointer
151044FC	QTX_TAIL_15	32	TX Queue #15, #(16 * n + 15) Tail Pointer
15104500	QRX_BASE_PTR_0	32	RX Ring #0 Base Pointer
15104504	QRX_MAX_CNT_0	32	RX Ring #0 Maximum Count
15104508	QRX_CRX_IDX_0	32	RX Ring #0 CPU Pointer
1510450C	QRX_DRX_IDX_0	32	RX Ring #0 DMA Pointer
15104580	VQTX_TB_BASE_0	32	TX Virtual Queue Table #0 Base Address
15104584	VQTX_TB_BASE_1	32	TX Virtual Queue Table #1 Base Address
15104588	VQTX_TB_BASE_2	32	TX Virtual Queue Table #2 Base Address
1510458C	VQTX_TB_BASE_3	32	TX Virtual Queue Table #3 Base Address
15104590	VQTX_TB_BASE_4	32	TX Virtual Queue Table #4 Base Address
15104594	VQTX_TB_BASE_5	32	TX Virtual Queue Table #5 Base Address
15104598	VQTX_TB_BASE_6	32	TX Virtual Queue Table #6 Base Address
1510459C	VQTX_TB_BASE_7	32	TX Virtual Queue Table #7 Base Address
151045F0	QDMA_PAGE	32	QDMA Configuration Page
15104600	QDMA_INFO	32	QDMA Information
15104604	QDMA_GLO_CFG	32	QDMA Global Configuration
15104608	QDMA_RST_IDX	32	QDMA Reset Index
1510460C	QDMA_DELAY_INT	32	Delay Interrupt Configuration
15104610	QDMA_FC_THRES	32	Flow Control Threshold
15104614	QDMA_FC_MODE	32	QDMA Flow Control Mode
15104618	QDMA_INT_STS	32	Interrupt Status
1510461C	QDMA_INT_MASK	32	Interrupt Mask
15104620	QDMA_INT_GRP1	32	QDMA Interrupt Group 1 Control
15104624	QDMA_INT_GRP2	32	QDMA Interrupt Group 2 Control
15104628	QDMA_DROP_PREC	32	QDMA Drop by FFA Percentage Control
15104640	QDMA_HRED1	32	QDMA HW RED Distribution - I
15104644	QDMA_HRED2	32	QDMA HW RED Distribution - II
15104648	QDMA_SRED1	32	QDMA SW RED Distribution - I
1510464C	QDMA_SRED2	32	QDMA SW RED Distribution - II
15104670	QDMA_INT_STS_G0	32	QDMA Interrupt Status Group 0
15104674	QDMA_INT_STS_G1	32	QDMA Interrupt Status Group 1
15104678	QDMA_INT_STS_G2	32	QDMA Interrupt Status Group 2
15104680	VQTX_GLO	32	TX Virtual Queue Global Configuration
1510468C	VQTX_INVLD_PTR	32	TX Virtual Queue Invalid Pointer
15104690	VQTX_NUM	32	Number of TX Virtual Queue Configuration
15104698	VQTX_SCH	32	TX Virtual Queue Schedule Configuration
151046A0	VQTX_HASH_CFG	32	TX Virtual Queue Hash Configuration
151046A4	VQTX_HASH_SD	32	TX Virtual Queue Hash Seed

Address	Name	Width	Register Function
151046B0	VQTX_VLD_CFG	32	TX Virtual Queue Valid Configuration
151046BC	QTX_MIB_IF	32	TX Queue MIB Interface
151046C0	VQTX_MIB_PCNT	32	TX Virtual Queue MIB Packet Count
151046C4	VQTX_MIB_BCNTL	32	TX Virtual Queue MIB Byte Count Low Bytes
151046C8	VQTX_MIB_BCNTH	32	TX Virtual Queue MIB Byte Count High Bytes
151046CC	VQTX_MIB_DPCNT	32	TX Virtual Queue MIB Drop Packet Count
151046D0	QTX_MIB_PCNT	32	TX Physical Queue MIB Forward Packet Count
151046D4	QTX_MIB_DPCNT	32	TX Physical Queue MIB Dropped Packet Count
151046D8	QTX_MIB_BCNTL	32	TX Physical Queue MIB Byte Count Low Bytes
151046DC	QTX_MIB_BCNTH	32	TX Physical Queue MIB Byte Count High Bytes
15104700	QTX_CTX_PTR	32	TX Forward CPU Pointer
15104704	QTX_DTX_PTR	32	TX Forward DMA Pointer
15104708	QTX_FWD_CNT	32	TX Forward DMA Counter
15104710	QTX_CRX_PTR	32	TX Release CPU Pointer
15104714	QTX_DRX_PTR	32	TX Release DMA Pointer
15104718	QTX_RLS_CNT	32	TX Release DMA Counter
15104720	QDMA_FQ_HEAD	32	Free Page Head Pointer
15104724	QDMA_FQ_TAIL	32	Free Page Tail Pointer
15104728	QDMA_FQ_CNT	32	Free Page Counter
1510472C	QDMA_FQ_BLEN	32	Free Page Buffer Length
15104798	QDMA_TX_SCH1_SCH2	32	TX Scheduler1 and Scheduler2 Rate Control
1510479C	QDMA_TX_SCH3_SCH4	32	TX Scheduler3 and Scheduler4 Rate Control
151047C0	VQTX_0_3_BIND_QID	32	QDMA Virtual Queue Group #0~3 to Physical Queue Binding
151047C4	VQTX_4_7_BIND_QID	32	QDMA Virtual Queue Group #4~7 to Physical Queue Binding
151047E0	QTX_FC_SW_STS_0_15	32	TX Queue#0~15 Software Path Flow Control Status
151047EC	QDMA_ULTRA_CFG	32	QDMA AXI ULTRA Configuration
151047F0	QDMA_BUS_CFG	32	QDMA AXI BUS Configuration
151047F4	QDMA_RBUS_CFG	32	QDMA RBUS Configuration
151047F8	QDMA_RBUS_STAT_0	32	R2X Status Register 0
151047FC	QDMA_RBUS_STAT_1	32	R2X Status Register 1

15104400 QTX_CFG_0 TX Queue #0, #(16 * n) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

15104404 QTX_SCH_0 TX Queue #0, #(16 * n) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCH_SEL		BUCKET_DEP		MIN_RATE_EN	MIN_RATE_MAN							MIN_RATE_EXP			
Type	RW		RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_WGHT				MAX_RATE_EN	MAX_RATE_MAN							MAX_RATE_EXP			
Type	RW				RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:30	TX_SCH_SEL	**TX queue on scheduler no.** 0: SCH1 scheduler 1: SCH2 scheduler 2: SCH3 scheduler 3: SCH4 scheduler
29:28	BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3:16KB
27	MIN_RATE_EN	**Enable TX Queue min. rate control** [Note] Rate control is calculated by 125 MHz bus clock. Remember to multiply by a factor when the bus clock is not 125 MHz. 0: Disable. When disabled, shaper will always let the packet pass (infinite rate) 1: Enable min. shaper
26:20	MIN_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** Value range: 0~127
19:16	MIN_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** Value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps)

Bit(s)	Name	Description
		4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps
15:12	MAX_RATE_WGHT	**The weighted value of the WFQ for TX queue # maximum rate.** 0: Weight value = 16 1: Weight value = 1 2: Weight value = 2 n: Weight value = n 15: Weight value = 15
11	MAX_RATE_EN	**Enable TX Queue max. rate control** [Note] Rate control is calculated by 125 MHz bus clock. Remember to multiply by a factor when the bus clock is not 125 MHz. 0: Disable. When disabled, shaper will always let the packet pass (infinite rate) 1: Enable max. shaper
10:4	MAX_RATE_MAN	**Mantissa part of the max. rate control of the TX queue #** Value range: 0~127
3:0	MAX_RATE_EXP	**Exponent part of the max. rate control of the TX queue #** Value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps) 5: QDMA_RATE_EXP5 (default: 100Mbps) Others: 20'd1, 1Gbps

15104408 QTX_HEAD_0 TX Queue #0, #(16 * n) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510440C QTX_TAIL_0 TX Queue #0, #(16 * n) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104410 QTX_CFG_1 TX Queue #1, #(16 * n + 1) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

15104414 QTX_SCH_1 TX Queue #1, #(16 * n + 1) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104418 QTX_HEAD_1 TX Queue #1, #(16 * n + 1) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510441C QTX_TAIL_1 TX Queue #1, #(16 * n + 1) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104420 QTX_CFG_2 TX Queue #2, #(16 * n + 2) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES.
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES.

15104424 QTX_SCH_2 TX Queue #2, #(16 * n + 2) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104428 QTX_HEAD_2 TX Queue #2, #(16 * n + 2) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510442C QTX_TAIL_2 TX Queue #2, #(16 * n + 2) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104430 QTX_CFG_3 TX Queue #3, #(16 * n + 3) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104434 QTX_SCH_3 TX Queue #3, #(16 * n + 3) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104438 QTX_HEAD_3 TX Queue #3, #(16 * n + 3) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510443C QTX_TAIL_3 TX Queue #3, #(16 * n + 3) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104440 QTX_CFG_4 TX Queue #4, #(16 * n + 4) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104444 QTX_SCH_4 TX Queue #4, #(16 * n + 4) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104448 QTX_HEAD_4 TX Queue #4, #(16 * n + 4) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510444C QTX_TAIL_4 TX Queue #4, #(16 * n + 4) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104450 QTX_CFG_5 TX Queue #5, #(16 * n + 5) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104454 QTX_SCH_5 TX Queue #5, #(16 * n + 5) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104458 QTX_HEAD_5 TX Queue #5, #(16 * n + 5) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510445C **QTX_TAIL_5** **TX Queue #5, #(16 * n + 5) Tail Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104460 QTX_CFG_6 TX Queue #6, #(16 * n + 6) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104464 QTX_SCH_6 TX Queue #6, #(16 * n + 6) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104468 QTX_HEAD_6 TX Queue #6, #(16 * n + 6) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510446C QTX_TAIL_6 TX Queue #6, #(16 * n + 6) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104470 QTX_CFG_7 TX Queue #7, #(16 * n + 7) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104474 QTX_SCH_7 TX Queue #7, #(16 * n + 7) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104478 QTX_HEAD_7 TX Queue #7, #(16 * n + 7) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510447C **QTX_TAIL_7** **TX Queue #7, #(16 * n + 7) Tail Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104480 QTX_CFG_8 TX Queue #8, #(16 * n + 8) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104484 QTX_SCH_8 TX Queue #8, #(16 * n + 8) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104488 QTX_HEAD_8 TX Queue #8, #(16 * n + 8) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510448C QTX_TAIL_8 TX Queue #8, #(16 * n + 8) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104490 QTX_CFG_9 TX Queue #9, #(16 * n + 9) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

15104494 QTX_SCH_9 TX Queue #9, #(16 * n + 9) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

15104498 QTX_HEAD_9 TX Queue #9, #(16 * n + 9) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

1510449C QTX_TAIL_9 TX Queue #9, #(16 * n + 9) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

151044A0 **QTX_CFG_10** **TX Queue #10, #(16 * n + 10) Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

151044A4 QTX_SCH_10 TX Queue #10, #(16 * n + 10) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

151044A8 QTX_HEAD_10 TX Queue #10, #(16 * n + 10) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

151044AC **QTX_TAIL_10** **TX Queue #10, #(16 * n + 10) Tail Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

151044B0 QTX_CFG_11 TX Queue #11, #(16 * n + 11) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

151044B4 QTX_SCH_11 TX Queue #11, #(16 * n + 11) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

151044B8 QTX_HEAD_11 TX Queue #11, #(16 * n + 11) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

151044BC **QTX_TAIL_11** **TX Queue #11, #(16 * n + 11) Tail Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

151044C0 QTX_CFG_12 TX Queue #12, #(16 * n + 12) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

151044C4 QTX_SCH_12 TX Queue #12, #(16 * n + 12) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

151044C8 QTX_HEAD_12 TX Queue #12, #(16 * n + 12) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

151044CC QTX_TAIL_12 TX Queue #12, #(16 * n + 12) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

151044D0 QTX_CFG_13 TX Queue #13, #(16 * n + 13) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

151044D4 QTX_SCH_13 TX Queue #13, #(16 * n + 13) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

151044D8 QTX_HEAD_13 TX Queue #13, #(16 * n + 13) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

151044DC QTX_TAIL_13 TX Queue #13, #(16 * n + 13) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

151044E0 QTX_CFG_14 TX Queue #14, #(16 * n + 14) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

151044E4 QTX_SCH_14 TX Queue #14, #(16 * n + 14) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

151044E8 QTX_HEAD_14 TX Queue #14, #(16 * n + 14) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

151044EC QTX_TAIL_14 TX Queue #14, #(16 * n + 14) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

151044F0 QTX_CFG_15 TX Queue #15, #(16 * n + 15) Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_RESV_CNT								SW_RESV_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TX_DES_CNT	**TX descriptor count in Queue #**
15:8	HW_RESV_CNT	**Buffer Reserved for HW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved
7:0	SW_RESV_CNT	**Buffer Reserved for SW path** The reserved buffer number is specified on QDMA_RES_THRES. 0: No reserved buffer 1: Buffer Reserved

151044F4 QTX_SCH_15 TX Queue #15, #(16 * n + 15) Schedule 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_SCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_SCH	**Please refer to the description of QTX_SCH_0, the same definition.**

151044F8 QTX_HEAD_15 TX Queue #15, #(16 * n + 15) Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_HEAD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_HEAD	**TX descriptor head pointer in Queue #**

151044FC QTX_TAIL_15 TX Queue #15, #(16 * n + 15) Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DES_TAIL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DES_TAIL	**TX descriptor tail pointer in Queue #**

15104500 QRX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring # (4-DW aligned address)**

15104504 QRX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #**

15104508 QRX_CRX_IDX_0 RX Ring #0 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510450C QRX_DRX_IDX_0 RX Ring #0 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15104580 VQTX_TB_BASE_0 TX Virtual Queue Table #0 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_0	**Base address of TX Virtual Queue Table #0** This virtual queue table belongs to virtual queue group #0

15104584 VQTX_TB_BASE_1 TX Virtual Queue Table #1 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_1	**Base address of TX Virtual Queue Table #1** This virtual queue table belongs to virtual queue group #1

15104588 VQTX_TB_BASE_2 TX Virtual Queue Table #2 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_2	**Base address of TX Virtual Queue Table #2** This virtual queue table belongs to virtual queue group #2

1510458C VQTX_TB_BASE_3 TX Virtual Queue Table #3 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_3	**Base address of TX Virtual Queue Table #3** This virtual queue table belongs to virtual queue group #3

15104590 VQTX_TB_BASE_4 TX Virtual Queue Table #4 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_4	**Base address of TX Virtual Queue Table #4** This virtual queue table belongs to virtual queue group #4

15104594 VQTX_TB_BASE_5 TX Virtual Queue Table #5 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_5	**Base address of TX Virtual Queue Table #5** This virtual queue table belongs to virtual queue group #5

15104598 VQTX_TB_BASE_6 TX Virtual Queue Table #6 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_6	**Base address of TX Virtual Queue Table #6** This virtual queue table belongs to virtual queue group #6

1510459C VQTX_TB_BASE_7 TX Virtual Queue Table #7 Base Address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_TB_BASE_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_TB_BASE_7															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_TB_BASE_7	**Base address of TX Virtual Queue Table #7** This virtual queue table belongs to virtual queue group #7

151045F0 QDMA_PAGE QDMA Configuration Page 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**QTX_CFG_PAGE**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	QTX_CFG_PAGE	**Switch the page of per physical queue configuration registers** This setting will control the following registers: QTX_CFG_*/QTX_SCH_*/QTX_HEAD_*/QTX_TAIL_*/RST_TX_IDX*/QDMA_DROP_PREC/FORCE_QUE 0: Mapping to physical queue #0~15, page n = 0 1: Mapping to physical queue #16~31, page n = 1 2: Mapping to physical queue #32~47, page n = 2 3: Mapping to physical queue #48~63, page n = 3 4: Mapping to physical queue #64~79, page n = 4 5: Mapping to physical queue #80~95, page n = 5 6: Mapping to physical queue #96~111, page n = 6 7: Mapping to physical queue #112~127, page n = 7 Others: Reserved

15104600 QDMA_INFO QDMA Information 1C010080

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV				INDEX_WIDTH											
Type	RO				RO											
Reset	0	0	0	1	1	1	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_QUE_NUM															
Type	RO															
Reset	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	REV	**QDMA revision**
27:24	INDEX_WIDTH	**Ring index width**
15:0	TX_QUE_NUM	**TX queue number**

15104604 QDMA_GLO_CFG QDMA Global Configuration 55404530

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLKGATE_BYP	BYTE_SWAP		PKT_RX_WDONE	DMAD_WR_WDONE										
Type	RW	RW	RW		RW	RW										
Reset	0	1	0		0	1										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MUTLI_CNT				LEAKY_BK			MUTLI_DMA	BIG_ENDIAN		QDMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type	RW				RW			RW	RW		RW		RO	RW	RO	RW
Reset	0	1	0	0	0			1	0		1	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	**Prepend 2-byte to RX-buffer (packet) for aligning IP header to 32-bit boundary.** Default MAC header is 14-byte 0: Disable 2-byte prepended 1: Enable 2-byte prepended
30	CSR_CLKGATE_BYP	**Clock gated Bypass** 0: DMA clock is gating as idle 1: DMA clock is free-running
29	BYTE_SWAP	**Byte Swap** 0: QDMA will not do byte swapping for TX/RX packet descriptor 1: QDMA will do byte swapping for TX/RX packet descriptor
27	PKT_RX_WDONE	**Packet Payload Write Done Check** 0: Write transaction finished after AXI write last 1: Write transaction finished till AXI response done be asserted
26	DMAD_WR_WDONE	**Packet Descriptor Write Done Check** 0: Write transaction finished after AXI write last 1: Write transaction finished till AXI response done be asserted
15:12	MUTLI_CNT	**Number of TX DMA read outstanding transactions when QDMA_GLO_CFG[8] = 1'b1.** 4'h1: Single-issue 4'h2: 2 read transactions 4'h4: 4 read transactions 4'hf: 15 read transactions

Bit(s)	Name	Description
11	LEAKY_BK	**Select bucket type for TX queue MAX sharper and MIN sharper** 0: Token bucket 1: Leaky bucket
8	MUTLI_DMA	**Enable TX DAM AXI read outstanding transaction** 0: Disable TX DMA read outstanding transaction 1: Enable TX DMA read outstanding transaction
7	BIG_ENDIAN	**Big-endian** 0: QDMA will not do byte swapping for TX/RX packet header and payload 1: QDMA will do byte swapping for TX/RX packet header and payload
5:4	QDMA_BT_SIZE	**The burst size of QDMA** 0: 4 DWORDs (16-byte) 1: 8 DWORDs (32-byte) 2: 16 DWORDs (64-byte) 3: 32 DWORDs (128-byte)
3	RX_DMA_BUSY	0: RX_DMA is not busy 1: RX_DMA is busy
2	RX_DMA_EN	0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, and then stop) 1: Enable RX_DMA
1	TX_DMA_BUSY	0: TX_DMA is not busy 1: TX_DNA is busy
0	TX_DMA_EN	0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, and then stop) 1: Enable TX_DMA

15104608 QDMA_RST_IDX QDMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				RST_SCH											RST_DRX_IDX1	RST_DRX_IDX0
Type				RW											RW	RW
Reset				0											0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RST_TX_IDX15	RST_TX_IDX14	RST_TX_IDX13	RST_TX_IDX12	RST_TX_IDX11	RST_TX_IDX10	RST_TX_IDX9	RST_TX_IDX8	RST_TX_IDX7	RST_TX_IDX6	RST_TX_IDX5	RST_TX_IDX4	RST_TX_IDX3	RST_TX_IDX2	RST_TX_IDX1	RST_TX_IDX0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
28	RST_SCH	**Write 1 to reset all token buckets of scheduler** Only valid when QTX_CFG_PAGE = 0
17	RST_DRX_IDX1	**Write 1 to reset RX_DMA RX_IDX1 to 0** Only valid when QTX_CFG_PAGE = 0
16	RST_DRX_IDX0	**Write 1 to reset RX_DMA RX_IDX0 to 0** Only valid when QTX_CFG_PAGE = 0
15	RST_TX_IDX15	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 15) to 0**
14	RST_TX_IDX14	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 14) to 0**
13	RST_TX_IDX13	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 13) to 0**
12	RST_TX_IDX12	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 12) to 0**
11	RST_TX_IDX11	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 11) to 0**
10	RST_TX_IDX10	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 10) to 0**
9	RST_TX_IDX9	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 9) to 0**
8	RST_TX_IDX8	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 8) to 0**
7	RST_TX_IDX7	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 7) to 0**
6	RST_TX_IDX6	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 6) to 0**
5	RST_TX_IDX5	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 5) to 0**
4	RST_TX_IDX4	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 4) to 0**
3	RST_TX_IDX3	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 3) to 0**
2	RST_TX_IDX2	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 2) to 0**
1	RST_TX_IDX1	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 1) to 0**
0	RST_TX_IDX0	**Write 1 to reset TX_DMA TX_IDX (16 * QTX_CFG_PAGE + 0) to 0**

1510460C QDMA_DELAY_INT Delay Interrupt Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RXDLY_INT_EN	RXMAX_PINT							RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DINT_EN	RLS_MAX_PINT							RLS_MAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RXDLY_INT_EN	0: Disable RX delayed interrupt mechanism 1: Enable RX delayed interrupt mechanism
30:24	RXMAX_PINT	**Specified Max. number of pending interrupts** When the number of pending interrupts is equal to or greater than the value specified here or interrupt pending time reaches the limit (see below), a final RX_DLY_INT is generated. [Note] Resetting to 0 can disable pending interrupt count check.
23:16	RXMAX_PTIME	**Specified Max. pending time** When the pending time is equal to or greater than RXMAX_PTIME x 20us or the number of pending RX_DONE is equal to or greater than RXMAX_PINT (see above), a final RX_DLY_INT is generated. [Note] Resetting to 0 can disable pending interrupt time check.
15	RLS_DINT_EN	0: Disable RLS delayed interrupt mechanism 1: Enable RLS delayed interrupt mechanism
14:8	RLS_MAX_PINT	**Specified Max. number of pending interrupts** When the number of pending interrupts is equal to or greater than the value specified here or interrupt pending time reaches the limit (see below), a final RLS_DLY_INT is generated. [Note] Resetting to 0 can disable pending interrupt count check.
7:0	RLS_MAX_PTIME	**Specified Max. pending time** When the pending time is equal to or greater than RLS_MAX_PTIME x 20us or the number of pended RX_DONE is equal to or greater than RLS_MAX_PINT (see above), a final RLS_DLY_INT is generated. [Note] Resetting to 0 can disable pending interrupt time check.

15104610 QDMA_FC_THRES Flow Control Threshold 90904444

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_FSTVQ_MODE		SW_DROP_MODE		SW_DROP_FSTVQ		SW_DROP_FFA	SW_DROP_EN	HW_DROP_FSTVQ_MODE		HW_REDDROP_MODE		HW_DROP_FSTVQ		HW_FC_RELEASE	HW_DROP_EN
Type	RW		RW		RW		RW	RW	RW		RW		RW		RW	RW
Reset	1	0	0	1	0		0	0	1	0	0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SHARE_SW_TH				SHARE_HW_TH				FREE_TH				RING_TH			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

Bit(s)	Name	Description
31:30	SW_DROP_FSTVQ_MODE	**SW drop condition on fullest virtual queue** If the corresponding PQ SW occupied queue depth is over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be dropped depending on the usage of SW free-for-all buffer. 2'b00: FFA usage >= 0% 2'b01: FFA usage >= 25% 2'b10: FFA usage >= 50% 2'b11: FFA usage >= 75%
29:28	SW_DROP_MODE	**Drop Distribution Mode for SW Drop** Different drop probability when SW Free-for-All buffer usage (>75% / >50% / >25% / >0%) Drop Probability: 2'b00: 50%/25%/0%/0% 2'b01: 75%/50%/25%/0% 2'b10: 100%/75%/50%/25% 2'b11: 100%/100%/75%/50%
27	SW_DROP_FSTVQ	**SW drops en-queuing packet on fullest virtual queue; only take effect on the physical queues bound with virtual queues.**
25	SW_DROP_FFA	**Flow Control Drop** QDMA asserts FC when FFA is equal to 0 and egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit. 0: QDMA de-asserts FC when the egress queue count is less than the reserved queue count. 1: QDMA de-asserts FC when FFA is bigger than 0 or the egress queue count is less than the reserved queue count.
24	SW_DROP_EN	**Enable Flow Control for SW buffer pool**

Bit(s)	Name	Description
		QDMA drops packets when FFA is equal to 0 and the egress queue count is bigger than the reserved queue count.
23:22	HW_DROP_FSTVQ_MODE	**HW drop condition on fullest virtual queue** If the corresponding PQ SW occupied queue depth over the SW_RESV_CNT, the en-queuing packet to fullest VQ will be dropped depending on the usage of HW free-for-all buffer. 2'b00: FFA usage >= 0% 2'b01: FFA usage >= 25% 2'b10: FFA usage >= 50% 2'b11: FFA usage >= 75%
21:20	HW_REDDROP_MODE	**Random Early Drop Distribution Mode for HW Drop** Four different drop probabilities when HW Free-for-All (FFA) buffer usage is (>75% / >50% / >25% / >0%) Drop Probability: 2'b00: 50%/25%/0%/0% 2'b01: 75%/50%/25%/0% 2'b10: 100%/75%/50%/25% 2'b11: 100%/100%/75%/50%
19	HW_DROP_FSTVQ	**HW drops en-queuing packet on fullest virtual queue; only take effect on the physical queues bound with virtual queues.**
17	HW_FC_RELEASE	**Flow Control Release Condition (not for RED)** QDMA asserts FC when FFA is equal to DROP/PFC condition and the egress queue count is bigger than the reserved queue count. However, the de-assert condition is specified on this control bit. 0: QDMA de-asserts FC when the egress queue count is less than the reserved queue count. 1: QDMA de-asserts FC when FFA is bigger than DROP/PFC condition or the egress queue count is less than the reserved queue count.
16	HW_DROP_EN	**Drop packets when HW flow control is asserted** QDMA drops packets when Free-for-all (FFA) is equal to 0 and the egress queue count is bigger than the reserved queue count.
15:12	SHARE_SW_TH	**SW Shared buffer threshold** QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
11:8	SHARE_HW_TH	**HW Shared buffer threshold** QDMA will drop TX packets when the left shared buffer descriptors reach this threshold
7:4	FREE_TH	**RX free buffer threshold**

Bit(s)	Name	Description
		QDMA will pause RXDMA interface when the left free buffer descriptors reach this threshold
3:0	RING_TH	**RX Ring threshold** QDMA will pause RXDMA interface when the left RX ring descriptors reach this threshold

15104614 QDMA_FC_MODE QDMA Flow Control Mode 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Reserved															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved												TX_PFC_RELEASE	TX_PFC_ASSERT	TX_PFC_MODE	
Type	RW												RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:4	Reserved	**Reserved**
3	TX_PFC_RELEASE	**PFC Loose Release** QDMA TX queue assert PFC signal only if the egress queue count is bigger than the reserved queue count. 0: PFC is released when FFA and TXQ meet the release condition 1: Release only if TXQ is less than QDMA_TX threshold
2	TX_PFC_ASSERT	**PFC Strict Assertion** QDMA TX queue assert PFC signal only if the egress queue count is bigger than the reserved queue count. 0: PFC is asserted when both FFA and TXQ meet the trigger condition 1: Ignore FFA condition
1:0	TX_PFC_MODE	**Priority Flow Control Assertion Mode** QDMA TXQ asserts PFC signal to PSE when Free-for-all (FFA) usage reach the value and TXQ is bigger than the reserved queue count. When PFC is asserted, the de-asserted condition is that FFA is less than the value and TXQ drops a half lower than the reserved queue count. 2'b00: FFA usage > 0% 2'b01: FFA usage > 25% 2'b10: FFA usage > 50% 2'b11: FFA usage > 75%

15104618 QDMA_INT_STS Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT												RX_DONE_INT0
Type	W1C	W1C	W1C	W1C												W1C
Reset	0	0	0	0												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0				FWD_FIFO_OV				QTX_REQ_EMP_VQ				RLS_DONE_INT
Type	W1C	W1C	W1C	W1C				W1C				W1C				W1C
Reset	0	0	0	0				0				0				0

Bit(s)	Name	Description
31	RX_COHERENT	**RX_DMA finds data coherent event while checking DDONE bit.**
30	RX_DLY_INT	**Summary of the whole QDMA RX related interrupts.**
29	RLS_COHERENT	**TX_DMA finds data coherent event while checking DDONE bit.**
28	RLS_DLY_INT	**Summary of the whole QDMA TX related interrupts.**
16	RX_DONE_INT0	**RX ring #0 packet receive interrupt**
15	VQDEP_DEQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1
14	VQDEP_DEQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0
13	VQDEP_ENQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ has en-queued the first packet descriptor, but the VQ_DEPTH already >=1.
12	VQDEP_ENQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ has en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff.
8	FWD_FIFO_OV	**Forwarding engine FIFO overflow interrupt**
4	QTX_REQ_EMP_VQ	**QDMA TX request to transmit an empty VQ**
0	RLS_DONE_INT	**CPU release transmitted packet interrupt**

1510461C QDMA_INT_MASK Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_COHERENT	RX_DLY_INT	RLS_COHERENT	RLS_DLY_INT												RX_DONE_INT0
Type	RW	RW	RW	RW												RW
Reset	0	0	0	0												0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQDEP_DEQ_ERR1	VQDEP_DEQ_ERR0	VQDEP_ENQ_ERR1	VQDEP_ENQ_ERR0				FWD_FIFO_OV				QTX_REQ_EMP_VQ				RLS_DONE_INT
Type	RW	RW	RW	RW				RW				RW				RW
Reset	0	0	0	0				0				0				0

Bit(s)	Name	Description
31	RX_COHERENT	**Enable interrupt for RX_DMA data coherent event** 0: Disable interrupt 1: Enable interrupt
30	RX_DLY_INT	**Summary of the whole QDMA RX related interrupts.** 0: Disable interrupt 1: Enable interrupt
29	RLS_COHERENT	**Enable interrupt for TX_DMA data coherent event** 0: Disable interrupt 1: Enable interrupt
28	RLS_DLY_INT	**Summary of the whole QDMA TX related interrupts.** 0: Disable interrupt 1: Enable interrupt
16	RX_DONE_INT0	**RX ring #0 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
15	VQDEP_DEQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ not empty yet after de-queuing, but the remainder VQ_DEPTH >= 1 0: Disable interrupt 1: Enable interrupt
14	VQDEP_DEQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during de-queuing.** A VQ becomes empty after de-queuing but the remainder VQ_DEPTH = 0 0: Disable interrupt 1: Enable interrupt

Bit(s)	Name	Description
13	VQDEP_ENQ_ERR1	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ has en-queued the first packet descriptor, but the VQ_DEPTH already >= 1. 0: Disable interrupt 1: Enable interrupt
12	VQDEP_ENQ_ERR0	**VQ depth mismatch with the VQHPTR & VQTPTR during en-queuing.** A VQ has en-queued a packet descriptor, but the VQ_DEPTH already full = 16'hffff. 0: Disable interrupt 1: Enable interrupt
8	FWD_FIFO_OV	**Forwarding engine FIFO overflow interrupt** 0: Disable interrupt 1: Enable interrupt
4	QTX_REQ_EMP_VQ	**QDMA TX request to transmit an empty VQ**
0	RLS_DONE_INT	**CPU release transmitted packet interrupt** 0: Disable interrupt 1: Enable interrupt

15104620 QDMA_INT_GRP1 QDMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP1	**Interrupt group 1 assignment.** Each bit's definition is the same as "QDMA_INT_STS" 0: Leave to QDMA interrupt group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0) 1: Assign to QDMA interrupt group 1

15104624 QDMA_INT_GRP2 QDMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_GRP2	**Interrupt group 2 assignment.** Each bit's definition is the same as "QDMA_INT_STS" 0: Leave to QDMA interrupt group 0, if (QDMA_INT_GRP1[n]==0 & QDMA_INT_GRP2[n]==0) 1: Assign to QDMA interrupt group 2

15104628 QDMA_DROP_PREC QDMA Drop by FFA Percentage Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_DROP_PREC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SW_DROP_PREC	**QDMA SW Drop by FFA Percentage Control** QDMA drop packets based on the full percentage of Free-for-All [31:16] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)] 0: Disable drop by FFA percentage 1: Enable drop by FFA percentage
15:0	HW_DROP_PREC	**QDMA HW Drop by FFA Percentage Control** QDMA drop packets based on the full percentage of Free-for-All [15:0] = [PQ#(16 * QTX_CFG_PAGE + 15) : PQ#(16 * QTX_CFG_PAGE + 0)] 0: Disable drop by FFA percentage 1: Enable drop by FFA percentage

15104640 QDMA_HRED1 QDMA HW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	**Low Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	**Middle Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

15104644 QDMA_HRED2 QDMA HW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															FFA_UTIL_SEL
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_HIGH_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REV0	**Reserved**
16	FFA_UTIL_SEL	**Manually Set FFA Utilization** When the bit is set, FFA utilization will be configurable.
15:0	FFA_HIGH_UTIL	**High Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

15104648 QDMA_SRED1 QDMA SW RED Distribution - I FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FFA_LOW_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	FFA_LOW_UTIL	**Low Utilization of FFA on HW path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 25% probability.
15:0	FFA_MIDDLE_UTIL	**Middle Utilization of FFA on CPU path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 50% probability.

1510464C QDMA_SRED2 QDMA SW RED Distribution - II FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															FFA_UTIL_SEL
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFA_MIDDLE_UTIL															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:17	REV0	**Reserved**
16	FFA_UTIL_SEL	**Manually Set FFA Utilization** When the bit is set, FFA utilization will be configurable.
15:0	FFA_MIDDLE_UTIL	**High Utilization of FFA on CPU path** When the utilization of FFA reaches the threshold, RED will start to drop the en-queued packets by 75% probability.

15104670 QDMA_INT_STS_G0 QDMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G0	**Interrupt group 0 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is the same as "QDMA_INT_STS"

15104674 QDMA_INT_STS_G1 QDMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G1	**Interrupt group 1 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is the same as "QDMA_INT_STS"

15104678 QDMA_INT_STS_G2 QDMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QDMA_INT_STS_G2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QDMA_INT_STS_G2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QDMA_INT_STS_G2	**Interrupt group 2 status, this information already "and" with "QDMA_INT_IMR"** Each bit definition is the same as "QDMA_INT_STS"

15104680 VQTX_GLO TX Virtual Queue Global Configuration 000005EA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															VQTB_MIB_EN	
Type															RW	
Reset															0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_GQTUM															
Type	RW															
Reset	0	0	0	0	0	1	0	1	1	1	1	0	1	0	1	0

Bit(s)	Name	Description
17	VQTB_MIB_EN	**Configuration for the MIB packet/byte counter field of virtual queue table** 0: Disable MIB counter field; each virtual table entry is 16 bytes 1: Enable MIB counter field; each virtual table entry extends to 32 bytes, to record the amount of transmitted byte and packet count for each virtual queue
15:0	VQTX_GQTUM	**Amount of bytes a virtual queue is allowed to de-queue before the scheduler moves to the next virtual queue. Defaults to the MTU of the interface. The minimum value is 1.**

1510468C VQTX_INVLD_PTR TX Virtual Queue Invalid Pointer DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_INVLD_PTR															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_INVLD_PTR															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	VQTX_INVLD_PTR	**The pointer address indicates an invalid virtual queue head/tail pointer.** Either "VQHPTR" or "VQTPTR" of VQ table is equal to this invalid pointer VQTX_INVLD_PTR, which means there is no valid packet in this virtual queue.

15104690 VQTX_NUM Number of TX Virtual Queue Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VQTX_NUM_7				VQTX_NUM_6				VQTX_NUM_5				VQTX_NUM_4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_NUM_3				VQTX_NUM_2				VQTX_NUM_1				VQTX_NUM_0		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
30:28	VQTX_NUM_7	**Number of virtual queues in virtual queue group #7**
26:24	VQTX_NUM_6	**Number of virtual queues in virtual queue group #6**
22:20	VQTX_NUM_5	**Number of virtual queues in virtual queue group #5**
18:16	VQTX_NUM_4	**Number of virtual queues in virtual queue group #4**
14:12	VQTX_NUM_3	**Number of virtual queues in virtual queue group #3**
10:8	VQTX_NUM_2	**Number of virtual queues in virtual queue group #2**
6:4	VQTX_NUM_1	**Number of virtual queues in virtual queue group #1**
2:0	VQTX_NUM_0	**Number of virtual queues in virtual queue group #0** 0: Disable virtual queue function 1: 32 2: 64 3: 128 4: 256 5: 512 6: 1024 7: Reserved

15104698 VQTX_SCH TX Virtual Queue Schedule Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			VQTX_SCH_7				VQTX_SCH_6				VQTX_SCH_5				VQTX_SCH_4	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			VQTX_SCH_3				VQTX_SCH_2				VQTX_SCH_1				VQTX_SCH_0	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Name	Description
29:28	VQTX_SCH_7	**Virtual queues scheduling strategy for virtual queue group #7**
25:24	VQTX_SCH_6	**Virtual queues scheduling strategy for virtual queue group #6**
21:20	VQTX_SCH_5	**Virtual queues scheduling strategy for virtual queue group #5**
17:16	VQTX_SCH_4	**Virtual queues scheduling strategy for virtual queue group #4**
13:12	VQTX_SCH_3	**Virtual queues scheduling strategy for virtual queue group #3**
9:8	VQTX_SCH_2	**Virtual queues scheduling strategy for virtual queue group #2**
5:4	VQTX_SCH_1	**Virtual queues scheduling strategy for virtual queue group #1**
1:0	VQTX_SCH_0	**Virtual queues scheduling strategy for virtual queue group #0** 0: SFQ (packet base round robin) 1: DRR (deficit round robin) 2: Reserved 3: Reserved

151046A0 VQTX_HASH_CFG TX Virtual Queue Hash Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					HASH_PTB_MODE_EN_3	HASH_PTB_MODE_EN_2	HASH_PTB_MODE_EN_1	HASH_PTB_MODE_EN_0			HASH_ST_MODE					HASH_PTB_PRD
Type					RW	RW	RW	RW			RW					RW
Reset					0	0	0	0			0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_PTB_PRD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27	HASH_PTB_MODE_EN_3	**Enable "Exclusive with CRC32" as a candidate algorithm for perturbed hash changing. This field is only valid when HASH_PTB_PRD!=0.**
26	HASH_PTB_MODE_EN_2	**Enable "Exclusive with (B^(A&~C))" as a candidate algorithm for perturbed hash changing. This field is only valid when HASH_PTB_PRD!=0.**
25	HASH_PTB_MODE_EN_1	**Enable "Exclusive with (A&B)|(~A&C)" as a candidate algorithm for perturbed hash changing. This field is only valid when HASH_PTB_PRD!=0.**
24	HASH_PTB_MODE_EN_0	**Enable "Exclusive with HASH_SEED" as a candidate algorithm for perturbed hash changing. This field is only valid when HASH_PTB_PRD!=0.** (If HASH_PTB_MODE_EN_0~3 are all "0", hash will be forced on "Exclusive with HASH_SEED" mode.)
21:20	HASH_ST_MODE	**Hash scrambled mode selection, for static hash virtual queue index generating.** This field is only valid when HASH_PTB_PRD = 0 3: Exclusive with CRC32 2: Exclusive with (B^(A&~C)) 1: Exclusive with (A&B)|(~A&C) 0: Exclusive with HASH_SEED
16:0	HASH_PTB_PRD	**If HASH_PTB_PRD = 0, it means operating in static hash mode, never changing the hash algorithm periodically.** Otherwise, operating in perturb hash mode when HASH_PTB_PRD != 0. HASH_PERTURB_PRD indicates the period to change the hash algorithm for virtual queue index generating, in 1ms unit.

151046A4 VQTX_HASH_SD TX Virtual Queue Hash Seed 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HASH_SD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HASH_SD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HASH_SD	**Hash seed for "Exclusive with HASH_SEED" mode.**

151046B0 VQTX_VLD_CFG TX Virtual Queue Valid Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_VLD_STRG_7				VQTX_VLD_STRG_6				VQTX_VLD_STRG_5				VQTX_VLD_STRG_4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_VLD_STRG_3				VQTX_VLD_STRG_2				VQTX_VLD_STRG_1				VQTX_VLD_STRG_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	VQTX_VLD_STRG_7	**Virtual Queue Group #7: Virtual queue valid bit map starting slice number.**
27:24	VQTX_VLD_STRG_6	**Virtual Queue Group #6: Virtual queue valid bit map starting slice number.**
23:20	VQTX_VLD_STRG_5	**Virtual Queue Group #5: Virtual queue valid bit map starting slice number.**
19:16	VQTX_VLD_STRG_4	**Virtual Queue Group #4: Virtual queue valid bit map starting slice number.**
15:12	VQTX_VLD_STRG_3	**Virtual Queue Group #3: Virtual queue valid bit map starting slice number.**
11:8	VQTX_VLD_STRG_2	**Virtual Queue Group #2: Virtual queue valid bit map starting slice number.**
7:4	VQTX_VLD_STRG_1	**Virtual Queue Group #1: Virtual queue valid bit map starting slice number.**
3:0	VQTX_VLD_STRG_0	**Virtual Queue Group #0: Virtual queue valid bit map starting slice number.** 1 VQ valid bit slice comprises 64-bit map. The amount of VQ valid slices for 1 VQ group depends on the setting of "VQTX_NUM_#"; hardware will allocate VQ valid bit slices for each VQ group. 4'h0: VQ valid bit map starting from slice#0 4'h1: VQ valid bit map starting from slice#1 4'h15: VQ valid bit map starting from slice#15

151046BC QTX_MIB_IF TX Queue MIB Interface 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			MIB_RC_DIS	VQTX_MIB_EN				MIB_PQ_SHW_SEP		QTX_MIB_QID						
Type			RW	W1				RW		RW						
Reset			0	0				0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							QTX_MIB_VQID									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
29	MIB_RC_DIS	**Disable the clear action during MIB reading** 0: After MIB reading is done, the target MIB counter will be cleared to 0 1: Keeps the value of target MIB counter after MIB reading
28	VQTX_MIB_EN	**Enable VQTB MIB read procedure** 0: After MIB accessing is done, HW will clear this bit to 0 and put the result in VQTX_MIB_PCNT, VQTX_MIB_DPCNT, VQTX_MIB_BCNT0, VQTX_MIB_BCNT1 1: Enable MIB accessing procedure
24	MIB_PQ_SHW_SEP	**Separate the PQ's HW/SW MIB counter of QTX_MIB_PCNT and QTX_MIB_DPCNT** 0: Use the whole 32 bits as one MIB counter, which accumulates SW and HW packet counts 1: Separate the SW and HW MIB counters
22:16	QTX_MIB_QID	**Physical queue ID for MIB accessing**
9:0	QTX_MIB_VQID	**Virtual queue ID for MIB accessing**

151046C0 VQTX_MIB_PCNT TX Virtual Queue MIB Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_PCNT	**Packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

151046C4 VQTX_MIB_BCNTL TX Virtual Queue MIB Byte Count Low Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNTH	**Byte count [31:0] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

151046C8 VQTX_MIB_BCNTH TX Virtual Queue MIB Byte Count High Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_BCNTL	**Byte count [63:32] of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

151046CC VQTX_MIB_DPCNT TX Virtual Queue MIB Drop Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VQTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VQTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	VQTX_MIB_DPCNT	**Dropped packet count of virtual queue table, according to QTX_MIB_QID and QTX_MIB_VQID.** Unavailable when VQTB_MIB_EN = 0

151046D0 QTX_MIB_PCNT TX Physical Queue MIB Forward Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_PCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_PCNT	**Accumulated forwarded packet count, according to QTX_MIB_QID.** If MIB_PQ_SHW_SEP = 1, this counter will be separated into two 16-bit counters, [31:16] for software path and [15:0] for hardware path.

151046D4 QTX_MIB_DPCNT TX Physical Queue MIB Dropped Packet Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_DPCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_DPCNT	**Accumulated dropped packet count, according to QTX_MIB_QID.** If MIB_PQ_SHW_SEP = 1, this counter will be separated into two 16bits counter, [31:16] for software path, [15:0] for hardware path.

151046D8 QTX_MIB_BCNTL TX Physical Queue MIB Byte Count Low Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_BCNTL															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_BCNTL	**Accumulated forwarded byte count [31:0] of physical queue #QTX_MIB_QID.** Reading QTX_MIB_BCNTL will not clear the value of QTX_MIB_BCNTL. QTX_MIB_BCNTL will be cleared by reading QTX_MIB_BCNTH when VQTB_MIB_RC_DIS = 0.

151046DC QTX_MIB_BCNTH TX Physical Queue MIB Byte Count High Bytes 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_MIB_BCNTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_MIB_BCNTH	**Accumulated forwarded byte count [35:32] of physical queue #QTX_MIB_QID** If VQTB_MIB_RC_DIS = 0, reading QTX_MIB_BCNTH will clear the value of QTX_MIB_BCNTH & QTX_MIB_BCNTL.

15104700 QTX_CTX_PTR TX Forward CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_CTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_CTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_CTX_PTR	**TX forward chain CPU pointer**

15104704 QTX_DTX_PTR TX Forward DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWD_DTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWD_DTX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWD_DTX_PTR	**TX forward chain DMA pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104708 QTX_FWD_CNT TX Forward DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACC_HW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_SW_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ACC_HW_CNT	**Accumulated HW forwarded counter**
15:0	ACC_SW_CNT	**Accumulated SW forwarded counter**

15104710 QTX_CRX_PTR TX Release CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_CRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_CRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_CRX_PTR	**TX release chain CPU pointer**

15104714 QTX_DRX_PTR TX Release DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RLS_DRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RLS_DRX_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RLS_DRX_PTR	**TX release chain DMA pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104718 QTX_RLS_CNT TX Release DMA Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACC_RLS_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACC_RLS_CNT	**Accumulated TX released descriptor count**

15104720 QDMA_FQ_HEAD Free Page Head Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_HEAD_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_HEAD_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_HEAD_PTR	**Free buffer head pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104724 QDMA_FQ_TAIL Free Page Tail Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FQ_TAIL_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQ_TAIL_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FQ_TAIL_PTR	**Free buffer tail pointer** When QDMA TX is disabled, this field can be set to the initial pointer by CPU. After QDMA TX is enabled, this field is read-only.

15104728 QDMA_FQ_CNT Free Page Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HWFQ_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SWFQ_CNT	**Free buffer on CPU Pool** Initial free buffer count on CPU pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.
15:0	HWFQ_CNT	**Free buffer on HW Pool** Initial free buffer count on HW pool when QDMA_GLO_CFG.TX_DMA_EN is de-asserted.

1510472C QDMA_FQ_BLEN Free Page Buffer Length 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FQ_BUF_BLEN													
Type			RW													
Reset			0	0	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
29:16	FQ_BUF_BLEN	**Free buffer byte length** Configured free buffer length, QDMA RX will fetch the length info to decide the payload length on one descriptor/buffer.

15104798 QDMA_TX_SCH1_SCH2 TX Scheduler1 and Scheduler2 Rate Control 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCH2_MAX_WFQ	SCH2_LEAKY_BK	SCH2_BUCKET_DEP		SCH2_RATE_EN	SCH2_RATE_MAN							SCH2_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCH1_MAX_WFQ	SCH1_LEAKY_BK	SCH1_BUCKET_DEP		SCH1_RATE_EN	SCH1_RATE_MAN							SCH1_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	SCH2_MAX_WFQ	**Physical Queue arbitration mechanism between MIN and MAX rates** 0: Strict Priority 1: Weighted Fair Queue
30	SCH2_LEAKY_BK	**Select bucket type for scheduler output sharper** 0: Token bucket 1: Leaky bucket
29:28	SCH2_BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3:16KB
27	SCH2_RATE_EN	**Enable TX SCH2 max. rate control** 0: Disable 1: Enable
26:20	SCH2_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH2** Value range: 0~127
19:16	SCH2_RATE_EXP	**Exponent part of the max. rate control of the TX SCH2** Value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps)

Bit(s)	Name	Description
		5: QDMA_RATE_EXP5 (default: 100Mbps)
		Others: 20'd1, 1Gbps
15	SCH1_MAX_WFQ	**Physical Queue arbitration mechanism between MIN and MAX rates**
		0: Strict Priority
		1: Weighted Fair Queue
14	SCH1_LEAKY_BK	**Select bucket type for scheduler output sharper**
		0: Token bucket
		1: Leaky bucket
13:12	SCH1_BUCKET_DEP	**Bucket Depth**
		0: 2KB
		1: 4KB
		2: 8KB
		3:16KB
11	SCH1_RATE_EN	**Enable TX SCH1 max. rate control**
		0: Disable
		1: Enable
10:4	SCH1_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH1**
		Value range: 0~127
3:0	SCH1_RATE_EXP	**Exponent part of the max. rate control of the TX SCH2**
		Value selection
		0: QDMA_RATE_EXP0 (default: 1kbps)
		1: QDMA_RATE_EXP1 (default: 10kbps)
		2: QDMA_RATE_EXP2 (default: 100kbps)
		3: QDMA_RATE_EXP3 (default: 1Mbps)
		4: QDMA_RATE_EXP4 (default: 10Mbps)
		5: QDMA_RATE_EXP5 (default: 100Mbps)
		Others: 20'd1, 1Gbps

1510479C QDMA_TX_SCH3_SCH4 TX Scheduler3 and Scheduler4 Rate Control 00100010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SCH4_MAX_WFQ	SCH4_LEAKY_BK	SCH4_BUCKET_DEP		SCH4_RATE_EN	SCH4_RATE_MAN							SCH4_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SCH3_MAX_WFQ	SCH3_LEAKY_BK	SCH3_BUCKET_DEP		SCH3_RATE_EN	SCH3_RATE_MAN							SCH3_RATE_EXP			
Type	RW	RW	RW		RW	RW							RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	SCH4_MAX_WFQ	**Physical Queue arbitration mechanism between MIN and MAX rates** 0: Strict Priority 1: Weighted Fair Queue
30	SCH4_LEAKY_BK	**Select bucket type for scheduler output sharper** 0: Token bucket 1: Leaky bucket
29:28	SCH4_BUCKET_DEP	**Bucket Depth** 0: 2KB 1: 4KB 2: 8KB 3:16KB
27	SCH4_RATE_EN	**Enable TX SCH4 max. rate control** 0: Disable 1: Enable
26:20	SCH4_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH4** Value range: 0~127
19:16	SCH4_RATE_EXP	**Exponent part of the max. rate control of the TX SCH4** Value selection 0: QDMA_RATE_EXP0 (default: 1kbps) 1: QDMA_RATE_EXP1 (default: 10kbps) 2: QDMA_RATE_EXP2 (default: 100kbps) 3: QDMA_RATE_EXP3 (default: 1Mbps) 4: QDMA_RATE_EXP4 (default: 10Mbps)

Bit(s)	Name	Description
		5: QDMA_RATE_EXP5 (default: 100Mbps)
		Others: 20'd1, 1Gbps
15	SCH3_MAX_WFQ	**Physical Queue arbitration mechanism between MIN and MAX rates**
		0: Strict Priority
		1: Weighted Fair Queue
14	SCH3_LEAKY_BK	**Select bucket type for scheduler output sharper**
		0: Token bucket
		1: Leaky bucket
13:12	SCH3_BUCKET_DEP	**Bucket Depth**
		0: 2KB
		1: 4KB
		2: 8KB
		3:16KB
11	SCH3_RATE_EN	**Enable TX SCH3 max. rate control**
		0: Disable
		1: Enable
10:4	SCH3_RATE_MAN	**Mantissa part of the max. rate control of the TX SCH3**
		Value range: 0~127
3:0	SCH3_RATE_EXP	**Exponent part of the max. rate control of the TX SCH3**
		Value selection
		0: QDMA_RATE_EXP0 (default: 1kbps)
		1: QDMA_RATE_EXP1 (default: 10kbps)
		2: QDMA_RATE_EXP2 (default: 100kbps)
		3: QDMA_RATE_EXP3 (default: 1Mbps)
		4: QDMA_RATE_EXP4 (default: 10Mbps)
		5: QDMA_RATE_EXP5 (default: 100Mbps)
		Others: 20'd1, 1Gbps

151047C0 VQTX_0_3_BIND_QID QDMA Virtual Queue Group #0~3 to Physical Queue Binding 03020100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VQTX_3_BIND_QID								VQTX_2_BIND_QID						
Type		RW								RW						
Reset		0	0	0	0	0	1	1		0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_1_BIND_QID								VQTX_0_BIND_QID						
Type		RW								RW						
Reset		0	0	0	0	0	0	1		0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	VQTX_3_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #3**
22:16	VQTX_2_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #2**
14:8	VQTX_1_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #1**
6:0	VQTX_0_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #0**

151047C4 **VQTX_4_7_BIND_QID** **QDMA Virtual Queue Group #4~7 to Physical Queue Binding** **07060504**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		VQTX_7_BIND_QID								VQTX_6_BIND_QID						
Type		RW								RW						
Reset		0	0	0	0	1	1	1		0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		VQTX_5_BIND_QID								VQTX_4_BIND_QID						
Type		RW								RW						
Reset		0	0	0	0	1	0	1		0	0	0	0	1	0	0

Bit(s)	Name	Description
30:24	VQTX_7_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #7**
22:16	VQTX_6_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #6**
14:8	VQTX_5_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #5**
6:0	VQTX_4_BIND_QID	**The Physical Queue Number which binds with Virtual queue group #4**

151047E0 **QTX_FC_SW_STS_0_15** **TX Queue#0~15 Software Path Flow Control Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	QTX_FC_SW_STS_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QTX_FC_SW_STS_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	QTX_FC_SW_STS_0_15	**TX Queue Software Path Flow Control Status** Each bit indicates the flow control decision on each physical queue's packet from software path. [0]: PQ#0 .... [15]: PQ#15 0: Packet could be en-queued 1: Current incoming packets will be dropped

151047EC **QDMA_ULTRA_CFG** **QDMA AXI ULTRA Configuration** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_ULTRA_EN					AXI_ULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_PREULTRA_EN					AXI_PREULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AXI_ULTRA_EN	**Enable AXI Ultra transaction** 0: Disable 1: Enable
26:16	AXI_ULTRA_THRES	**AXI Ultra threshold.** If CDM TX free FIFO count is bigger than AXI_ULTRA_THRES, it will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.
15	AXI_PREULTRA_EN	**Enable AXI Pre-ultra transaction** 0: Disable 1: Enable
10:0	AXI_PREULTRA_THRES	**AXI Pre-ultra threshold.** If CDM TX free FIFO count is bigger than AXI_PREULTRA_THRES, it will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1.

151047F0 QDMA_BUS_CFG QDMA AXI BUS Configuration 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												CCI_EN	CCI_VQTB_EN	CCI_QRXFQ_EN	CCI_FQ_EN
Type	RO												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AXI_CTRL_UPDATED	AXI_R_BUSY	AXI_W_BUSY		AXI_LOCK_ERROR	AXI_ERRMID_SET_RIRQ	AXI_ERRMID_SET_BIRQ	AXI_OUTSTANDING_EXTEND	AXI_QOS_ON		AXI_CG_DISABLE
Type						RO	RO	RO		RO	RO	RO	RW	RW		RW
Reset						1	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
31:20	REV0	**Reserved**
19	CCI_EN	**QDMA CCI global control bit on BMU, QTX and QRX**
18	CCI_VQTB_EN	**BMU VQTB access the bus through CCI if CCI_EN = 1**
17	CCI_QRXFQ_EN	**QRX FQ_DES access the bus through CCI if CCI_EN = 1**
16	CCI_FQ_EN	**BMU FQ_DES access the bus through CCI if CCI_EN = 1**
10	AXI_CTRL_UPDATED	**Master interface control signal updated status**
9	AXI_R_BUSY	**Read transaction not completes**
8	AXI_W_BUSY	**Write transaction not completes**
6	AXI_LOCK_ERROR	**Detects lock error**
5	AXI_ERRMID_SET_RIRQ	**Detects error MID from slave in R channel**
4	AXI_ERRMID_SET_BIRQ	**Detects error MID from slave in B channel**
3	AXI_OUTSTANDING_EXTEND	**Auto adds extra outstanding for QoS command** 0: Disable 1: Enable
2	AXI_QOS_ON	**Enable QoS function** 0: Disable 1: Enable
0	AXI_CG_DISABLE	**Disable auto clock gating of AXI component** 0: Disable 1: Enable

151047F4 QDMA_RBUS_CFG QDMA RBUS Configuration 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									R2X_DBG_SEL						R2X_INT_B	R2X_INT_EN
Type									RW						RO	RW
Reset									0	0	0	0			1	0

Bit(s)	Name	Description
7:4	R2X_DBG_SEL	**Select debug information from R2X** 0: R2X interrupt status 1: R2X interrupt enable and Rbus status 2: Rbus address 3: AXI status 4: AXI write address 5: AXI read address 6: Internal buffer handshake 7: Coherence sequence and Coherence length 8: Coherence compare address
1	R2X_INT_B	**R2X interrupt status** R2X wrapper interrupt will set 1'b1 when receiving len = 0 cmd from rbus master.
0	R2X_INT_EN	**Enable R2X Interrupt** Enable R2X wrapper interrupt when receiving len = 0 cmd from rbus master. 0: Disable 1: Enable

151047F8 QDMA_RBUS_STAT_0 R2X Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_INT_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_INT_STATUS	**Record the address when receiving len = 0 cmd from R2X selected channel according to QDMA_RBUS_CFG[7:4]**

151047FC QDMA_RBUS_STAT_1 R2X Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	R2X_DBG_INFO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	R2X_DBG_INFO	**Record debug information from R2X selected channel according to QDMA_RBUS_CFG[7:4]**

5.4 ADMA

5.4.1 Register Definition

Module name: ADMAv2 Base address: (+0x15106000)

Address	Name	Width	Register Function
15106000	ADMA_TX_BASE_PTR_0	32	TX Ring #0 Base Pointer
15106004	ADMA_TX_MAX_CNT_0	32	TX Ring #0 Maximum Count
15106008	ADMA_TX_CTX_IDX_0	32	TX Ring #0 CPU Pointer
1510600C	ADMA_TX_DTX_IDX_0	32	TX Ring #0 DMA Pointer
15106010	ADMA_TX_BASE_PTR_1	32	TX Ring #1 Base Pointer
15106014	ADMA_TX_MAX_CNT_1	32	TX Ring #1 Maximum Count
15106018	ADMA_TX_CTX_IDX_1	32	TX Ring #1 CPU Pointer
1510601C	ADMA_TX_DTX_IDX_1	32	TX Ring #1 DMA Pointer
15106020	ADMA_TX_BASE_PTR_2	32	TX Ring #2 Base Pointer
15106024	ADMA_TX_MAX_CNT_2	32	TX Ring #2 Maximum Count
15106028	ADMA_TX_CTX_IDX_2	32	TX Ring #2 CPU Pointer
1510602C	ADMA_TX_DTX_IDX_2	32	TX Ring #2 DMA Pointer
15106030	ADMA_TX_BASE_PTR_3	32	TX Ring #3 Base Pointer
15106034	ADMA_TX_MAX_CNT_3	32	TX Ring #3 Maximum Count
15106038	ADMA_TX_CTX_IDX_3	32	TX Ring #3 CPU Pointer
1510603C	ADMA_TX_DTX_IDX_3	32	TX Ring #3 DMA Pointer
15106100	ADMA_RX_BASE_PTR_0	32	RX Ring #0 Base Pointer
15106104	ADMA_RX_MAX_CNT_0	32	RX Ring #0 Maximum Count
15106108	ADMA_RX_CRX_IDX_0	32	RX Ring #0 CPU Pointer
1510610C	ADMA_RX_DRX_IDX_0	32	RX Ring #0 DMA Pointer
15106110	ADMA_RX_BASE_PTR_1	32	RX Ring #1 Base Pointer
15106114	ADMA_RX_MAX_CNT_1	32	RX Ring #1 Maximum Count
15106118	ADMA_RX_CRX_IDX_1	32	RX Ring #1 CPU pointer
1510611C	ADMA_RX_DRX_IDX_1	32	RX Ring #1 DMA Pointer
15106120	ADMA_RX_BASE_PTR_2	32	RX Ring #2 Base Pointer
15106124	ADMA_RX_MAX_CNT_2	32	RX Ring #2 Maximum Count
15106128	ADMA_RX_CRX_IDX_2	32	RX Ring #2 CPU Pointer
1510612C	ADMA_RX_DRX_IDX_2	32	RX Ring #2 DMA Pointer
15106130	ADMA_RX_BASE_PTR_3	32	RX Ring #3 Base Pointer
15106134	ADMA_RX_MAX_CNT_3	32	RX Ring #3 Maximum Count
15106138	ADMA_RX_CRX_IDX_3	32	RX Ring #3 CPU Pointer
1510613C	ADMA_RX_DRX_IDX_3	32	RX Ring #3 DMA Pointer
15106140	ADMA_RX_BASE_PTR_4	32	RX Ring #4 Base Pointer
15106144	ADMA_RX_MAX_CNT_4	32	RX Ring #4 Maximum Count
15106148	ADMA_RX_CRX_IDX_4	32	RX Ring #4 CPU Pointer
1510614C	ADMA_RX_DRX_IDX_4	32	RX Ring #4 DMA Pointer
15106150	ADMA_RX_BASE_PTR_5	32	RX Ring #5 Base Pointer
15106154	ADMA_RX_MAX_CNT_5	32	RX Ring #5 Maximum Count
15106158	ADMA_RX_CRX_IDX_5	32	RX Ring #5 CPU Pointer
1510615C	ADMA_RX_DRX_IDX_5	32	RX Ring #5 DMA Pointer
15106160	ADMA_RX_BASE_PTR_6	32	RX Ring #6 Base Pointer
15106164	ADMA_RX_MAX_CNT_6	32	RX Ring #6 Maximum Count
15106168	ADMA_RX_CRX_IDX_6	32	RX Ring #6 CPU Pointer
1510616C	ADMA_RX_DRX_IDX_6	32	RX Ring #6 DMA Pointer
15106170	ADMA_RX_BASE_PTR_7	32	RX Ring #7 Base Pointer
15106174	ADMA_RX_MAX_CNT_7	32	RX Ring #7 Maximum Count
15106178	ADMA_RX_CRX_IDX_7	32	RX Ring #7 CPU Pointer

Address	Name	Width	Register Function
1510617C	ADMA_RX_DRX_IDX_7	32	RX Ring #7 DMA Pointer
15106200	ADMA_INFO	32	ADMA Information
15106204	ADMA_GLO_CFG	32	ADMA Global Configuration
15106208	ADMA_RST_IDX	32	ADMA Reset Index
15106210	ADMA_RX_CFG	32	ADMA Rx DMA Configuration
15106220	ADMA_INT_STATUS	32	ADMA Interrupt Status
15106228	ADMA_INT_MASK	32	ADMA Interrupt Mask
15106240	ADMA_INT_STS_GRP0	32	ADMA Interrupt Status Group 0
15106244	ADMA_INT_STS_GRP1	32	ADMA Interrupt Status Group 1
15106248	ADMA_INT_STS_GRP2	32	ADMA Interrupt Status Group 2
1510624C	ADMA_INT_STS_GRP3	32	ADMA Interrupt Status Group 3
15106250	ADMA_INT_GRP1	32	ADMA Interrupt Group 1 Control
15106254	ADMA_INT_GRP2	32	ADMA Interrupt Group 2 Control
15106258	ADMA_INT_GRP3	32	ADMA Interrupt Group 3 Control
15106260	ADMA_BUS_CFG	32	ADMA AXI BUS Configuration
15106264	ADMA_ULTRA_CFG	32	ADMA AXI ULTRA Configuration
15106290	ADMA_INT_STATUS_0	32	ADMA Interrupt Status 0
15106294	ADMA_INT_MASK_0	32	ADMA Interrupt Mask 0
15106298	ADMA_INT_STATUS_1	32	ADMA Interrupt Status 1
1510629C	ADMA_INT_MASK_1	32	ADMA Interrupt Mask 1
151062A0	ADMA_INT_STATUS_2	32	ADMA Interrupt Status 2
151062A4	ADMA_INT_MASK_2	32	ADMA Interrupt Mask 2
151062A8	ADMA_INT_STATUS_3	32	ADMA Interrupt Status 3
151062AC	ADMA_INT_MASK_3	32	ADMA Interrupt Mask 3
151062B0	ADMA_TX_DELAY_INT_CFG_0	32	ADMA Tx Delay Interrupt Configuration 0
151062B4	ADMA_TX_DELAY_INT_CFG_1	32	ADMA Tx Delay Interrupt Configuration 1
151062C0	ADMA_RX_DELAY_INT_CFG_0	32	ADMA Rx Delay Interrupt Configuration 0

15106000 ADMA_TX_BASE_PTR_0 TX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #0 (4-DW aligned address)**

15106004 ADMA_TX_MAX_CNT_0 TX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #0**

15106008 ADMA_TX_CTX_IDX_0 TX Ring #0 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_CTX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1510600C ADMA_TX_DTX_IDX_0 TX Ring #0 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_DTX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

15106010 ADMA_TX_BASE_PTR_1 TX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #1 (4-DW aligned address)**

15106014 ADMA_TX_MAX_CNT_1 TX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #1**

15106018 ADMA_TX_CTX_IDX_1 TX Ring #1 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_CTX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1510601C ADMA_TX_DTX_IDX_1 TX Ring #1 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_DTX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

15106020 ADMA_TX_BASE_PTR_2 TX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #2 (4-DW aligned address)**

15106024 ADMA_TX_MAX_CNT_2 TX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #2**

15106028 ADMA_TX_CTX_IDX_2 TX Ring #2 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_CTX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1510602C **ADMA_TX_DTX_IDX_2** **TX Ring #2 DMA Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_DTX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

15106030 ADMA_TX_BASE_PTR_3 TX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BASE_PTR	**Point to the base address of TX Ring #3 (4-DW aligned address)**

15106034 ADMA_TX_MAX_CNT_3 TX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_MAX_CNT	**The maximum number of TXD count in TX Ring #3**

15106038 ADMA_TX_CTX_IDX_3 TX Ring #3 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_CTX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_CTX_IDX	**Point to the next TXD CPU wants to use**

1510603C ADMA_TX_DTX_IDX_3 TX Ring #3 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**TX_DTX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	TX_DTX_IDX	**Point to the next TXD DMA wants to use**

15106100 ADMA_RX_BASE_PTR_0 RX Ring #0 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #0 (4-DW aligned address)**

15106104 ADMA_RX_MAX_CNT_0 RX Ring #0 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #0**

15106108 ADMA_RX_CRX_IDX_0 RX Ring #0 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510610C ADMA_RX_DRX_IDX_0 RX Ring #0 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106110 ADMA_RX_BASE_PTR_1 RX Ring #1 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #1 (4-DW aligned address)**

15106114 ADMA_RX_MAX_CNT_1 RX Ring #1 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #1**

15106118 ADMA_RX_CRX_IDX_1 RX Ring #1 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510611C ADMA_RX_DRX_IDX_1 RX Ring #1 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106120 ADMA_RX_BASE_PTR_2 RX Ring #2 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #2 (4-DW aligned address)**

15106124 ADMA_RX_MAX_CNT_2 RX Ring #2 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #2**

15106128 ADMA_RX_CRX_IDX_2 RX Ring #2 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510612C ADMA_RX_DRX_IDX_2 RX Ring #2 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106130 ADMA_RX_BASE_PTR_3 RX Ring #3 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #3 (4-DW aligned address)**

15106134 ADMA_RX_MAX_CNT_3 RX Ring #3 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #3**

15106138 ADMA_RX_CRX_IDX_3 RX Ring #3 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_CRX_IDX											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510613C ADMA_RX_DRX_IDX_3 RX Ring #3 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106140 ADMA_RX_BASE_PTR_4 RX Ring #4 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #4 (4-DW aligned address)**

15106144 ADMA_RX_MAX_CNT_4 RX Ring #4 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #4**

15106148 ADMA_RX_CRX_IDX_4 RX Ring #4 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510614C ADMA_RX_DRX_IDX_4 RX Ring #4 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106150 ADMA_RX_BASE_PTR_5 RX Ring #5 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #5 (4-DW aligned address)**

15106154 ADMA_RX_MAX_CNT_5 RX Ring #5 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #5**

15106158 ADMA_RX_CRX_IDX_5 RX Ring #5 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510615C ADMA_RX_DRX_IDX_5 RX Ring #5 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106160 ADMA_RX_BASE_PTR_6 RX Ring #6 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #6 (4-DW aligned address)**

15106164 ADMA_RX_MAX_CNT_6 RX Ring #6 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX_MAX_CNT											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #6**

15106168 ADMA_RX_CRX_IDX_6 RX Ring #6 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510616C **ADMA_RX_DRX_IDX_6** **RX Ring #6 DMA Pointer** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106170 ADMA_RX_BASE_PTR_7 RX Ring #7 Base Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BASE_PTR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BASE_PTR	**Point to the base address of RX Ring #7 (4-DW aligned address)**

15106174 ADMA_RX_MAX_CNT_7 RX Ring #7 Maximum Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_MAX_CNT**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_MAX_CNT	**The maximum number of RXD count in RX Ring #7**

15106178 ADMA_RX_CRX_IDX_7 RX Ring #7 CPU Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_CRX_IDX**											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_CRX_IDX	**Point to the next RXD CPU wants to use**

1510617C ADMA_RX_DRX_IDX_7 RX Ring #7 DMA Pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RX_DRX_IDX**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	RX_DRX_IDX	**Point to the next RXD DMA wants to use**

15106200 ADMA_INFO ADMA Information 4C000804

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					INDEX_WIDTH				BASE_PTR_WIDTH							
Type					RO				RO							
Reset					1	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_RING_NUM								TX_RING_NUM							
Type	RO								RO							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
27:24	INDEX_WIDTH	**Ring index width**
23:16	BASE_PTR_WIDTH	**Base pointer width, x** Base_addr[31:32-x] is shared with all ring base addresses. Only ring #0 base address[31:32-x] field is writable. [Note]: "0" means no bit of base_address is shared.
15:8	RX_RING_NUM	**RX ring number**
7:0	TX_RING_NUM	**TX ring number**

15106204 ADMA_GLO_CFG ADMA Global Configuration 50404C70

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_2B_OFFSET	CSR_CLKGATE_BYP	BYTE_SWAP	DEC_WCOMP	PKT_WCOMP	BYTE_SWAP_BIT_SEL	BIG_ENDIAN_BIT_SEL									
Type	RW	RW	RW	RW	RW	RW	RW									
Reset	0	1	0	1	0	0	0									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MUTLI_CNT				MULTI_EN	CHK_DDONE		RX_DMA_LRO_EN	BIG_ENDIAN	TX_WB_DDONE	DMA_BT_SIZE		RX_DMA_BUSY	RX_DMA_EN	TX_DMA_BUSY	TX_DMA_EN
Type	RW				RW	RW		RW	RW	RW	RW		RO	RW	RO	RW
Reset	0	1	0	0	1	1		0	0	1	1	1	0	0	0	0

Bit(s)	Name	Description
31	RX_2B_OFFSET	**Prepend 2 bytes to RX-buffer (packet) for aligning IP header with 32-bit boundary.** Default MAC header is 14 bytes 0: Disable 2 bytes prepended 1: Enable 2 bytes prepended
30	CSR_CLKGATE_BYP	**Bypass clock gating** 0: DMA clock is gated as idle 1: DMA clock is free-running
29	BYTE_SWAP	**Byte Swap** 0: DMA will not do byte swapping for TX/RX packet descriptor 1: DMA will do byte swapping for TX/RX packet descriptor
28	DEC_WCOMP	**DMA checks WDONE or WCOMPLETE when updating descriptor into DRAM** 0: DMA checks WDONE when updating descriptor into DRAM 1: DMA checks WCOMPLETE when updating descriptor into DRAM
27	PKT_WCOMP	**RX_DMA checks WDONE or WCOMPLETE when writing packet into DRAM** 0: RX_DMA checks WDONE when writing packet into DRAM 1: RX_DMA checks WCOMPLETE when writing packet into DRAM
26	BYTE_SWAP_BIT_SEL	**Bit selection for byte swap function** 0: 64-bit byte swap mode 1: 32-bit byte swap mode
25	BIG_ENDIAN_BIT_SEL	**Bit selection for endian control** 0: 64-bit endian mode

Bit(s)	Name	Description
		1: 32-bit endian mode
15:12	MUTLI_CNT	**Number of TX DMA read outstanding transactions when ADMA_GLO_CFG[11] = 1'b1.** 4'h1: Single-issue 4'h2: 2 read transactions 4'h4: 4 read transactions 4'hf: 15 read transactions
11	MULTI_EN	**Enable TX DAM AXI read outstanding transaction** 0: Disable TX DMA read outstanding transaction 1: Enable TX DMA read outstanding transaction
10	CHK_DDONE	**Enable DMA checking DDONE; if DDONE = 1, DMA will enter Coherence protection** 0: Bypass DDONE checking 1: Check DDONE
8	RX_DMA_LRO_EN	**Enable ADMA RX DMA LRO** 0: Disable RX LRO Ring 1: Enable RX LRO Ring
7	BIG_ENDIAN	**Big endian** 0: DMA will not do byte swapping for TX/RX packet header and payload 1: DMA will do byte swapping for TX/RX packet header and payload
6	TX_WB_DDONE	0: Disable TX_DMA writing back DDONE into TXD 1: Enable TX_DMA writing back DDONE into TXD
5:4	DMA_BT_SIZE	**The burst size of ADMA** 0: Reserved 1: 8 DWORDs (32-byte) 2: 16 DWORDs (64-byte) 3: 32 DWORDs (128-byte)
3	RX_DMA_BUSY	0: RX_DMA is not busy 1: RX_DMA is busy
2	RX_DMA_EN	0: Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet and then stop) 1: Enable RX_DMA
1	TX_DMA_BUSY	0: TX_DMA is not busy

Bit(s)	Name	Description
		1: TX_DMA is busy
0	TX_DMA_EN	0: Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet and then stop) 1: Enable TX_DMA

15106208 ADMA_RST_IDX ADMA Reset Index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									RST_DRX_IDX7	RST_DRX_IDX6	RST_DRX_IDX5	RST_DRX_IDX4	RST_DRX_IDX3	RST_DRX_IDX2	RST_DRX_IDX1	RST_DRX_IDX0
Type									WO	WO	WO	WO	WO	WO	WO	WO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RST_DTX_IDX3	RST_DTX_IDX2	RST_DTX_IDX1	RST_DTX_IDX0
Type													WO	WO	WO	WO
Reset													0	0	0	0

Bit(s)	Name	Description
23	RST_DRX_IDX7	**Write 1 to reset RX_DMA RX_IDX7 to 0**
22	RST_DRX_IDX6	**Write 1 to reset RX_DMA RX_IDX6 to 0**
21	RST_DRX_IDX5	**Write 1 to reset RX_DMA RX_IDX5 to 0**
20	RST_DRX_IDX4	**Write 1 to reset RX_DMA RX_IDX4 to 0**
19	RST_DRX_IDX3	**Write 1 to reset RX_DMA RX_IDX3 to 0**
18	RST_DRX_IDX2	**Write 1 to reset RX_DMA RX_IDX2 to 0**
17	RST_DRX_IDX1	**Write 1 to reset RX_DMA RX_IDX1 to 0**
16	RST_DRX_IDX0	**Write 1 to reset RX_DMA RX_IDX0 to 0**
3	RST_DTX_IDX3	**Write 1 to reset TX_DMA TX_IDX3 to 0**
2	RST_DTX_IDX2	**Write 1 to reset TX_DMA TX_IDX2 to 0**
1	RST_DTX_IDX1	**Write 1 to reset TX_DMA TX_IDX1 to 0**
0	RST_DTX_IDX0	**Write 1 to reset TX_DMA TX_IDX0 to 0**

15106210 ADMA_RX_CFG ADMA Rx DMA Configuration 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRO_SDL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													FREEQ_THRES			
Type													RW			
Reset													0	0	1	0

Bit(s)	Name	Description
31:16	LRO_SDL	**ADMA LRO Free Buffer SDL**
3:0	FREEQ_THRES	**RX free queue threshold** ADMA will stop DMA interface when left RX descriptors reach this threshold

15106220 ADMA_INT_STATUS ADMA Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DONE_DLY_INT7	RX_DONE_DLY_INT6	RX_DONE_DLY_INT5	RX_DONE_DLY_INT4	RX_DONE_DLY_INT3	RX_DONE_DLY_INT2	RX_DONE_DLY_INT1	RX_DONE_DLY_INT0	RX_DONE_INT7	RX_DONE_INT6	RX_DONE_INT5	RX_DONE_INT4	RX_DONE_INT3	RX_DONE_INT2	RX_DONE_INT1	RX_DONE_INT0
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT					TX_DONE_DLY_INT3	TX_DONE_DLY_INT2	TX_DONE_DLY_INT1	TX_DONE_DLY_INT0	TX_DONE_INT3	TX_DONE_INT2	TX_DONE_INT1	TX_DONE_INT0
Type	W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_DONE_DLY_INT7	**RX ring #7 packet receive delay interrupt**
30	RX_DONE_DLY_INT6	**RX ring #6 packet receive delay interrupt**
29	RX_DONE_DLY_INT5	**RX ring #5 packet receive delay interrupt**
28	RX_DONE_DLY_INT4	**RX ring #4 packet receive delay interrupt**
27	RX_DONE_DLY_INT3	**RX ring #3 packet receive delay interrupt**
26	RX_DONE_DLY_INT2	**RX ring #2 packet receive delay interrupt**
25	RX_DONE_DLY_INT1	**RX ring #1 packet receive delay interrupt**
24	RX_DONE_DLY_INT0	**RX ring #0 packet receive delay interrupt**
23	RX_DONE_INT7	**RX ring #7 packet receive interrupt**
22	RX_DONE_INT6	**RX ring #6 packet receive interrupt**
21	RX_DONE_INT5	**RX ring #5 packet receive interrupt**
20	RX_DONE_INT4	**RX ring #4 packet receive interrupt**
19	RX_DONE_INT3	**RX ring #3 packet receive interrupt**
18	RX_DONE_INT2	**RX ring #2 packet receive interrupt**
17	RX_DONE_INT1	**RX ring #1 packet receive interrupt**
16	RX_DONE_INT0	**RX ring #0 packet receive interrupt**
15	RX_COHERENT	**RX_DMA finds data coherent event while checking DDONE bit.**
14	RX_DLY_INT	**Summary of the whole ADMA RX related interrupts.**
13	TX_COHERENT	**TX_DMA finds data coherent event while checking DDONE bit.**
12	TX_DLY_INT	**Summary of the whole ADMA TX related interrupts.**
7	TX_DONE_DLY_INT3	**TX ring #3 packet transmit delay interrupt**
6	TX_DONE_DLY_INT2	**TX ring #2 packet transmit delay interrupt**
5	TX_DONE_DLY_INT1	**TX ring #1 packet transmit delay interrupt**
4	TX_DONE_DLY_INT0	**TX ring #0 packet transmit delay interrupt**

Bit(s)	Name	Description
3	TX_DONE_INT3	**TX ring #3 packet transmit interrupt**
2	TX_DONE_INT2	**TX ring #2 packet transmit interrupt**
1	TX_DONE_INT1	**TX ring #1 packet transmit interrupt**
0	TX_DONE_INT0	**TX ring #0 packet transmit interrupt**

15106228 ADMA_INT_MASK ADMA Interrupt Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DONE_DLY_INT7	RX_DONE_DLY_INT6	RX_DONE_DLY_INT5	RX_DONE_DLY_INT4	RX_DONE_DLY_INT3	RX_DONE_DLY_INT2	RX_DONE_DLY_INT1	RX_DONE_DLY_INT0	RX_DONE_INT7	RX_DONE_INT6	RX_DONE_INT5	RX_DONE_INT4	RX_DONE_INT3	RX_DONE_INT2	RX_DONE_INT1	RX_DONE_INT0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_COHERENT	RX_DLY_INT	TX_COHERENT	TX_DLY_INT					TX_DONE_DLY_INT3	TX_DONE_DLY_INT2	TX_DONE_DLY_INT1	TX_DONE_DLY_INT0	TX_DONE_INT3	TX_DONE_INT2	TX_DONE_INT1	TX_DONE_INT0
Type	RW	RW	RW	RW					RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RX_DONE_DLY_INT7	**RX ring #7 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
30	RX_DONE_DLY_INT6	**RX ring #6 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
29	RX_DONE_DLY_INT5	**RX ring #5 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
28	RX_DONE_DLY_INT4	**RX ring #4 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
27	RX_DONE_DLY_INT3	**RX ring #3 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
26	RX_DONE_DLY_INT2	**RX ring #2 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
25	RX_DONE_DLY_INT1	**RX ring #1 packet receive delay interrupt** 0: Disable interrupt 1: Enable interrupt
24	RX_DONE_DLY_INT0	**RX ring #0 packet receive delay interrupt** 0: Disable interrupt

Bit(s)	Name	Description
		1: Enable interrupt
23	RX_DONE_INT7	**RX ring #7 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
22	RX_DONE_INT6	**RX ring #6 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
21	RX_DONE_INT5	**RX ring #5 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
20	RX_DONE_INT4	**RX ring #4 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
19	RX_DONE_INT3	**RX ring #3 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
18	RX_DONE_INT2	**RX ring #2 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
17	RX_DONE_INT1	**RX ring #1 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
16	RX_DONE_INT0	**RX ring #0 packet receive interrupt** 0: Disable interrupt 1: Enable interrupt
15	RX_COHERENT	**RX_DMA finds data coherent event while checking DDONE bit.** 0: Disable interrupt 1: Enable interrupt
14	RX_DLY_INT	**Summary of the whole ADMA RX related interrupts.** 0: Disable interrupt 1: Enable interrupt
13	TX_COHERENT	**TX_DMA finds data coherent event while checking DDONE bit.**

Bit(s)	Name	Description
		0: Disable interrupt
		1: Enable interrupt
12	TX_DLY_INT	**Summary of the whole ADMA TX related interrupts.**
		0: Disable interrupt
		1: Enable interrupt
7	TX_DONE_DLY_INT3	**TX ring #3 packet transmit delay interrupt**
		0: Disable interrupt
		1: Enable interrupt
6	TX_DONE_DLY_INT2	**TX ring #2 packet transmit delay interrupt**
		0: Disable interrupt
		1: Enable interrupt
5	TX_DONE_DLY_INT1	**TX ring #1 packet transmit delay interrupt**
		0: Disable interrupt
		1: Enable interrupt
4	TX_DONE_DLY_INT0	**TX ring #0 packet transmit delay interrupt**
		0: Disable interrupt
		1: Enable interrupt
3	TX_DONE_INT3	**TX ring #3 packet transmit interrupt**
		0: Disable interrupt
		1: Enable interrupt
2	TX_DONE_INT2	**TX ring #2 packet transmit interrupt**
		0: Disable interrupt
		1: Enable interrupt
1	TX_DONE_INT1	**TX ring #1 packet transmit interrupt**
		0: Disable interrupt
		1: Enable interrupt
0	TX_DONE_INT0	**TX ring #0 packet transmit interrupt**
		0: Disable interrupt
		1: Enable interrupt

15106240 ADMA_INT_STS_GRP0 ADMA Interrupt Status Group 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP0	**Interrupt group 0 status, this information already "and" with "~ADMA_INT_GRP1 & ~ADMA_INT_GRP2"** Each bit definition is the same as "ADMA_INT_STATUS"

15106244 ADMA_INT_STS_GRP1 ADMA Interrupt Status Group 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP1	**Interrupt group 1 status, this information already "and" with "ADMA_INT_GRP1"** Each bit definition is the same as "ADMA_INT_STATUS"

15106248 ADMA_INT_STS_GRP2 ADMA Interrupt Status Group 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP2	**Interrupt group 2 status, this information already "and" with "ADMA_INT_GRP2"** Each bit definition is the same as "ADMA_INT_STATUS"

1510624C **ADMA_INT_STS_GRP3** **ADMA Interrupt Status Group 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_STS_GRP3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_STS_GRP3	**Interrupt group 3 status, this information already "and" with "ADMA_INT_GRP3"** Each bit definition is the same as "ADMA_INT_STATUS"

15106250 ADMA_INT_GRP1 ADMA Interrupt Group 1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_GRP1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_GRP1	**Interrupt group 1 assignment.** Each bit's definition is the same as "ADMA_INT_STATUS" 0: Leave to ADMA interrupt group 0, if (ADMA_INT_GRP1[n]==0 & ADMA_INT_GRP2[n]==0 & ADMA_INT_GRP3[n]==0) 1: Assign to ADMA interrupt group 1

15106254 ADMA_INT_GRP2 ADMA Interrupt Group 2 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_GRP2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_GRP2	**Interrupt group 2 assignment.** Each bit's definition is the same as "ADMA_INT_STATUS" 0: Leave to ADMA interrupt group 0, if (ADMA_INT_GRP1[n]==0 & ADMA_INT_GRP2[n]==0 & ADMA_INT_GRP3[n]==0) 1: Assign to ADMA interrupt group 2

15106258 ADMA_INT_GRP3 ADMA Interrupt Group 3 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ADMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADMA_INT_GRP3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ADMA_INT_GRP3	**Interrupt group 3 assignment.** Each bit's definition is the same as "ADMA_INT_STATUS" 0: Leave to ADMA interrupt group 0, if (ADMA_INT_GRP1[n]==0 & ADMA_INT_GRP2[n]==0 & ADMA_INT_GRP3[n]==0) 1: Assign to ADMA interrupt group 3

15106260 ADMA_BUS_CFG ADMA AXI BUS Configuration 00000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						AXI_CTRL_UPDATED	AXI_R_BUSY	AXI_W_BUSY		AXI_LOCK_ERROR	AXI_ERRMID_SET_RIRQ	AXI_ERRMID_SET_BIRQ	AXI_OUTSTANDING_EXTEND	AXI_QOS_ON		AXI_CG_DISABLE
Type						RO	RO	RO		RO	RO	RO	RW	RW		RW
Reset						1	0	0		0	0	0	0	0		0

Bit(s)	Name	Description
10	AXI_CTRL_UPDATED	**Master interface control signal updated status**
9	AXI_R_BUSY	**Read transaction not completes**
8	AXI_W_BUSY	**Write transaction not completes**
6	AXI_LOCK_ERROR	**Detect lock error**
5	AXI_ERRMID_SET_RIRQ	**Detect error MID from slave in R channel**
4	AXI_ERRMID_SET_BIRQ	**Detect error MID from slave in B channel**
3	AXI_OUTSTANDING_EXTEND	**Auto add extra outstanding for QoS command** 0: Disable 1: Enable
2	AXI_QOS_ON	**Enable QoS function** 0: Disable 1: Enable
0	AXI_CG_DISABLE	**Disable auto clock gating of AXI component** 0: Disable 1: Enable

15106264 ADMA_ULTRA_CFG ADMA AXI ULTRA Configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AXI_ULTRA_EN					AXI_ULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AXI_PREULTRA_EN					AXI_PREULTRA_THRES										
Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AXI_ULTRA_EN	**Enable AXI Ultra transaction** 0: Disable 1: Enable
26:16	AXI_ULTRA_THRES	**AXI Ultra threshold.** If CDM TX free FIFO count is bigger than AXI_ULTRA_THRES, it will trigger AXI Ultra transaction when AXI_ULTRA_EN = 1.
15	AXI_PREULTRA_EN	**Enable AXI Pre-ultra transaction** 0: Disable 1: Enable
10:0	AXI_PREULTRA_THRES	**AXI Pre-ultra threshold.** If CDM TX free FIFO count is bigger than AXI_PREULTRA_THRES, it will trigger AXI Pre-ultra transaction when AXI_PREULTRA_EN = 1.

15106290 ADMA_INT_STATUS_0 ADMA Interrupt Status 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	**Interrupt Status** Bitmap same as ADMA_INT_STATUS

15106294 ADMA_INT_MASK_0 ADMA Interrupt Mask 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	**Interrupt Mask** Bitmap same as ADMA_INT_MASK

15106298 ADMA_INT_STATUS_1 ADMA Interrupt Status 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	**Interrupt Status** Bitmap same as ADMA_INT_STATUS

1510629C ADMA_INT_MASK_1 ADMA Interrupt Mask 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	**Interrupt Mask** Bitmap same as ADMA_INT_MASK

151062A0 **ADMA_INT_STATUS_2** **ADMA Interrupt Status 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	**Interrupt Status** Bitmap same as ADMA_INT_STATUS

151062A4 ADMA_INT_MASK_2 ADMA Interrupt Mask 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	**Interrupt Mask** Bitmap same as ADMA_INT_MASK

151062A8 ADMA_INT_STATUS_3 ADMA Interrupt Status 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_STATUS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_STATUS	**Interrupt Status** Bitmap same as ADMA_INT_STATUS

151062AC **ADMA_INT_MASK_3** **ADMA Interrupt Mask 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_MASK															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_MASK	**Interrupt Mask** Bitmap same as ADMA_INT_MASK

151062B0 ADMA_TX_DELAY_INT_CFG_0 ADMA Tx Delay Interrupt Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING1_TXDLY_INT_EN	RING1_TXMAX_PINT							RING1_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING0_TXDLY_INT_EN	RING0_TXMAX_PINT							RING0_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING1_TXDLY_INT_EN	**Enable delay interrupt mechanism for Tx Ring 1** 0: Disable 1: Enable
30:24	RING1_TXMAX_PINT	**Specified Max. number of pending interrupts** [Note] Resetting to 0 can disable pending interrupt count check.
23:16	RING1_TXMAX_PTIME	**Specified Max. pending time** [Note] Resetting to 0 can disable pending interrupt time check.
15	RING0_TXDLY_INT_EN	**Enable delay interrupt mechanism for Tx Ring 0** 0: Disable 1: Enable
14:8	RING0_TXMAX_PINT	**Specified Max. number of pending interrupts** [Note] Resetting to 0 can disable pending interrupt count check.
7:0	RING0_TXMAX_PTIME	**Specified Max. pending time** [Note] Resetting to 0 can disable pending interrupt time check.

151062B4 ADMA_TX_DELAY_INT_CFG_1 ADMA Tx Delay Interrupt Configuration 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING3_TXDLY_INT_EN	RING3_TXMAX_PINT							RING3_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING2_TXDLY_INT_EN	RING2_TXMAX_PINT							RING2_TXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING3_TXDLY_INT_EN	**Enable delay interrupt mechanism for Tx Ring 3** 0: Disable 1: Enable
30:24	RING3_TXMAX_PINT	**Specified Max. number of pending interrupts** [Note] Resetting to 0 can disable pending interrupt count check.
23:16	RING3_TXMAX_PTIME	**Specified Max. pending time** [Note] Resetting to 0 can disable pending interrupt time check.
15	RING2_TXDLY_INT_EN	**Enable delay interrupt mechanism for Tx Ring 2** 0: Disable 1: Enable
14:8	RING2_TXMAX_PINT	**Specified Max. number of pending interrupts** [Note] Resetting to 0 can disable pending interrupt count check.
7:0	RING2_TXMAX_PTIME	**Specified Max. pending time** [Note] Resetting to 0 can disable pending interrupt time check.

151062C0 ADMA_RX_DELAY_INT_CFG_0 ADMA Rx Delay Interrupt Configuration 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING_4_7_RXDLY_INT_EN	RING_4_7_RXMAX_PINT							RING_4_7_RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RING_0_3_RXDLY_INT_EN	RING_0_3_RXMAX_PINT							RING_0_3_RXMAX_PTIME							
Type	RW	RW							RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	RING_4_7_RXDLY_INT_EN	**Enable delay interrupt mechanism for Rx Ring 4~7** 0: Disable 1: Enable
30:24	RING_4_7_RXMAX_PINT	**Specified Max. number of pending interrupts for Rx Ring 4~7** [Note] Resetting to 0 can disable pending interrupt count check.
23:16	RING_4_7_RXMAX_PTIME	**Specified Max. pending time for Rx Ring 4~7** [Note] Resetting to 0 can disable pending interrupt time check.
15	RING_0_3_RXDLY_INT_EN	**Enable delay interrupt mechanism for Rx Ring 0~3** 0: Disable 1: Enable
14:8	RING_0_3_RXMAX_PINT	**Specified Max. number of pending interrupts for Rx Ring 0~3** [Note] Resetting to 0 can disable pending interrupt count check.
7:0	RING_0_3_RXMAX_PTIME	**Specified Max. pending time for Rx Ring 0~3** [Note] Resetting to 0 can disable pending interrupt time check.

5.5 LRO

5.5.1 Register Definition

Module name: LRO2 Base address: (+0x15106400)

Address	Name	Width	Register Function
15106408	LRO2_CTRL_DW0	32	Control CRs
1510640C	LRO2_CTRL_DW1	32	Control CRs
15106410	LRO2_CTRL_DW2	32	Control CRs
15106414	LRO2_CTRL_DW3	32	Control CRs
15106418	LRO2_CTRL_DW4	32	Control CRs
1510641C	LRO2_ALT_SCORE_DELTA	32	LRO2 ALT Score Delta
15106420	LRO2_TIMEOUT_FLAG	32	LRO2 Timeout Flag
15106430	LRO2_RING1_STS	32	LRO2 Ring1 Status
15106434	LRO2_RING2_STS	32	LRO2 Ring2 Status
15106438	LRO2_RING3_STS	32	LRO2 Ring3 Status
1510643C	LRO2_RING4_STS	32	LRO2 Ring4 Status
15106450	LRO2_RING1_STP_DTP_DW	32	Source TCP Port Number
15106454	LRO2_RING1_DIP_DW0	32	Destination IP address[31:0]
15106458	LRO2_RING1_DIP_DW1	32	Destination IP address[63:32]
1510645C	LRO2_RING1_DIP_DW2	32	Destination IP address[95:64]
15106460	LRO2_RING1_DIP_DW3	32	Destination IP address[127:96]
15106464	LRO2_RING1_SIP_DW0	32	Source IP address[31:0]
15106468	LRO2_RING1_SIP_DW1	32	Source IP address[63:32]
1510646C	LRO2_RING1_SIP_DW2	32	Source IP address[95:64]
15106470	LRO2_RING1_SIP_DW3	32	Source IP address[127:96]
15106474	LRO2_RING1_CTRL_DW0	32	l2_vlan_vid_l2_l
15106478	LRO2_RING1_CTRL_DW1	32	RX ring age time[9:0]
1510647C	LRO2_RING1_CTRL_DW2	32	LRO2_MAX_AGGREGATED_CNT_L
15106480	LRO2_RING1_CTRL_DW3	32	Reserved
15106490	LRO2_RING2_STP_DTP_DW	32	Source TCP Port Number
15106494	LRO2_RING2_DIP_DW0	32	Destination IP address[31:0]
15106498	LRO2_RING2_DIP_DW1	32	Destination IP address[63:32]
1510649C	LRO2_RING2_DIP_DW2	32	Destination IP address[95:64]
151064A0	LRO2_RING2_DIP_DW3	32	Destination IP address[127:96]
151064A4	LRO2_RING2_SIP_DW0	32	Source IP address[31:0]
151064A8	LRO2_RING2_SIP_DW1	32	Source IP address[63:32]
151064AC	LRO2_RING2_SIP_DW2	32	Source IP address[95:64]
151064B0	LRO2_RING2_SIP_DW3	32	Source IP address[127:96]
151064B4	LRO2_RING2_CTRL_DW0	32	l2_vlan_vid_l2_l
151064B8	LRO2_RING2_CTRL_DW1	32	RX ring age time[9:0]
151064BC	LRO2_RING2_CTRL_DW2	32	LRO2_MAX_AGGREGATED_CNT_L
151064C0	LRO2_RING2_CTRL_DW3	32	Reserved
151064D0	LRO2_RING3_STP_DTP_DW	32	Source TCP Port Number
151064D4	LRO2_RING3_DIP_DW0	32	Destination IP address[31:0]
151064D8	LRO2_RING3_DIP_DW1	32	Destination IP address[63:32]
151064DC	LRO2_RING3_DIP_DW2	32	Destination IP address[95:64]
151064E0	LRO2_RING3_DIP_DW3	32	Destination IP address[127:96]
151064E4	LRO2_RING3_SIP_DW0	32	Source IP address[31:0]
151064E8	LRO2_RING3_SIP_DW1	32	Source IP address[63:32]
151064EC	LRO2_RING3_SIP_DW2	32	Source IP address[95:64]
151064F0	LRO2_RING3_SIP_DW3	32	Source IP address[127:96]
151064F4	LRO2_RING3_CTRL_DW0	32	l2_vlan_vid_l2_l

Address	Name	Width	Register Function
151064F8	LRO2_RING3_CTRL_DW1	32	RX ring age time[9:0]
151064FC	LRO2_RING3_CTRL_DW2	32	LRO2_MAX_AGGREGATED_CNT_L
15106500	LRO2_RING3_CTRL_DW3	32	Reserved
15106510	LRO2_RING4_STP_DTP_DW	32	Source TCP Port Number
15106514	LRO2_RING4_DIP_DW0	32	Destination IP address[31:0]
15106518	LRO2_RING4_DIP_DW1	32	Destination IP address[63:32]
1510651C	LRO2_RING4_DIP_DW2	32	Destination IP address[95:64]
15106520	LRO2_RING4_DIP_DW3	32	Destination IP address[127:96]
15106524	LRO2_RING4_SIP_DW0	32	Source IP address[31:0]
15106528	LRO2_RING4_SIP_DW1	32	Source IP address[63:32]
1510652C	LRO2_RING4_SIP_DW2	32	Source IP address[95:64]
15106530	LRO2_RING4_SIP_DW3	32	Source IP address[127:96]
15106534	LRO2_RING4_CTRL_DW0	32	l2_vlan_vid_l2_l
15106538	LRO2_RING4_CTRL_DW1	32	RX ring age time[9:0]
1510653C	LRO2_RING4_CTRL_DW2	32	LRO2_MAX_AGGREGATED_CNT_L
15106540	LRO2_RING4_CTRL_DW3	32	Reserved

15106408 LRO2_CTRL_DW0 Control CRs F0884000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RING_RELINGUISH_DONE				RING_RELINGUISH_REQ				cr_l4_ctrl_psh_en	lro_crsn_bnw	cr_alt_score_mode	first_ineligible_pkt_redirect_en	L3_CKS_UPD_EN	SDL		
Type	RO				RW				RW	RW	RW	RW	RW	RW		
Reset	1	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDL													MULTIPLE_NON_RING_EN	IPv6_EN	EN
Type	RW													RW	RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	RING_RELINGUISH_DONE	**Indicate there are relinquished rings**
27:24	RING_RELINGUISH_REQ	**FW requests to flush aggregated packets by writing 1, then 0**
23	cr_l4_ctrl_psh_en	0: Disable l4 PSH LRO eligibility check 1: Push asserted is LRO ineligible
22	lro_crsn_bnw	**lro_crsn_bnw** 1: Blacklist, 0: Whitelist
21	cr_alt_score_mode	0: Throughput (byte count) 1: Packet count
20	first_ineligible_pkt_redirect_en	**In order to save one LRO RXD with large sdl0 (64KB), it is better to redirect ineligible packets into Normal ring when the hit LRO ring is clean and empty without existing aggregated packets.**
19	L3_CKS_UPD_EN	**Enable ipv4 checksum update** 1: Enable, 0: Disable
18:3	SDL	**Max aggregated packet length**
2	MULTIPLE_NON_RING_EN	**To enable multiple non-LRO Rx rings** 0: Multiple non-LRO Rx ring disable 1: Multiple non-LRO Rx ring enable
1	IPv6_EN	**Enable bit for IPv6 packet LRO** 0: Disable LRO to IPv6 flow 1: Enable LRO to IPv6 flow
0	EN	**Enable bit to activate RX LRO feature** 0: Disable LRO 1: Enable LRO

Bit(s)	Name	Description

1510640C LRO2_CTRL_DW1 Control CRs 1F1E1F1E

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CPU_REASON															
Type	RW															
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPU_REASON															
Type	RW															
Reset	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	0

Bit(s)	Name	Description
31:0	CPU_REASON	**CPU reason code set (5b per reason).**

15106410 LRO2_CTRL_DW2 Control CRs 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTO_LEARN_ELIGIBLE_THRESHOLD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTO_LEARN_ELIGIBLE_THRESHOLD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AUTO_LEARN_ELIGIBLE_THRESHOLD	**Min threshold to become a candidate for LRO aggregation**

15106414 LRO2_CTRL_DW3 Control CRs 05F20F00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_RXD_SDL0															
Type	RW															
Reset	0	0	0	0	0	1	0	1	1	1	1	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAND_WGT_IDX		VLAN_VID_CMP_DEPTH		VLAN_EN				REV							
Type	RW		RW		RW				RW							
Reset	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	MIN_RXD_SDL0	**The least remaining room of SDL0 in RXD for LRO aggregation.** It should be greater than the maximum size of packet RX MAC can accept without dropping. That is, MIN_RXD_SDL0 MUST be equal to or greater than MAX_RX_JUMBO/MAC_RX_PKT_LEN fields in CR MAC_P*_MCR(address : 1B11_0100)
15:14	CAND_WGT_IDX	**Candidate weight index** The estimated candidate weight value = throughput >> {CAND_WGT_IDX,1'b0}
13:12	VLAN_VID_CMP_DEPTH	**Determine depth of VLAN ID needed to be compared**
11:8	VLAN_EN	**Support max 4-depth VLAN for LRO**
7:0	REV	**Reserved**

15106418 LRO2_CTRL_DW4 Control CRs 00008100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															SPC_TAG_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	REV	**Reserved**
16	SPC_TAG_EN	**Enable special tag**
15:0	EXT_TPID	**User extended TPID**

1510641C LRO2_ALT_SCORE_DELTA LRO2 ALT Score Delta 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ALT_SCORE_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALT_SCORE_DELTA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ALT_SCORE_DELTA	**To add a delta before determining whether to replace or not.**

15106420 LRO2_TIMEOUT_FLAG LRO2 Timeout Flag 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0							AGE_TIMEOUT				AGG_TIMEOUT				BUSY
Type	RO							RC				RC				RC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV0	**Reserved**
8:5	AGE_TIMEOUT	**If the ring times out, the related bit will be on. After CR reading, the bit will be cleared.**
4:1	AGG_TIMEOUT	**If the ring times out, the related bit will be on. After CR reading, the bit will be cleared.**
0	BUSY	**LRO busy**

15106430 LRO2_RING1_STS LRO2 Ring1 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	**Reserved**
8	AGG_CNT_ZERO	1'b1: There is no aggregated packet 1'b0: There are already aggregated packets
7:0	AGG_CNT	Aggregated packet count number

15106434 LRO2_RING2_STS LRO2 Ring2 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	**Reserved**
8	AGG_CNT_ZERO	1'b1: There is no aggregated packet 1'b0: There are already aggregated packets
7:0	AGG_CNT	Aggregated packet count number

15106438 LRO2_RING3_STS LRO2 Ring3 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	**Reserved**
8	AGG_CNT_ZERO	1'b1: There is no aggregated packet 1'b0: There are already aggregated packets
7:0	AGG_CNT	**Current aggregated packet count number**

1510643C LRO2_RING4_STS LRO2 Ring4 Status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV							AGG_CNT_ZERO	AGG_CNT							
Type	RO							RO	RO							
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:9	REV	Reserved
8	AGG_CNT_ZERO	1'b1: There is no aggregated packet 1'b0: There are already aggregated packets
7:0	AGG_CNT	**Current aggregated packet count number**

15106450 LRO2_RING1_STP_DTP_DW Source TCP Port Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	**Source TCP port number**
15:0	DTP	**Destination TCP port number**

15106454 LRO2_RING1_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[31:0]**

15106458 LRO2_RING1_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[63:32]**

1510645C LRO2_RING1_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[95:64]**

15106460 LRO2_RING1_DIP_DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[127:96]**

15106464 LRO2_RING1_SIP_DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[31:0]**

15106468 LRO2_RING1_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[63:32]**

1510646C LRO2_RING1_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[95:64]**

15106470 LRO2_RING1_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[127:96]**

15106474 LRO2_RING1_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L						VLAN_VID_L1									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_IPV4_EN	FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	**VLAN VID of four forced port LRO rings**
25:14	VLAN_VID_L1	**To validate IPv4 flow of forced port LRO ring**
13:2	VLAN_VID_L0	**To validate IPv4 flow of forced port LRO ring**
1	FRCP_IPV4_EN	**To validate IPv4 flow of forced port LRO ring**
0	FRCP_IPV6_EN	**To validate IPv6 flow of forced port LRO ring**

15106478 LRO2_RING1_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	**Age time to flush LRO ring**
21	VLAN_VLD_L3	**Valid bit of VLAN VID for four forced port LRO ring**
20	VLAN_VLD_L2	**Valid bit of VLAN VID for four forced port LRO ring**
19	VLAN_VLD_L1	**Valid bit of VLAN VID for four forced port LRO ring**
18	VLAN_VLD_L0	**Valid bit of VLAN VID for four forced port LRO ring**
17:6	VLAN_VID_L3	**VLAN VID of four forced port LRO rings**
5:0	VLAN_VID_L2_H	**VLAN VID of four forced port LRO rings**

1510647C LRO2_RING1_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L						MAX_AGG_TIME									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	**To limit max aggregated packets**
25:10	MAX_AGG_TIME	**Maximum aggregation time to flush, = 0 to disable flush**
9	MYIP_VLD	**To validate programmed DIP information**
8	VLD	**To validate programmed flow information**
7:6	OP_MODE	**00: normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	AGE_TIME_H	**Age time to flush LRO ring, = 0 to disable flush**

15106480 LRO2_RING1_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**To limit max aggregated packets**
1:0	MAX_AGGREGATED_CNT_H	**To limit max aggregated packets**

15106490 LRO2_RING2_STP_DTP_DW Source TCP Port Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	**Source TCP port number**
15:0	DTP	**Destination TCP port number**

15106494 LRO2_RING2_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[31:0]**

15106498 LRO2_RING2_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[63:32]**

1510649C LRO2_RING2_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[95:64]**

151064A0 **LRO2_RING2_DIP_DW3** **Destination IP address[127:96]** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[127:96]**

151064A4 LRO2_RING2_SIP_DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[31:0]**

151064A8 LRO2_RING2_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[63:32]**

151064AC LRO2_RING2_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[95:64]**

151064B0 LRO2_RING2_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[127:96]**

151064B4 LRO2_RING2_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L						VLAN_VID_L1									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_IPV4_EN	FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	**VLAN VID of four forced port LRO rings**
25:14	VLAN_VID_L1	**To validate IPv4 flow of forced port LRO ring**
13:2	VLAN_VID_L0	**To validate IPv4 flow of forced port LRO ring**
1	FRCP_IPV4_EN	**To validate IPv4 flow of forced port LRO ring**
0	FRCP_IPV6_EN	**To validate IPv6 flow of forced port LRO ring**

151064B8 LRO2_RING2_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	**Age time to flush LRO ring**
21	VLAN_VLD_L3	**Valid bit of VLAN VID for four forced port LRO ring**
20	VLAN_VLD_L2	**Valid bit of VLAN VID for four forced port LRO ring**
19	VLAN_VLD_L1	**Valid bit of VLAN VID for four forced port LRO ring**
18	VLAN_VLD_L0	**Valid bit of VLAN VID for four forced port LRO ring**
17:6	VLAN_VID_L3	**VLAN VID of four forced port LRO rings**
5:0	VLAN_VID_L2_H	**VLAN VID of four forced port LRO rings**

151064BC LRO2_RING2_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L						MAX_AGG_TIME									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	**To limit max aggregated packets**
25:10	MAX_AGG_TIME	**Maximum aggregation time to flush, =0 to disable flush**
9	MYIP_VLD	**To validate programmed DIP information**
8	VLD	**To validate programmed flow information**
7:6	OP_MODE	**00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	AGE_TIME_H	**Age time to flush LRO ring, = 0 to disable flush**

151064C0 LRO2_RING2_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**To limit max aggregated packets**
1:0	MAX_AGGREGATED_CNT_H	**To limit max aggregated packets**

151064D0 LRO2_RING3_STP_DTP_DW Source TCP Port Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	**Source TCP port number**
15:0	DTP	**Destination TCP port number**

151064D4 LRO2_RING3_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[31:0]**

151064D8 LRO2_RING3_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[63:32]**

151064DC LRO2_RING3_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[95:64]**

151064E0 LRO2_RING3_DIP_DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[127:96]**

151064E4 LRO2_RING3_SIP_DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[31:0]**

151064E8 LRO2_RING3_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[63:32]**

151064EC LRO2_RING3_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[95:64]**

151064F0 LRO2_RING3_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[127:96]**

151064F4 LRO2_RING3_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L						VLAN_VID_L1									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_IPV4_EN	FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	**VLAN VID of four forced port LRO rings**
25:14	VLAN_VID_L1	**To validate IPv4 flow of forced port LRO ring**
13:2	VLAN_VID_L0	**To validate IPv4 flow of forced port LRO ring**
1	FRCP_IPV4_EN	**To validate IPv4 flow of forced port LRO ring**
0	FRCP_IPV6_EN	**To validate IPv6 flow of forced port LRO ring**

151064F8 LRO2_RING3_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	**Age time to flush LRO ring**
21	VLAN_VLD_L3	**Valid bit of VLAN VID for four forced port LRO ring**
20	VLAN_VLD_L2	**Valid bit of VLAN VID for four forced port LRO ring**
19	VLAN_VLD_L1	**Valid bit of VLAN VID for four forced port LRO ring**
18	VLAN_VLD_L0	**Valid bit of VLAN VID for four forced port LRO ring**
17:6	VLAN_VID_L3	**VLAN VID of four forced port LRO rings**
5:0	VLAN_VID_L2_H	**VLAN VID of four forced port LRO rings**

151064FC LRO2_RING3_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L						MAX_AGG_TIME									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	**To limit max aggregated packets**
25:10	MAX_AGG_TIME	**Maximum aggregation time to flush, = 0 to disable flush**
9	MYIP_VLD	**To validate programmed DIP information**
8	VLD	**To validate programmed flow information**
7:6	OP_MODE	**00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	AGE_TIME_H	**Age time to flush LRO ring, = 0 to disable flush**

15106500 LRO2_RING3_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**To limit max aggregated packets**
1:0	MAX_AGGREGATED_CNT_H	**To limit max aggregated packets**

15106510 LRO2_RING4_STP_DTP_DW Source TCP Port Number 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DTP															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STP	**Source TCP port number**
15:0	DTP	**Destination TCP port number**

15106514 LRO2_RING4_DIP_DW0 Destination IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[31:0]**

15106518 LRO2_RING4_DIP_DW1 Destination IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[63:32]**

1510651C LRO2_RING4_DIP_DW2 Destination IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[95:64]**

15106520 LRO2_RING4_DIP_DW3 Destination IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Destination IP address[127:96]**

15106524 LRO2_RING4_SIP_DW0 Source IP address[31:0] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[31:0]**

15106528 LRO2_RING4_SIP_DW1 Source IP address[63:32] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[63:32]**

1510652C LRO2_RING4_SIP_DW2 Source IP address[95:64] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[95:64]**

15106530 LRO2_RING4_SIP_DW3 Source IP address[127:96] 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Source IP address[127:96]**

15106534 LRO2_RING4_CTRL_DW0 l2_vlan_vid_l2_l 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	VLAN_VID_L2_L						VLAN_VID_L1									
Type	RW						RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L1		VLAN_VID_L0												FRCP_IPV4_EN	FRCP_IPV6_EN
Type	RW		RW												RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:26	VLAN_VID_L2_L	**VLAN VID of four forced port LRO rings**
25:14	VLAN_VID_L1	**To validate IPv4 flow of forced port LRO ring**
13:2	VLAN_VID_L0	**To validate IPv4 flow of forced port LRO ring**
1	FRCP_IPV4_EN	**To validate IPv4 flow of forced port LRO ring**
0	FRCP_IPV6_EN	**To validate IPv6 flow of forced port LRO ring**

15106538 LRO2_RING4_CTRL_DW1 RX ring age time[9:0] FFC00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AGE_TIME_L										VLAN_VLD_L3	VLAN_VLD_L2	VLAN_VLD_L1	VLAN_VLD_L0	VLAN_VID_L3	
Type	RW										RW	RW	RW	RW	RW	
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VLAN_VID_L3										VLAN_VID_L2_H					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:22	AGE_TIME_L	**Age time to flush LRO ring**
21	VLAN_VLD_L3	**Valid bit of VLAN VID for four forced port LRO ring**
20	VLAN_VLD_L2	**Valid bit of VLAN VID for four forced port LRO ring**
19	VLAN_VLD_L1	**Valid bit of VLAN VID for four forced port LRO ring**
18	VLAN_VLD_L0	**Valid bit of VLAN VID for four forced port LRO ring**
17:6	VLAN_VID_L3	**VLAN VID of four forced port LRO rings**
5:0	VLAN_VID_L2_H	**VLAN VID of four forced port LRO rings**

1510653C LRO2_RING4_CTRL_DW2 LRO2_MAX_AGGREGATED_CNT_L 03FFFCBF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_AGGREGATED_CNT_L						MAX_AGG_TIME									
Type	RW						RW									
Reset	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_AGG_TIME						MYIP_VLD	VLD	OP_MODE		AGE_TIME_H					
Type	RW						RW	RW	RW		RW					
Reset	1	1	1	1	1	1	0	0	1	0	1	1	1	1	1	1

Bit(s)	Name	Description
31:26	MAX_AGGREGATED_CNT_L	**To limit max aggregated packets**
25:10	MAX_AGG_TIME	**Maximum aggregation time to flush, = 0 to disable flush**
9	MYIP_VLD	**To validate programmed DIP information**
8	VLD	**To validate programmed flow information**
7:6	OP_MODE	**00 : normal, 01 : PSE, 10 : forced_port, 11 : auto_learn**
5:0	AGE_TIME_H	**Age time to flush LRO ring, = 0 to disable flush**

15106540 LRO2_RING4_CTRL_DW3 Reserved 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV														MAX_AGGREGATED_CNT_H	
Type	RO														RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:2	REV	**To limit max aggregated packets**
1:0	MAX_AGGREGATED_CNT_H	**To limit max aggregated packets**

5.6 RSS

5.6.1 Register Definition

Module name: RSS2 Base address: (+0x15106800)

Address	Name	Width	Register Function
15106800	RSS2_GLO_CFG	32	RSS Global Configuration
15106808	RSS2_GLO_CFG3	32	RSS Global Configuration3
15106820	RSS2_HASH_KEY_DW0	32	RSS Hash Key DW0
15106824	RSS2_HASH_KEY_DW1	32	RSS Hash Key DW1
15106828	RSS2_HASH_KEY_DW2	32	RSS Hash Key DW2
1510682C	RSS2_HASH_KEY_DW3	32	RSS Hash Key DW3
15106830	RSS2_HASH_KEY_DW4	32	RSS Hash Key DW4
15106834	RSS2_HASH_KEY_DW5	32	RSS Hash Key DW5
15106838	RSS2_HASH_KEY_DW6	32	RSS Hash Key DW6
1510683C	RSS2_HASH_KEY_DW7	32	RSS Hash Key DW7
15106840	RSS2_HASH_KEY_DW8	32	RSS Hash Key DW8
15106844	RSS2_HASH_KEY_DW9	32	RSS Hash Key DW9
15106850	RSS2_INDR_TABLE_DW0	32	RSS Indirection Table DW0
15106854	RSS2_INDR_TABLE_DW1	32	RSS Indirection Table DW1
15106858	RSS2_INDR_TABLE_DW2	32	RSS Indirection Table DW2
1510685C	RSS2_INDR_TABLE_DW3	32	RSS Indirection Table DW3
15106860	RSS2_INDR_TABLE_DW4	32	RSS Indirection Table DW4
15106864	RSS2_INDR_TABLE_DW5	32	RSS Indirection Table DW5
15106868	RSS2_INDR_TABLE_DW6	32	RSS Indirection Table DW6
1510686C	RSS2_INDR_TABLE_DW7	32	RSS Indirection Table DW7

15106800 RSS2_GLO_CFG RSS Global Configuration 1F1F3370

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				IPV4_TUPLE_EN								IPV6_TUPLE_EN				
Type				RW								RW				
Reset				1	1	1	1	1				1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		IPV4_TYPE				IPV6_TYPE				INDR_TBL_SIZE			RSS_CFG_RDY	RSS_CFG_REQ	RSS_BUSY	RSS_ENABLE
Type		RW				RW				RW			RO	RW	RO	RW
Reset		0	1	1		0	1	1		1	1	1	0	0	0	0

Bit(s)	Name	Description
28:24	IPV4_TUPLE_EN	**IPv4 Hash Tuple Global Enable** This field controls which hash tuple is valid for IPv4 hash calculation. The invalid (disabled) tuple can be seen as 0x0 when calculating HASH. For example, when SIP is disabled, 2-tuple and 4-tuple hash will not consider SIP. Another example is when DPORT is disabled, 4-tuple hash will not consider DPORT. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation. 5'b00000: Disable All 5'b00010: Enable SIP for HASH 5'b00100: Enable DIP for HASH 5'b01000: Enable SPORT for HASH 5'b10000: Enable DPORT for HASH 5'b11111: Enable DPORT,SPORT,DIP,SIP for HASH Others: Combinations of the above hash tuple
20:16	IPV6_TUPLE_EN	**IPv6 Hash Tuple Global Enable** This field controls which hash tuple is valid for IPv6 hash calculation. See description of IPV4_TUPLE_EN for more detail. Bit Maps: {DPROT,SPORT,DIP,SIP,Reserved} Set the bits to 1 to enable corresponding hash tuple for hash calculation. Set the bits to 0 to disable corresponding hash tuple for hash calculation. 5'b00000: Disable All

Bit(s)	Name	Description
		5'b00010: Enable SIP for HASH 5'b00100: Enable DIP for HASH 5'b01000: Enable SPORT for HASH 5'b10000: Enable DPORT for HASH 5'b11111: Enable DPORT,SPORT,DIP,SIP for HASH Others: Combinations of the above hash tuple
14:12	IPV4_TYPE	**IPv4 Hash Type Selection Flag** This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv4 packets. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} RSS performs the hash calculations as specified for the enabled case. For example, if IPV4_TYPE = 3'b011, RSS will use 4-tuple hash for IPv4 TCP packets and 2-tuple hash for IPv4 non-TCP packets (such as IPv4 fragment packet). 3'b000: Disable IPv4 packets for RSS. RSS does not accept IPv4 packets 3'b001: Enable IPv4 2-tuple hash 3'b010: Enable TCP 4-tuple hash 3'b100: Enable UDP 4-tuple hash 3'b011: Enable IPv4 2-tuple hash + TCP 4-tuple hash 3'b101: Enable IPv4 2-tuple hash + UDP 4-tuple hash 3'b110: TCP 4-tuple hash + UDP 4-tuple hash 3'b111: IPv4 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash
10:8	IPV6_TYPE	**IPv6 Hash Type Selection Flag** This field controls the selection of hash 2-tuple and 4-tuple for different kinds of IPv6 packets. Bit Maps: {UDP 4-tuple,TCP4-tuple,IP 2-tuple} See description of IPV4_TYPE for more detail. 3'b000: Disable IPv6 packets for RSS. RSS does not accept IPv4 packets 3'b001: Enable IPv6 2-tuple hash 3'b010: Enable TCP 4-tuple hash 3'b100: Enable UDP 4-tuple hash 3'b011: Enable IPv6 2-tuple hash + TCP 4-tuple hash 3'b101: Enable IPv6 2-tuple hash + UDP 4-tuple hash

Bit(s)	Name	Description
		3'b110: TCP 4-tuple hash + UDP 4-tuple hash 3'b111: IPv6 2-tuple hash + TCP 4-tuple hash + UDP 4-tuple hash
6:4	INDR_TBL_SIZE	**Change the size of indirection table.** This register field affects how many bits of hash result will be used as the entry of indirection table. For example, INDR_TBL_SIZE = 6 means RSS uses only 6 bits of hash result as indirection table entry, which also means that indirection table has 2^6 = 64 entries. 3'd1: Indirection table size = 2 entries 3'd2: Indirection table size = 4 entries 3'd3: Indirection table size = 8 entries 3'd4: Indirection table size = 16 entries 3'd5: Indirection table size = 32 entries 3'd6: Indirection table size = 64 entries 3'd7: Indirection table size = 128 entries Other: Invalid value
3	RSS_CFG_RDY	**RSS is ready to accept new register configuration.** This register will be asserted after RSS accepted the request from RSS_CFG_REQ. See description of RSS_CFG_REQ for more detail. 0: Not Ready 1: Ready
2	RSS_CFG_REQ	**Request to change RSS register configuration.** When the request is asserted, RSS will be paused after the process of current packet has finished. Note that the asserted RSS_CFG_REQ is required before enabling RSS or changing other register settings (such as indirection table). Must wait until RSS_CFG_RDY = 1 before changing RSS register value (including RSS_ENABLE). 0: Deassert request 1: Assert request
1	RSS_BUSY	**RSS is working or not** 0: RSS IDLE 1: RSS BUSY
0	RSS_ENABLE	**Enable/Disable RSS** 0: Disable RSS 1: Enable RSS

Bit(s)	Name	Description

15106808 RSS2_GLO_CFG3 RSS Global Configuration3 00008100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV															SPC_TAG_EN
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXT_TPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	REV	**Reserved**
16	SPC_TAG_EN	**Enable special tag**
15:0	EXT_TPID	**User extended TPID**

15106820 RSS2_HASH_KEY_DW0 RSS Hash Key DW0 BEAC01FA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	0	1	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 31~0**

15106824 RSS2_HASH_KEY_DW1 RSS Hash Key DW1 6A42B73B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	0	1	1	1	0	0	1	1	1	0	1	1

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 63~32**

15106828 RSS2_HASH_KEY_DW2 RSS Hash Key DW2 8030F20C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 95~64**

1510682C RSS2_HASH_KEY_DW3 RSS Hash Key DW3 77CB2DA3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	1	1	0	1	1	1	1	1	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	0	1	1	0	1	1	0	1	0	0	0	1	1

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 127~96**

15106830 RSS2_HASH_KEY_DW4 RSS Hash Key DW4 AE7B30B4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	0	1	0	1	1	1	0	0	1	1	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	1	0	0	0	0	1	0	1	1	0	1	0	0

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 159~128**

15106834 RSS2_HASH_KEY_DW5 RSS Hash Key DW5 D0CA2BCB

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1	1

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 191~160**

15106838 RSS2_HASH_KEY_DW6 RSS Hash Key DW6 43A38FB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 223~192**

1510683C RSS2_HASH_KEY_DW7 RSS Hash Key DW7 4167253D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	0	1	1	1	1	0	1

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 255~224**

15106840 RSS2_HASH_KEY_DW8 RSS Hash Key DW8 255B0EC2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	0	1	0	0	1	0	1	0	1	0	1	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 287~256**

15106844 RSS2_HASH_KEY_DW9 RSS Hash Key DW9 6D5A56DA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	0	1	1	0	1	1	0	1	0	1	0	1	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	0	1	0	1	0	1	1	0	1	1	0	1	1	0	1	0

Bit(s)	Name	Description
31:0	DATA	**Hash Key bit 319~288**

15106850 RSS2_INDR_TABLE_DW0 RSS Indirection Table DW0 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 15~0** Each entry has 2 bits

15106854 RSS2_INDR_TABLE_DW1 RSS Indirection Table DW1 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 31~16** Each entry has 2 bits

15106858 RSS2_INDR_TABLE_DW2 RSS Indirection Table DW2 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 47~32** Each entry has 2 bits

1510685C RSS2_INDR_TABLE_DW3 RSS Indirection Table DW3 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 63~48** Each entry has 2 bits

15106860 RSS2_INDR_TABLE_DW4 RSS Indirection Table DW4 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 79~64** Each entry has 2 bits

15106864 RSS2_INDR_TABLE_DW5 RSS Indirection Table DW5 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 95~80** Each entry has 2 bits

15106868 RSS2_INDR_TABLE_DW6 RSS Indirection Table DW6 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 111~96** Each entry has 2 bits

1510686C RSS2_INDR_TABLE_DW7 RSS Indirection Table DW7 DEADBEEF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DATA															
Type	RW															
Reset	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DATA															
Type	RW															
Reset	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1

Bit(s)	Name	Description
31:0	DATA	**Indirection Table Entry 127~112** Each entry has 2 bits

5.7 GMAC (Gigabit-Media Access Controller)

5.7.1 Register Definition

Module name: GMAC Base address: (+0x15110000)

Address	Name	Width	Register Function
15110000	MAC_PPSC	32	PHY Polling and SMI Master Control
15110004	MAC_PIAC	32	PHY Indirect Access Control
15110008	MAC_GPC	32	GIGA MAC Port Control
1511000C	MAC_MISC	32	MAC MISC register
15110100	MAC_P1_MCR	32	Port 1 MAC Control
15110104	MAC_P1_EEE	32	Port 1 EEE Control
15110108	MAC_P1_SR	32	Port 1 MAC Status
15110110	MAC_P1_WOL	32	Port 1 WOL
15110114	MAC_P1_SGMII	32	Port 1 SGMII
15110118	MAC_P1_PFC_CTRL	32	Port 1 PFC Control
1511011C	MAC_P1_PFC_STS	32	Port 1 PFC Status
15110120	MAC_P1_PFC_RX_PSON_CNT_L	32	Port 1 RX PFC pause on counter for low priority
15110124	MAC_P1_PFC_RX_PSON_CNT_H	32	Port 1 RX PFC pause on counter for high priority
15110128	MAC_P1_PFC_RX_PSOFF_CNT_L	32	Port 1 RX PFC pause off counter for low priority
1511012C	MAC_P1_PFC_RX_PSOFF_CNT_H	32	Port 1 RX PFC pause off counter for high priority
15110130	MAC_P1_PFC_TX_PSON_CNT_L	32	Port 1 TX PFC pause on counter for low priority
15110134	MAC_P1_PFC_TX_PSON_CNT_H	32	Port 1 TX PFC pause on counter for high priority
15110138	MAC_P1_PFC_TX_PSOFF_CNT_L	32	Port 1 TX PFC pause off counter for low priority
1511013C	MAC_P1_PFC_TX_PSOFF_CNT_H	32	Port 1 TX PFC pause off counter for high priority
15110200	MAC_P2_MCR	32	Port 2 MAC Control
15110204	MAC_P2_EEE	32	Port 2 EEE Control
15110208	MAC_P2_SR	32	Port 2 MAC Status
15110210	MAC_P2_WOL	32	Port 2 WOL
15110214	MAC_P2_SGMII	32	Port 2 SGMII
15110218	MAC_P2_PFC_CTRL	32	Port 2 PFC Control
1511021C	MAC_P2_PFC_STS	32	Port 2 PFC Status
15110220	MAC_P2_PFC_RX_PSON_CNT_L	32	Port 2 RX PFC pause on counter for low priority
15110224	MAC_P2_PFC_RX_PSON_CNT_H	32	Port 2 RX PFC pause on counter for high priority
15110228	MAC_P2_PFC_RX_PSOFF_CNT_L	32	Port 2 RX PFC pause off counter for low priority
1511022C	MAC_P2_PFC_RX_PSOFF_CNT_H	32	Port 2 RX PFC pause off counter for high priority
15110230	MAC_P2_PFC_TX_PSON_CNT_L	32	Port 2 TX PFC pause on counter for low priority
15110234	MAC_P2_PFC_TX_PSON_CNT_H	32	Port 2 TX PFC pause on counter for high priority
15110238	MAC_P2_PFC_TX_PSOFF_CNT_L	32	Port 2 TX PFC pause off counter for low priority
1511023C	MAC_P2_PFC_TX_PSOFF_CNT_H	32	Port 2 TX PFC pause off counter for high priority

15110000 MAC_PPSC PHY Polling and SMI Master Control 45000504

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_AP_EN	PHY_PRE_EN	PHY_MDC_CFG						RESV0			MDC_TURBO	RESV1		EE_AN_EN	
Type	RW	RW	RW						RW			RW	RW		RW	
Reset	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV2			PHY_END_ADDR					RESV3			PHY_START_ADDR				
Type	RW			RW					RW			RW				
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31	PHY_AP_EN	**Enable PHY auto polling** Indicate all PHY's status will be updated to PHY's status registers by PHY polling process.
30	PHY_PRE_EN	**Enable PHY preamble** Indicates SMI master will send preamble bits (32 bits) at each MDIO read/write transaction. [Note] This bit will affect both PHY polling mode and PHY indirect access mode.
29:24	PHY_MDC_CFG	**PHY MDC clock configuration** Used to configure the divider N for MDC clock frequency. MDC clock is sourced from 12.5 MHz system clock and divided by N. [Note] MDC clock is gated or disabled when PHY_MDC_CFG is set to 0.
23:21	RESV0	**Reserved**
20	MDC_TURBO	**MDC clock Turbo mode** When this bit is set, MDC clock is sourced from 25 MHz system clock and divided by PHY_MDC_CFG.
19:18	RESV1	**Reserved**
17:16	EE_AN_EN	**Enable PHY EEE auto-polling**
15:13	RESV2	**Reserved**
12:8	PHY_END_ADDR	**PHY polling end address** Indicate the end of PHY address of PHY auto-polling process. [Note] The difference between start and end must be 1.
7:5	RESV3	**Reserved**
4:0	PHY_START_ADDR	**PHY polling start address** Indicate the start of PHY address of PHY auto-polling process.

15110004 MAC_PIAC PHY Indirect Access Control 00090000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PHY_ACS_ST	RESV0	MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		NMDIO_ST	
Type	W1C	RW	RW					RW					RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MDIO_RW_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PHY_ACS_ST	**PHY access start** Start the indirect access of PHY's register. After PHY's register access is complete, this bit will be self-cleared to 0. 0: Idle or indirect access complete 1: Start PHY access
30	RESV0	**Reserved**
29:25	MDIO_REG_ADDR	**Register Address (Clause 22) or Device Address (Clause 45)**
24:20	MDIO_PHY_ADDR	**PHY Address (Clause 22) or Port Address (Clause 45)**
19:18	MDIO_CMD	**MDIO command** 2'b00: Address (Clause 45) 2'b01: MDIO write 2'b10: MDIO read (Clause 22)/Read inc (Clause 45) 2'b11: MDIO read (Clause 45)
17:16	NMDIO_ST	**MDIO Start Field** 2'b00: Start (Clause 45) 2'b01: Start (Clause 22) other: Reserved
15:0	MDIO_RW_DATA	**MDIO Read/Write data** This is used as MDIO data field for read/write data access. When MDIO write command is activated, this is used as MDIO write data field. When MDIO read command is activated, this is used as MDIO read data field for read access only.

15110008 MAC_GPC GIGA MAC Port Control 400C400C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RESV0				P2_RMII_CKRX	P2_RMII_CKIN	P2_TMII_FREQ	P2_TMII_MODE	P2_TX_CLK_MODE	P2_RX_CLK_MODE	P2_RX_SKEW	
Type					RW				RW	RW	RW	RW	RW	RW	RW	
Reset					0	0	0		0	0	0	0	1	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RESV2		P1_TMII_FREQ	P1_TMII_MODE	P1_TX_CLK_MODE	P1_RX_CLK_MODE	P1_RX_SKEW	
Type									RW		RW	RW	RW	RW	RW	
Reset									0	0	0	0	1	1	0	0

Bit(s)	Name	Description
27:25	RESV0	**Reserved**
23	P2_RMII_CKRX	**RMII Reference Clock Pin Selection** 0: TXC 1: RXC
22	P2_RMII_CKIN	**RMII Reference Clock Direction** 0: Output 1: Input
21	P2_TMII_FREQ	**TMII frequency**
20	P2_TMII_MODE	**TMII mode** Switch to Turbot MII mode
19	P2_TX_CLK_MODE	**P2 TX clock control** 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data are 90 degree offset)
18	P2_RX_CLK_MODE	**P2 RX clock control** 0: Delay 2ns on input rx_clk 1: No delay
17:16	P2_RX_SKEW	**P2 RX clock skew control** 2'b00: No delay 2'b01: Delay 150ps 2'b10: Delay 300ps 2'b11: Clock inversion
7:6	RESV2	**Reserved**
5	P1_TMII_FREQ	**TMII frequency**

Bit(s)	Name	Description
4	P1_TMII_MODE	**TMII mode** Switch to Turbot MII mode
3	P1_TX_CLK_MODE	**P1 TX clock control** 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data are 90 degree offset)
2	P1_RX_CLK_MODE	**P1 RX clock control** 0: Delay 2ns on input rx_clk 1: No delay
1:0	P1_RX_SKEW	**P1 RX clock skew control** 2'b00: No delay 2'b01: Delay 150ps 2'b10: Delay 300ps 2'b11: Clock inversion

1511000C MAC_MISC MAC MISC register 80000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTO_POLLING_1G	RESV														
Type	RW	RW														
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV															ESW_MUX_SEL
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	AUTO_POLLING_1G	1'b0: Disable auto polling 1G 1'b1: Enable auto polling 1G
30:1	RESV	**Reserved**
0	ESW_MUX_SEL	1'b0: MUX selection from gmac1 to gdm1 1'b1: MUX selection from switch to gdm1

15110100 MAC_P1_MCR Port 1 MAC Control 20006300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_RX_JUMBO				RESV0		MAC_RX_PKT_LEN		MTCC_LMT				IPG_CFG		RESV1	DIFF_RXFIFO_WCLR
Type	RW				RW		RW		RW				RW		RW	RW
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE	MAC_TX_EN	MAC_RX_EN	DEL_RXFIFO_CLR	GMAC_RDMA_HANG_ECO_ROLLBACK	PRMBL_LMT_EN	BKOFF_EN	BACKPR_EN	FORCE_EEE1G	FORCE_EEE100	FORCE_RX_FC	FORCE_TX_FC	FORCE_SPD		FORCE_DPX	FORCE_LINK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_RX_JUMBO	**Maximum received jumbo packet length** 4'h0, 4'h1: Reserved 4'h2: 2 Kbytes (max. length on FE/GDM) 4'h3 ... 4'hF: Reserved
27:26	RESV0	**Reserved**
25:24	MAC_RX_PKT_LEN	**Maximum received packet length** Sets the maximum length of ingress packets including CRC that can be received by MAC. 2'b00: 1518 bytes for untagged frames; 1522 bytes for tagged frames 2'b01: 1536 bytes 2'b10: 1552 bytes 2'b11: MAX_RX_JUMBO
23:20	MTCC_LMT	**MTCC limit** Maximum transmit collision count limitation. 0: Disable TX collision abort function; send packet until success 1 ~ 15: Maximum transmit collision count
19:18	IPG_CFG	**Inter-Frame Gap Shrink** 2'b00: Normal 96-bit IFG 2'b01: Transmit 96-bit IFG with short IFG in random behavior. 2'b10: shrink 64-bit IFG 2'b11: When any output queue inside the port is congested, shrink 64-bit IFG will be enabled; otherwise, normal 96-bit IFG will be the default.
17	RESV1	**Reserved**

Bit(s)	Name	Description
16	DIFF_RXFIFO_WCLR	**Change RX FIFO wclear function** 0: Remain RX FIFO wclear function 1: Change RX FIFO wclear function
15	FORCE_MODE	**Force MAC Mode** 0: Force mode off (MAC status is decided by PHY auto-polling) 1: Force mode on (MAC status is determined by FORCE_XXX register)
14	MAC_TX_EN	**Enable TX MAC** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN	**Enable RX MAC** 0: RX MAC function is disabled 1: RX MAC function is enabled
12	DEL_RXFIFO_CLR	**Disable RX FIFO clear function** 0: Remain RX FIFO clear function 1: Break RX FIFO clear function
11	GMAC_RDMA_HANG_ECO_ROLLBACK	**Rollback ECO for GMAC RDMA hang issue** 0: ECO is enabled 1: Rollback ECO
10	PRMBL_LMT_EN	**Enable Preamble Limit** 0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble. 1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD.
9	BKOFF_EN	**Enable Back-off** 0: Disabled 1: Let MAC follow the back-off mechanism when collision happens
8	BACKPR_EN	**Enable Back-Pressure** 0: Disabled 1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on
7	FORCE_EEE1G	**Force LPI mode for 1000m link speed** When (FORCE_MODE = 1), these bits are used to control MAC EEE mode

Bit(s)	Name	Description
		0: Do not have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	FORCE_EEE100	**Force LPI mode for 100m link speed** When (FORCE_MODE = 1), these bits are used to control MAC EEE mode 0: Do not have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	FORCE_RX_FC	**Force RX flow control** When (FORCE_MODE = 1), these bits are used to control MAC RX flow control 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	FORCE_TX_FC	**Force TX flow control** When (FORCE_MODE = 1), these bits are used to control MAC TX flow control 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	FORCE_SPD	**Force link speed** When (FORCE_MODE = 1), these bits are used to control MAC link speed 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: Reserved
1	FORCE_DPX	**Force duplex** When (FORCE_MODE = 1), these bits are used to control MAC link duplex 0: Half-duplex 1: Full-duplex
0	FORCE_LINK	**Force link state** When (FORCE_MODE = 1), these bits are used to control MAC link state 0: Link down 1: Link up

15110104 MAC_P1_EEE Port 1 EEE Control 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000								WAKEUP_TIME_100							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_TXIDLE_THD								RESV0				CKG_TXIDLE	CKG_RXLPI		LPI_MODE
Type	RW								RW				RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000	**Wake-up time for 1000mbps LPI mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packets after wake-up Time unit: 1us
23:16	WAKEUP_TIME_100	**Wake-up time for 100mbps LPI mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packets after wake-up Time unit: 1us
15:8	LPI_TXIDLE_THD	**TX IDLE timer to enter LPI mode** When there is no packet to be transmitted and the time period specified by LPI_TXIDLE_THD is exceeded, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner Time unit: 1ms
7:4	RESV0	**Reserved**
3	CKG_TXIDLE	**TX Clock Power Down** 0: Disable 1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.
2	CKG_RXLPI	**RX Clock Power Down** 0: Disable 1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.
0	LPI_MODE	**LPI mode activated** 0: Disable 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner

15110108 MAC_P1_SR Port 1 MAC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0								EEE1G_STATUS	EEE100_STATUS	RX_FC_STATUS	TX_FC_STATUS	SPD_STATUS		DPX_STATUS	LINK_STATUS
Type	RO								RO	RO	RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV0	**Reserved**
7	EEE1G_STATUS	**LPI mode for 1000m link speed** 0: Do not have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	EEE100_STATUS	**LPI mode for 100m link speed** 0: Do not have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	RX_FC_STATUS	**RX flow control status** 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	TX_FC_STATUS	**TX flow control status** 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	SPD_STATUS	**Link speed status** 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: reserved
1	DPX_STATUS	**Duplex status** 0: Half-duplex 1: Full-duplex
0	LINK_STATUS	**Link state**

Bit(s)	Name	Description
		0: Link down 1: Link up

15110110 MAC_P1_WOL Port 1 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_INT_STS	WOL_STS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0												SNP_PKT	CRC_DIS	WOL_INT_EN	WOL_EN
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	**GMAC1 Wake-up On Lan Debug Signals**
17	WOL_INT_STS	**GMAC1 Wake-up On Lan Interrupt Status**
16	WOL_STS	**GMAC1 Wake-up On Lan Status** If WOL_EN is enabled, this bit will change from 0 to 1 when GMAC RX state machine enters IDLE state. It indicates GMAC will drop all packets and detect magic packet. 0: Normal State 1: Listen State and detect magic packet
15:4	RESV0	**Reserved**
3	SNP_PKT	**GMAC1 Wake-up On Lan with snoopy packet**
2	CRC_DIS	**Disable GMAC1 Wake-up On Lan with CRC**
1	WOL_INT_EN	**Enable GMAC1 Wake-up On Lan Interrupt**
0	WOL_EN	**Enable GMAC1 Wake-up On Lan Function**

15110114 MAC_P1_SGMII Port 1 SGMII 050B0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOADPSTMR_EXTEND_TIME								SYNCDONE_TIME							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIS_TXCLK_ENA
Type																RW
Reset																1

Bit(s)	Name	Description
31:24	LOADPSTMR_EXTEND_TIME	**rxc_loadpstmr extend time in SGMII mode**
23:16	SYNCDONE_TIME	**Sync done time for RX flow control in SGMII mode**
0	DIS_TXCLK_ENA	**Disable txclk_ena in SGMII mode** 0: SGMII txclk_ena is enabled 1: SGMII txclk_ena is disabled

15110118 MAC_P1_PFC_CTRL Port 1 PFC Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV												PFC_AUTO_SYNC_DLY		PFC_SYNC_EN	PFC_EN
Type	RW												RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	RESV	**Reserved**
3:2	PFC_AUTO_SYNC_DLY	**Select the delay of sending PFC auto sync packet** 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
1	PFC_SYNC_EN	**Enable the PFC auto-sync ability** 0: Disable 1: Enable
0	PFC_EN	**Enable the PFC ability** 0: Disable 1: Enable

1511011C MAC_P1_PFC_STS Port 1 PFC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															PFC_AUTO_EN
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	RESV	**Reserved**
16	PFC_AUTO_EN	**PFC auto enable status** 0: Disable 1: Enable
31:17	TX_PFC_STS	**TX PFC status**
7:0	RX_PFC_STS	**RX PFC status**

15110120 MAC_P1_PFC_RX_PSON_CNT_L Port 1 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 3**
23:16	Q2_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 2**
15:8	Q1_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 1**
7:0	Q0_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 0**

15110124 MAC_P1_PFC_RX_PSON_CNT_H Port 1 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 7**
23:16	Q6_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 6**
15:8	Q5_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 5**
7:0	Q4_RX_PSON_CNT	**PFC RX pause on count for port 1 priority 4**

15110128 MAC_P1_PFC_RX_PSOFF_CNT_L Port 1 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 3**
23:16	Q2_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 2**
15:8	Q1_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 1**
7:0	Q0_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 0**

1511012C MAC_P1_PFC_RX_PSOFF_CNT_H Port 1 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 7**
23:16	Q6_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 6**
15:8	Q5_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 5**
7:0	Q4_RX_PSOFF_CNT	**PFC RX pause off count for port 1 priority 4**

15110130 MAC_P1_PFC_TX_PSON_CNT_L Port 1 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 3**
23:16	Q2_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 2**
15:8	Q1_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 1**
7:0	Q0_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 0**

15110134 MAC_P1_PFC_TX_PSON_CNT_H Port 1 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 7**
23:16	Q6_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 6**
15:8	Q5_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 5**
7:0	Q4_TX_PSON_CNT	**PFC TX pause on count for port 1 priority 4**

15110138 MAC_P1_PFC_TX_PSOFF_CNT_L Port 1 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 3**
23:16	Q2_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 2**
15:8	Q1_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 1**
7:0	Q0_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 0**

1511013C MAC_P1_PFC_TX_PSOFF_CNT_H Port 1 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 7**
23:16	Q6_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 6**
15:8	Q5_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 5**
7:0	Q4_TX_PSOFF_CNT	**PFC TX pause off count for port 1 priority 4**

15110200 MAC_P2_MCR Port 2 MAC Control 20006300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_RX_JUMBO				RESV0		MAC_RX_PKT_LEN		MTCC_LMT				IPG_CFG		RESV1	DIFF_RXFIFO_WCLR
Type	RW				RW		RW		RW				RW		RW	RW
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FORCE_MODE	MAC_TX_EN	MAC_RX_EN	DEL_RXFIFO_CLR	GMAC_RDMA_HANG_ECO_ROLLBACK	PRMBL_LMT_EN	BKOFF_EN	BACKPR_EN	FORCE_EEE1G	FORCE_EEE100	FORCE_RX_FC	FORCE_TX_FC	FORCE_SPD		FORCE_DPX	FORCE_LINK
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	MAX_RX_JUMBO	**Maximum received jumbo packet length** 4'h0, 4'h1: Reserved 4'h2: 2 Kbytes (maxi. length on FE/GDM) 4'h3 ... 4'hF: Reserved
27:26	RESV0	**Reserved**
25:24	MAC_RX_PKT_LEN	**Maximum received packet length** Sets the maximum length of ingress packets including CRC that can be received by MAC. 2'b00: 1518 bytes for untagged frames; 1522 bytes for tagged frames 2'b01: 1536 bytes 2'b10: 1552 bytes 2'b11: MAX_RX_JUMBO
23:20	MTCC_LMT	**MTCC limit** Maximum transmit collision count limitation. 0: Disable TX collision abort function, and send packets until success 1 ~ 15: Maximum transmit collision count
19:18	IPG_CFG	**Inter-Frame Gap Shrink** 2'b00: normal 96-bit IFG 2'b01: Transmit 96-bit IFG with short IFG in random behavior. 2'b10: shrink 64-bit IFG 2'b11: When any output queue inside the port is congested, shrink 64-bit IFG will be enabled; otherwise, normal 96-bit IFG will be the default.
17	RESV1	**Reserved**

Bit(s)	Name	Description
16	DIFF_RXFIFO_WCLR	**Change RX FIFO wclear function** 0: Remain RX FIFO wclear function 1: Change RX FIFO wclear function
15	FORCE_MODE	**Force MAC Mode** 0: Force mode off (MAC status is decided by PHY auto-polling) 1: Force mode on (MAC status is determined by FORCE_XXX register)
14	MAC_TX_EN	**Enable TX MAC** 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN	**Enable RX MAC** 0: RX MAC function is disabled 1: RX MAC function is enabled
12	DEL_RXFIFO_CLR	**Disable RX FIFO clear function** 0: Remain RX FIFO clear function 1: Break RX FIFO clear function
11	GMAC_RDMA_HANG_ECO_ROLLBACK	**Rollback ECO for GMAC RDMA hang issue** 0: ECO is enabled 1: Rollback ECO
10	PRMBL_LMT_EN	**Enable Preamble Limit** 0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble. 1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD.
9	BKOFF_EN	**Enable Back-off** 0: Disabled 1: Let MAC follow the back-off mechanism when collision happens
8	BACKPR_EN	**Enable Back-Pressure** 0: Disabled 1: Enable back-pressure mechanism when operating in half-duplex mode and flow-control is on
7	FORCE_EEE1G	**Force LPI mode for 1000m link speed** When (FORCE_MODE = 1), these bits are used to control MAC EEE mode

Bit(s)	Name	Description
		0: Do not have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	FORCE_EEE100	**Force LPI mode for 100m link speed** When (FORCE_MODE = 1), these bits are used to control MAC EEE mode 0: Do not have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	FORCE_RX_FC	**Force RX flow control** When (FORCE_MODE = 1), these bits are used to control MAC RX flow control 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	FORCE_TX_FC	**Force TX flow control** When (FORCE_MODE = 1), these bits are used to control MAC TX flow control 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	FORCE_SPD	**Force link speed** When (FORCE_MODE = 1), these bits are used to control MAC link speed 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: reserved
1	FORCE_DPX	**Force duplex** When (FORCE_MODE = 1), these bits are used to control MAC link duplex 0: Half-duplex 1: Full-duplex
0	FORCE_LINK	**Force link state** When (FORCE_MODE = 1), these bits are used to control MAC link state 0: Link down 1: Link up

15110204 MAC_P2_EEE Port 2 EEE Control 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000								WAKEUP_TIME_100							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_TXIDLE_THD								RESV0				CKG_TXIDLE	CKG_RXLPI		LPI_MODE
Type	RW								RW				RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000	**Wake-up time for 1000mbps LPI mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packets after wake-up Time unit: 1us
23:16	WAKEUP_TIME_100	**Wake-up time for 100mbps LPI mode** The minimum allowed time needed to wait for PHY to be fully functional and TXMAC can transmit packets after wake-up Time unit: 1us
15:8	LPI_TXIDLE_THD	**TX IDLE timer to enter LPI mode** When there is no packet to be transmitted and the time period specified by LPI_TXIDLE_THD is exceeded, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI signal to link partner. Time unit: 1ms
7:4	RESV0	**Reserved**
3	CKG_TXIDLE	**TX Clock Power Down** 0: Disable 1: Stop TX clock when the corresponding port has no traffic to send and has entered IDLE state for <LPI_TXIDLE_THD> ms.
2	CKG_RXLPI	**RX Clock Power Down** 0: Disable 1: Stop RX clock ticking when the corresponding port entering the LPI mode and IDLE state.
0	LPI_MODE	**LPI mode activated** 0: Disable 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner

15110208 MAC_P2_SR Port 2 MAC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0								EEE1G_STATUS	EEE100_STATUS	RX_FC_STATUS	TX_FC_STATUS	SPD_STATUS		DPX_STATUS	LINK_STATUS
Type	RO								RO	RO	RO	RO	RO		RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:8	RESV0	**Reserved**
7	EEE1G_STATUS	**LPI mode for 1000m link speed** 0: Do not have the ability of entering EEE low power idle mode for 1000m link speed 1: Have the ability of entering EEE low power idle mode
6	EEE100_STATUS	**LPI mode for 100m link speed** 0: Do not have the ability of entering EEE low power idle mode for 100m link speed 1: Have the ability of entering EEE low power idle mode
5	RX_FC_STATUS	**RX flow control status** 0: Disable 1: Let MAC accept the pause frame when operating in full-duplex mode and flow-control is on
4	TX_FC_STATUS	**TX flow control status** 0: Disable 1: Let MAC transmit the pause frame when operating in full-duplex mode and flow-control is on
3:2	SPD_STATUS	**Link speed status** 2'b00: 10mbps 2'b01: 100mbps 2'b10: 1000mbps 2'b11: Reserved
1	DPX_STATUS	**Duplex status** 0: Half-duplex 1: Full-duplex
0	LINK_STATUS	**Link state**

Bit(s)	Name	Description
		0: Link down 1: Link up

15110210 MAC_P2_WOL Port 2 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_INT_STS	WOL_STS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV0												SNP_PKT	CRC_DIS	WOL_INT_EN	WOL_EN
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	**GMAC2 Wake-up On Lan Debug Signals**
17	WOL_INT_STS	**GMAC2 Wake-up On Lan Interrupt Status**
16	WOL_STS	**GMAC2 Wake-up On Lan Status** If WOL_EN is enabled, this bit will change from 0 to 1 when GMAC RX state machine enters IDLE state. It indicates GMAC will drop all packets and detect magic packet. 0: Normal State 1: Listen State and detect magic packet
15:4	RESV0	**Reserved**
3	SNP_PKT	**GMAC2 Wake-up On Lan with snoopy packet**
2	CRC_DIS	**Disable GMAC2 Wake-up On Lan with CRC**
1	WOL_INT_EN	**Enable GMAC2 Wake-up On Lan Interrupt**
0	WOL_EN	**Enable GMAC2 Wake-up On Lan Function**

15110214 MAC_P2_SGMII Port 2 SGMII 050B0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LOADPSTMR_EXTEND_TIME								SYNCDONE_TIME							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DIS_TXCLK_ENA
Type																RW
Reset																1

Bit(s)	Name	Description
31:24	LOADPSTMR_EXTEND_TIME	**rxc_loadpstmr extend time in SGMII mode**
23:16	SYNCDONE_TIME	**Sync done time for RX flow control in SGMII mode**
0	DIS_TXCLK_ENA	**Disable txclk_ena in SGMII mode** 0: SGMII txclk_ena is enabled 1: SGMII txclk_ena is disabled

15110218 MAC_P2_PFC_CTRL Port 2 PFC Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV												PFC_AUTO_SYNC_DLY		PFC_SYNC_EN	PFC_EN
Type	RW												RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	RESV	**Reserved**
3:2	PFC_AUTO_SYNC_DLY	**Select the delay of sending PFC auto sync packet** 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
1	PFC_SYNC_EN	**Enable the PFC auto-sync ability** 0: Disable 1: Enable
0	PFC_EN	**Enable the PFC ability** 0: Disable 1: Enable

1511021C MAC_P2_PFC_STS Port 2 PFC Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV															PFC_AUTO_EN
Type	RO															RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:17	RESV	**Reserved**
16	PFC_AUTO_EN	**PFC auto enable status** 0: Disable 1: Enable
15:8	TX_PFC_STS	**TX PFC status**
7:0	RX_PFC_STS	**RX PFC status**

15110220 MAC_P2_PFC_RX_PSON_CNT_L Port 2 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 3**
23:16	Q2_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 2**
15:8	Q1_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 1**
7:0	Q0_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 0**

15110224 MAC_P2_PFC_RX_PSON_CNT_H Port 2 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 7**
23:16	Q6_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 6**
15:8	Q5_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 5**
7:0	Q4_RX_PSON_CNT	**PFC RX pause on count for port 2 priority 4**

15110228 MAC_P2_PFC_RX_PSOFF_CNT_L Port 2 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 3**
23:16	Q2_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 2**
15:8	Q1_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 1**
7:0	Q0_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 0**

1511022C MAC_P2_PFC_RX_PSOFF_CNT_H Port 2 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 7**
23:16	Q6_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 6**
15:8	Q5_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 5**
7:0	Q4_RX_PSOFF_CNT	**PFC RX pause off count for port 2 priority 4**

15110230 MAC_P2_PFC_TX_PSON_CNT_L Port 2 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 3**
23:16	Q2_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 2**
15:8	Q1_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 1**
7:0	Q0_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 0**

15110234 MAC_P2_PFC_TX_PSON_CNT_H Port 2 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 7**
23:16	Q6_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 6**
15:8	Q5_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 5**
7:0	Q4_TX_PSON_CNT	**PFC TX pause on count for port 2 priority 4**

15110238 MAC_P2_PFC_TX_PSOFF_CNT_L Port 2 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 3**
23:16	Q2_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 2**
15:8	Q1_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 1**
7:0	Q0_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 0**

1511023C MAC_P2_PFC_TX_PSOFF_CNT_H Port 2 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 7**
23:16	Q6_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 6**
15:8	Q5_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 5**
7:0	Q4_TX_PSOFF_CNT	**PFC TX pause off count for port 2 priority 4**

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